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New embedded DDSCR structure with high holding voltage and high robustness for 12-V applications*

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A new dual directional silicon-controlled rectifier based electrostatic discharge (ESD) protection device suitable for 12-V applications is proposed in this paper. The proposed device (NPEMDDSCR) is based on the embedded DDSCR (EMDDSCR) structure, in which the P+ electrode and P+ injection are removed from the inner finger. Compared with the conventional modified DDSCR (MDDSCR), its high holding voltage meets the requirements for applications. Compared with the embedded DDSCR (EMDDSCR), it has good conduction uniformity. The MDDSCR, EMDDSCR, and NPEMDDSCR are fabricated with an identical width in a 0.5-μm CDMOS process. In order to verify and predict the characteristics of the proposed ESD protection device, a transmission line pulse (TLP) testing system and a two-dimensional device simulation platform are used in this work. The measurements demonstrate that the NPEMDDSCR provides improved reliability and higher area efficiency for 12 V or similar applications. The measurement results also show that the NPEMDDSCR provides higher robustness and better latch-up immunity capability.

Keywords: DDSCR, holding voltage, failure current, conduction uniformity

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1. Introduction

With the development of silicon metal–oxide–semiconductor (Si MOS) technology, the availability of effective electrostatic discharge (ESD) protection solutions becomes more and more important. Although many ESD devices have been developed to solve this common reliability problem, the ESD structures with robustness and area efficiency are still difficult to obtain. Silicon controlled rectifier (SCR) is a kind of electrostatic discharge device with great development prospects, but its high triggering voltage and low holding voltage make it easy to suffer latch-up.[1,2] At present, there are some methods to improve the holding voltage. A simple and effective method is to increase the base width of the parasitic bipolar junction transistor.[3–5] In Ref. [6], the authors proposed a six-layer p–n–p–n–p–n structure to improve the holding voltage. Segmentation techniques were discussed in Refs. [7–9] to reduce emitter injection efficiency and achieve relatively high holding voltage. Their common shortcomings are that they sacrifice certain robustness for high holding voltage. Therefore, we must increase the finger length and finger number to improve the robustness. However, Wang *et al*. pointed out that the holding voltage of traditional DDSCR would decrease with the increase of finger number in the 0.5-μm CDMOS process.[10] Thus, between the high holding voltage and high area efficiency there seems to be an irreconcilable contradiction. At this time, Guan *et al*. proposed an embedded interdigital structure, which can effectively solve this contradiction.[11] The 2-finger embedded structure is in the form of the outer finger containing the inner finger, unlike the traditional structure which shares the anode. It can not only improve the robustness, but also maintain the holding voltage of the multi-finger device. However, the structure also has a defect of uneven conduction in this 0.5-μm CDMOS process, which is different from the process in Ref. [11], so the device will fail in advance, and can not meet the requirements for high robustness. At present, most of the existing papers focus on the improvement of the conduction uniformity of MOS structure,[12] only a few papers deal with the conduction uniformity of SCR structure.

In this paper, an improved embedded structure is proposed by removing P+ electrode and P+ injection from the inner finger in the device structure that was proposed in Ref. [11]. It can achieve the objectives of high area efficiency and high holding voltage. Through theoretical analysis and TCAD simulation, the influence of removing the P+ region on the device's holding voltage is verified. The TLP testing results confirm that the improved embedded structure not only obtains a higher holding voltage, but also increases the de-

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vice's failure current.

2. Device structure

A 2-finger MDDSCR with a P+ diffusion region inserted between the NWD and PW regions is shown in Fig. 1(a). The breakdown voltage of the DDSCR is determined by the NWD/P+ junction, rather than the NWD/PW junction in the conventional SCR, resulting in a decreased trigger voltage.[13] A new method of realizing an embedded structure was proposed in Ref. [11], which is called the EMDDSCR as shown in Fig. 1(b). The embedded structure adds an anode and cathode on each side of the MDDSCR to ensure that the holding voltage depends on the critical size of inner finger Unfortunately, this kind of embedded structure may cause the well-resistance to change in different processes and may cause the uneven current conduction. Therefore, in this article, an improved embedded structure NPEMDDSCR is proposed. The cross section view of the NPEMDDSCR is shown in Fig. 1(c). Comparing with the EMDDSCR, the P+ electrode and P+ injection of the internal finger are removed, and the remaining part is consistent with the traditional embedded structure. The inner finger refers to anode and inside cathode, and the outer finger means the anode and outside cathode, thus forming an embedded structure to discharge current. The two-finger equivalent circuit diagram of MDDSCR, EMDDSCR, and NPEMDDSCR are shown in Fig. 2, with red arrow representing the forward path and the blue arrow denoting the reverse path.

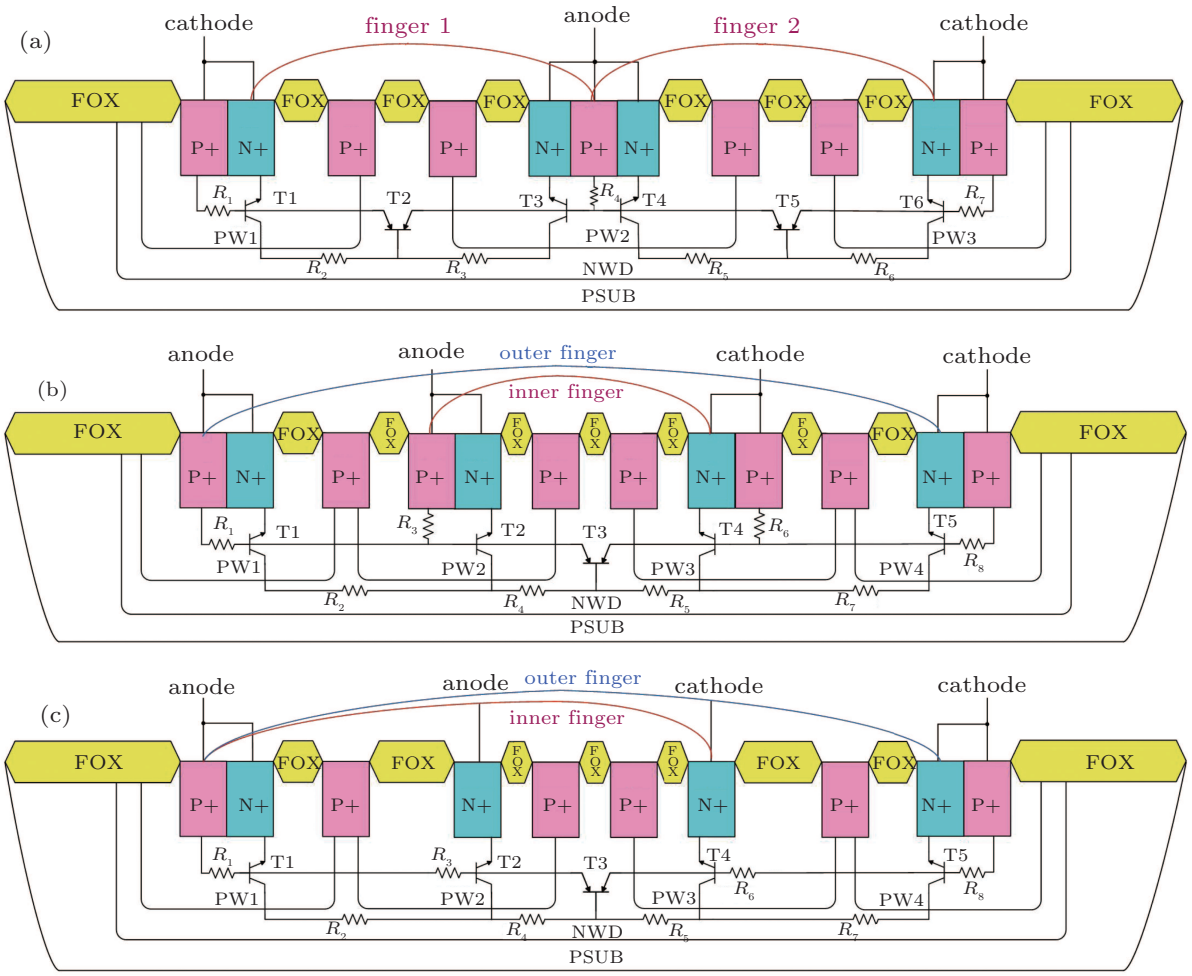


Fig. 1. Cross-section view of 2-finger DDSCR of (a) MDDSCR, (b) EMDDSCR, and (c) NPEMDDSCR.

When an ESD event occurs at the anode of the device, an avalanche breakdown will take place in the PN junction formed by NWD and P+ on the left side of PW3 first. As the hole current increases, the voltage drop between the base and emitter junction of parasitic transistor T4 increases (Vbe) and T4 eventually turns on. Unlike the EMDDSCR, the base resistance of parasitic transistor T4 is changed from resistor R_6 to the series-connected resistors R_6 and R_8 due to the removed P+ injection of the internal finger. Therefore, inside parasitic transistor T4 is easier to turn on than T6. The conduction of transistor T4 will provide the base current for T3, which forms a positive feedback working mechanism. Therefore, the internal SCR path is completely formed as shown in Fig. 2(c) by the red arrow of inner finger. The turn-on of the inner finger causes more and more current to

flow from the PW3 of inner finger, through the P+, to the PW4 of outer finger. The current through resistor R_8 slowly increases, and parasitic transistor T5 eventually turns on. Parasitic transistors T5 and T3 also form positive feedback, making the outer finger turn on, which is shown in Fig. 2(c) by the red arrow of outer finger.

When a positive ESD pulse is applied to the cathode since the device structure is symmetrical, its working process is similar to that of positive ESD pulse applied to the anode. But the triggering will occur on the junction of P+/NWD on the other side Its working path is shown in the blue arrow in Fig. 2(c).

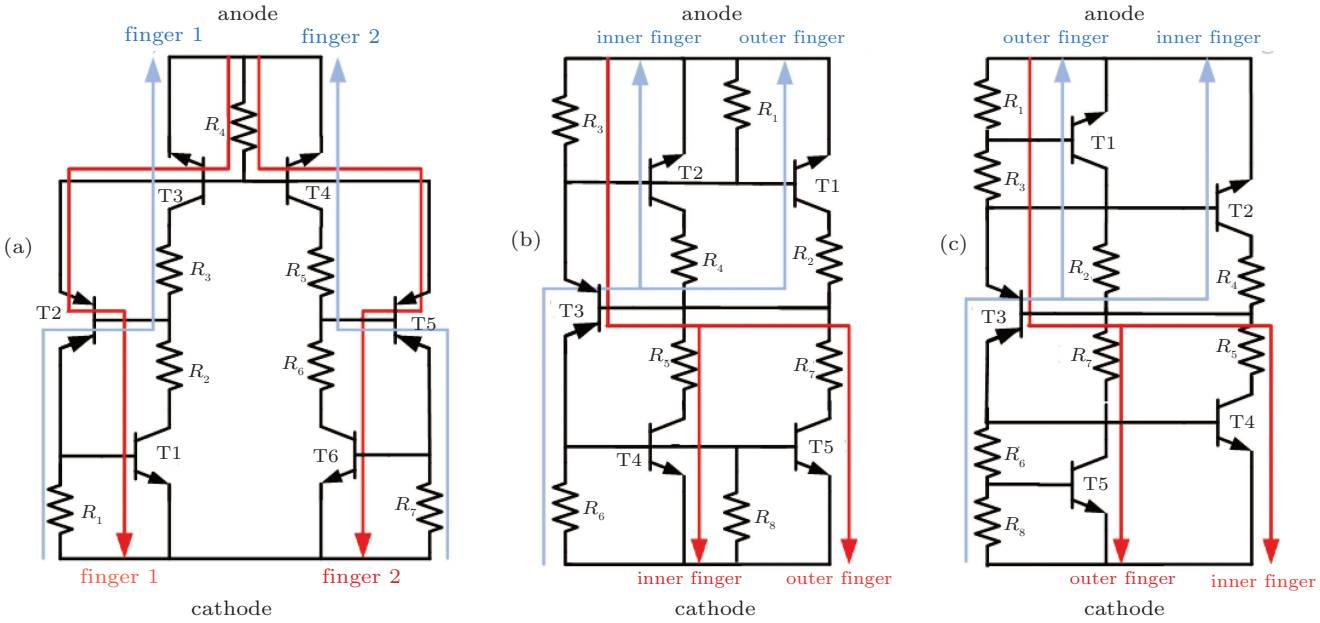


Fig. 2. Equivalent circuit of 2-finger DDSCR of (a) MDDSCR, (b) EMDDSCR, and (c) NPEMDDSCR.

3. Simulation and analysis

The Atlas 2D device simulator by Silvaco Corporation is applied to verifying the operation process of the proposed structure mentioned above. Figure 3 shows the TCAD simulated cross section of the MDDSCR, the EMDDSCR, and the NPEMDDSCR. The principle of operation of the proposed ESD protection device is shown below.

Figure 4 shows the total current flow of the MDDSCR, EMDDSCR, and NPEMDDSCR in the trigger point, holding point, and high ESD current pulse in sequence. When an ESD surge is applied to the anode, the potentials at the anode PW increase. If the potential reaches the threshold voltage, avalanche breakdown occurs in the P+ bridge and the NWD,

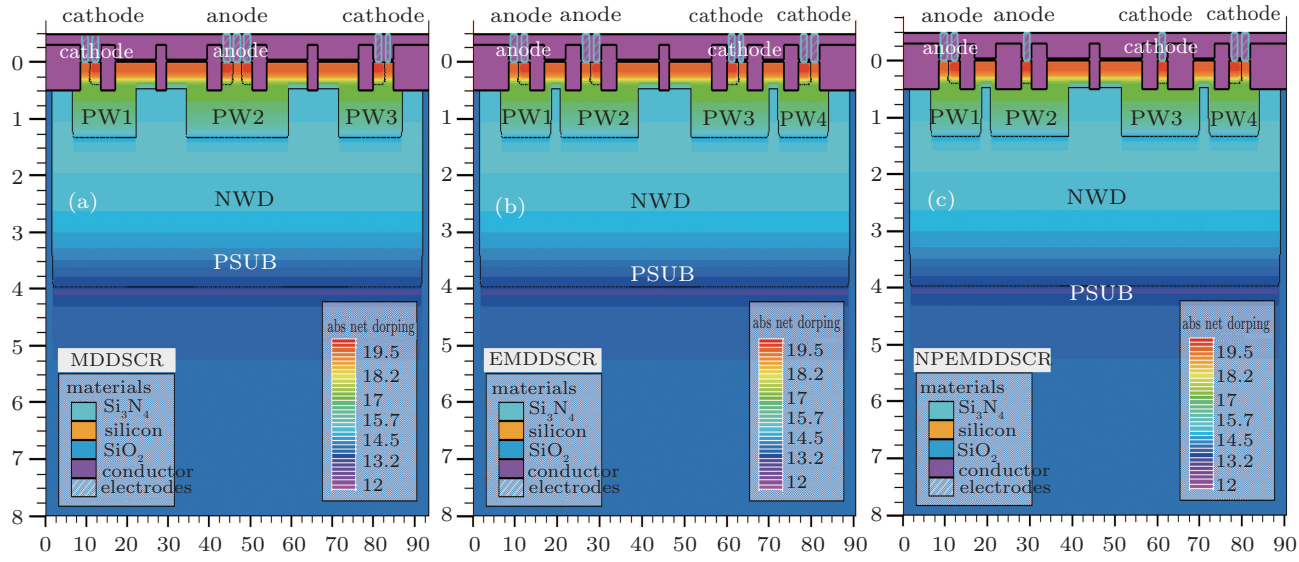


Fig. 3. TCAD simulated cross section of (a) MDDSCR, (b) EMDDSCR, and (c) NPEMDDSCR.

where the electron-hole pairs are generated. This phenomenon is confirmed by the impact ionization simulation results as shown in Fig. 5. The avalanche breakdown surfaces of the three devices are the identical. However, the 2-finger-MDDSCR has two avalanche breakdown surfaces, which will increase the risk of uneven conduction. At the trigger point as shown in Fig. 4(a), the 2-finger-MDDSCR device has a current flowing from the anode to the cathode on both sides. The trigger current of EMDDSCR device only flows from the anode of the inner finger to the cathode of the inner finger, which is because the on-resistance of external finger is larger than that of internal finger. Unlike the EMDDSCR, due to the removal of the P+ electrode and P+ injection for internal finger, the trigger current of NPEMDDSCR must flow from the anode to cathode via the anode P+, PW1, PW2, NWD, PW3, PW4, and cathode P+. At the holding point, the base resistance of NPN transistor T4 of inner finger is larger, so it is turned on before transistor T5 of outer finger. The inner finger of NPEMDDSCR begins to discharge current. Under high level ESD pulse, more and more current flows from the PW3 of inner finger, through P+, to the PW4 of outer finger. The parasitic transistor T5 of the outer finger also conducts, so that the outer finger SCR path is formed by transistors T3 and T5. As for EMDDSCR device, no matter what level the ESD pulse can reach, the current distribution is mainly concentrated in the inner finger. This is because the on-resistance on the current path of the outer finger is larger than that of the inner finger, and it shares less current, resulting in poor conduction uniformity of the whole device.

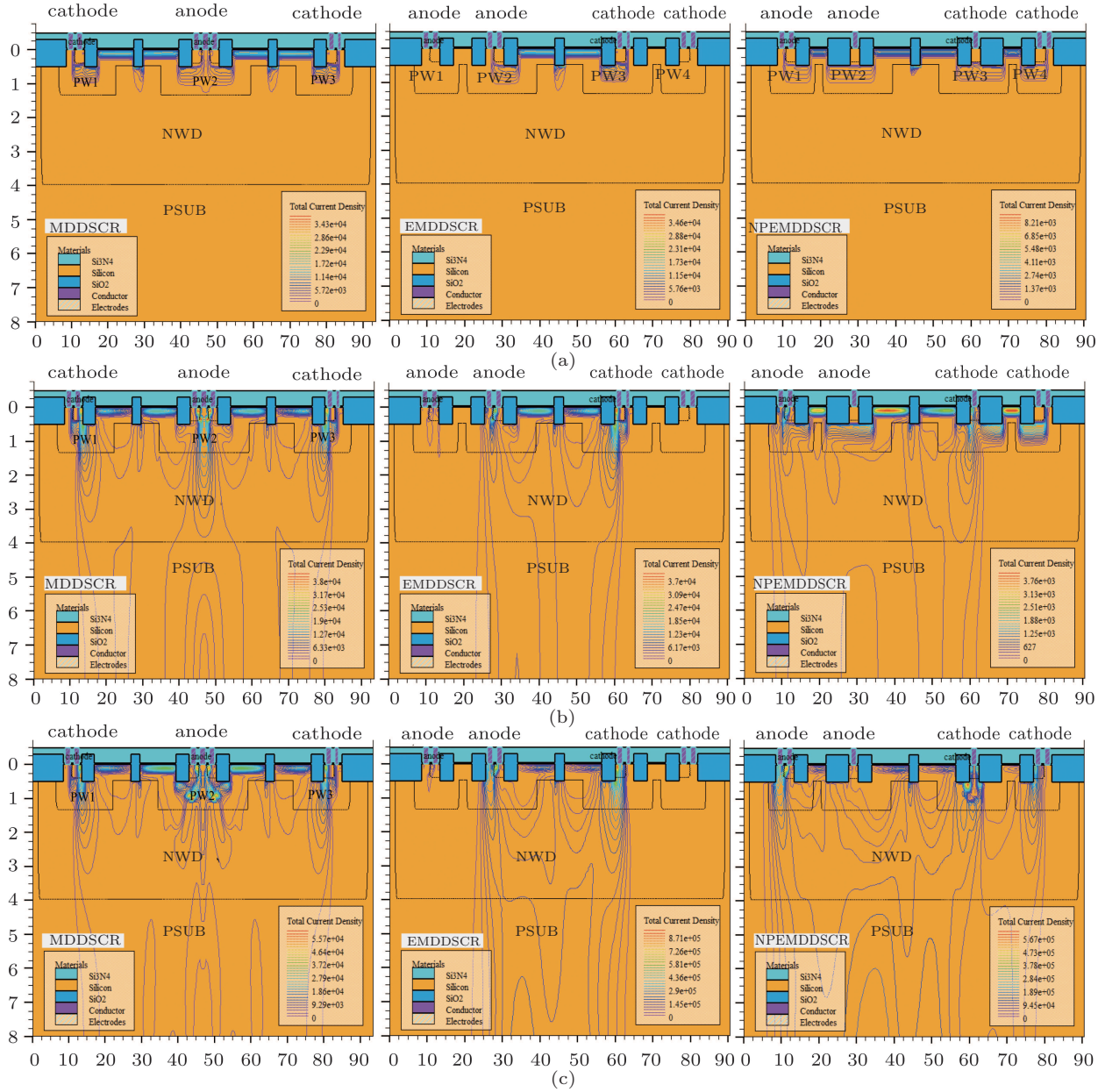


Fig. 4. Total current-flow-line at (a) the trigger point, (b) the holding point, and (c) the high ESD current pulse. In the legends of the figure, Si_3N_4 and SiO_2 symbolize Si_3N_4 and SiO_2 respectively. Number 3.43e + 04 equals to 3.43×10^4.

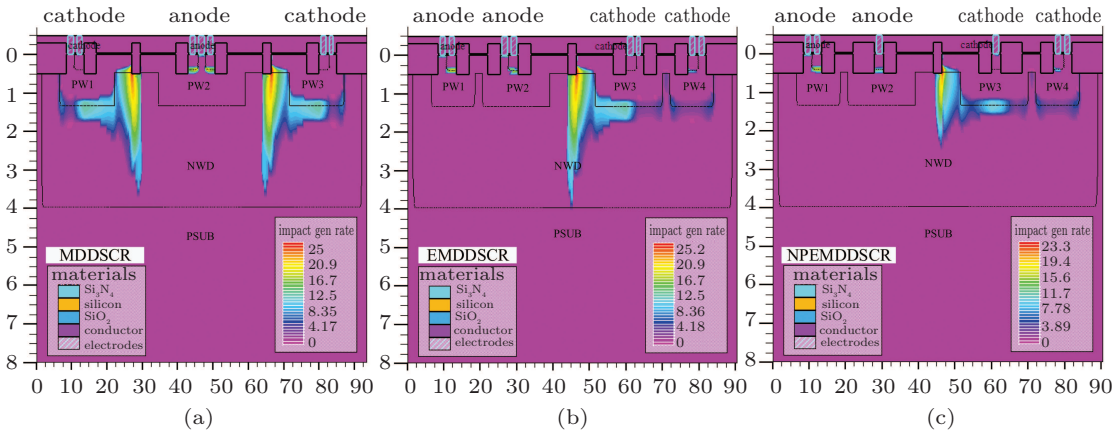


Fig. 5. Impact ionization of (a) MDDSCR, (b) EMDDSCR, and (c) NPEMDDSCR.

4. Experimental results

The MDDSCR, EMDDSCR, and NPEMDDSCR are fabricated in a 0.5-μm CDMOS process The finger width for each of these structures is 80 μm, and total width is 160 μm with two fingers. Those devices are designed to protect I/O pins for 12 V or have similar applications. The working voltage is in a range from −12 V to +12 V. Therefore, using the TLP test, the leakage current is measured at a voltage of 13.2 V (1.1 times the operating voltage). The applied pulse has a rising time of 10 ns and a pulse width of 100 ns.

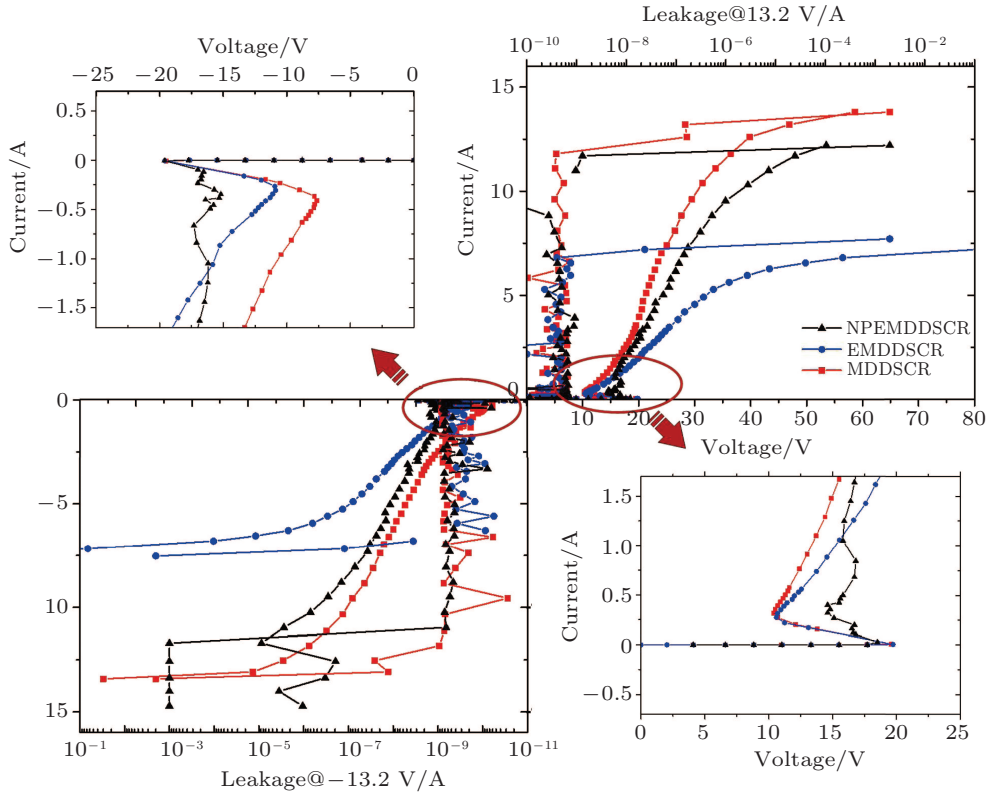


Fig. 6. Comparisons of TLP characteristic among MDDSCR, EMDDSCR, and NPEMDDSCR.

Figure 6 shows the reverse *I*–*V* characteristics of the MDDSCR, EMDDSCR, and NPEMDDSCR. Table 1 gives the detailed protection parameter values including HBM (Human Body Model) level, where the HBM is 1.5 times It2. According to the TLP measurement results, as the breakdown junctions are consistent, the trigger voltages are also about 19 V very consistently. Their differences are mainly reflected in holding voltage and failure current. The positive and negative holding voltage of MDDSCR are 10.40 V and 7.62 V, respectively. It shows the asymmetry of positive and nega-

tive *I*–*V* characteristics because it shares an anode and there are only one anode and two cathodes. The area of the anode emitter is relatively small, so the emitter injection efficiency is low. Therefore, the forward holding voltage is higher than the reverse holding voltage. The EMDDSCR has a positive and negative holding voltage of 10.50 V and 10.88 V respectively. Although it has similar positive and negative holding voltage, its failure current is only about 6 A, almost half of the value for MDDSCR. Obviously, because the outer finger does not turn on, the device only shows the discharge capacity of a single finger. This is also consistent with the simulation result. In contrast, the NPEMDDSCR has a forward holding voltage of 14.6 V and reverse holding voltage of 15.19 V. Not only are the positive and negative characteristics more symmetrical, but also the holding voltage is higher than the two above-memtioned cases This is because the current path of inner finger from the anode to cathode is longer than that of EMDDSCR, therefore making theNPEMDDSCR suitable for the 12-V application ESD design window. At the same time, the forward and reverse failure current can also reach 11.70 A and 10.96 A, respectively, similar to the scenario of MDDSCR, because both the internal finger and external finger can discharge current It is worth noting that the phenomenon of double snapbacks in the NPEMDDSCR's TLP curves is obvious. Corresponding to the simulated current density diagram, it can be seen that the first snapback represents the turn-on of the inner finger, and then the parasitic NPN on the outer finger is triggered. This NPN and parasitic PNP form the SCR path on the outer finger corresponding to the second snapback.

Table 1. TLP data for MDDSCR, EMDDSCR, and NPEMDDSCR.

Device name	Forward/reverse	VBD/V	Vt1/V	Vh/V	It2/A	HBM/kV
MDDSCR	forward	17	19.60	10.40	11.80	17.7
	reverse	17	19.50	7.63	13.07	19.6
EMDDSCR	forward	17	19.74	10.60	6.81	10.2
	reverse	17	19.61	10.88	6.55	9.8
NPEMDDSCR	forward	17	18.50	14.60	11.70	17.6
	reverse	17	19.60	15.19	10.96	16.4

5. Conclusions

An improved ESD protection device called the NPEMDDSCR is proposed, tested, and analyzed in this paper. Meanwhile, the ESD characteristics of the MDDSCR, EMDDSCR, and NPEMDDSCR are compared by TCAD simulation and TLP test curves. Compared with the MDDSCR, the NPEMDDSCR has symmetrical *I*–*V* characteristic curves and increases the holding voltage by more than 40%. Compared with the EMDDSCR, the NPEMDDSCR increases positive and negative failure currents by 71.8% and 67.3%, respectively. It can effectively solve the problem of uneven conduction to improve the overall robustness of the device. The improved embedded structure provides a good solution to the 12-V applications in 0.5-μm CDMOS process.

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