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Enhanced gated-diode-triggered silicon-controlled rectifier for robust electrostatic discharge (ESD) protection applications*

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A robust electron device called the enhanced gated-diode-triggered silicon-controlled rectifier (EGDTSCR) for electrostatic discharge (ESD) protection applications has been proposed and implemented in a 0.18-μm 5-V/24-V BCD process. The proposed EGDTSCR is constructed by adding two gated diodes into a conventional ESD device called the modified lateral silicon-controlled rectifier (MLSCR). With the shunting effect of the surface gated diode path, the proposed EGDTSCR, with a width of 50 μm, exhibits a higher failure current (*i.e.*, 3.82 A) as well as a higher holding voltage (*i.e.*, 10.21 V) than the MLSCR.

Keywords: electrostatic discharge (ESD), enhanced gated-diode-triggered silicon-controlled rectifier (EGDTSCR), modified lateral silicon-controlled rectifier (MLSCR), failure current, holding voltage

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1. Introduction

With the scale shrinking of integrated circuits, electrostatic discharge (ESD) has become a key factor affecting the reliability of integrated circuits.[1] Currently, more than one third of chip damages are ESD related, thus a reliable and effective ESD protection design is urgently needed.

The design of ESD protection has many difficulties, such as satisfying the design window while expecting high robustness and small footprint. Traditional ESD protection devices such as GGNMOS, diode, NPN, and RC power clamp usually occupy substantial chip area.[2] To alleviate the silicon footprint consumption of the ESD protection of each I/O pin in integrated circuits, silicon-controlled rectifier (SCR) becomes the most attractive choice among various ESD protection devices because of its highest robustness and smallest footprint.[3] However, the inherent regenerative feedback mechanism of SCR results in a deep snapback with a relatively small holding voltage, posing a threat of latch-up.[4] In addition, the transient power consumption of the ESD device will be inevitably increased with the increase of holding voltage, resulting in a sharp degeneration in the ESD failure current (I_{t2}). Therefore, it is extremely difficult to increase the holding voltage while maintaining a sufficiently high failure current.

Many efforts have been devoted to increasing the holding voltage of SCR.[5–8] The simplest scheme is to enlarge the distance between the anode and cathode of SCR,[5] but such a method is inefficient and insufficient to achieve latch-up immunity. Stacking technique[6] and ring-resistance-triggered technique[7] can effectively increase the holding voltage of SCR and achieve latch-up immunity, but these designs need to occupy substantial chip area, which is inconsistent with the design intention of high area efficiency. Under the constraints of chip area, segmentation techniques are introduced to reduce emitter injection efficiency of SCR device and achieve relatively high holding voltages.[8–10] However, the segmentation topology may cause current crowding, resulting in a deterioration in the ESD robustness.[11] Moreover, none of the above methods can simultaneously increase the holding voltage while maintaining a high failure current (I_{t2}).

In this paper, a robust electron device called the enhanced gated-diode-triggered silicon-controlled rectifier (EGDTSCR) has been proposed. As will be shown later, the proposed EGDTSCR possesses highly desirable ESD performances of both high holding voltage and high robustness.

2. Proposed device structures

Figures 1(a) and 1(b) illustrate cross-sectional views of conventional MLSCR and the proposed EGDTSCR, respectively. As shown in Fig. 1(a), there is a P+ region bridged across the NW/PW junction in the conventional MLSCR, which can achieve a lower triggering voltage. In the proposed EGDTSCR, two gated diodes D1 (reversed biased) and D2 (forward biased) are inserted into the N-well and P-well of the traditional MLSCR device, respectively, which share the same

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P+ region that bridges across the NW/PW junction. It should be noted that the gates of the two gated diodes are connected to the bridged P+ region by metal, and the N+ region of the reverse gated diode D1 in NW is in a floating state. Moreover, the N+ region of forward gated diode D2 reuses with the N+ region at cathode of MLSCR.

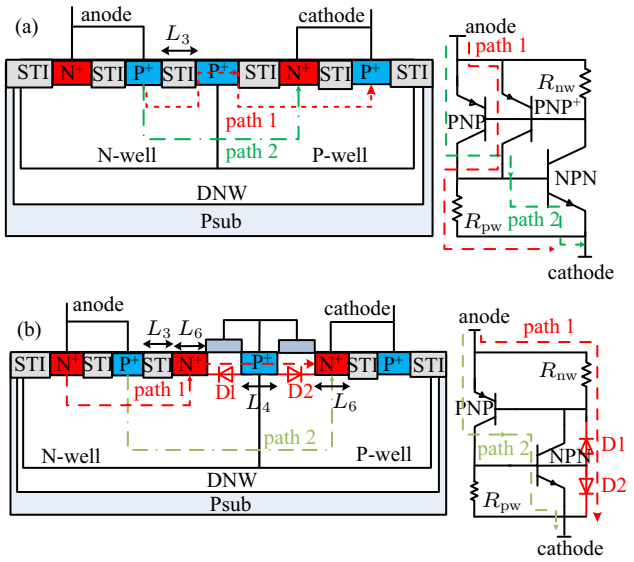


Fig. 1. Cross-sectional views of (a) conventional MLSCR and (b) the proposed EGDTSCR.

3. Operating mechanism

For the conventional MLSCR, the bridged P+ region has a higher doping concentration than PW, and the trigger voltage will be determined by NW/P+ junction, achieving a lower trigger voltage. During an ESD stress, the reverse-biased NW/P+ junction will first enter the avalanche breakdown state. Then the hole–electron pairs generated by the avalanche breakdown will turn on the parasitic lateral transistor NPN. When the voltage drop on NW exceeds 0.7 V, the parasitic transistors P+/NW/P+ and PNP will be triggered simultaneously.

Once the MLSCR is fired on, the parasitic PNP+ provides an additional shunt path, and part of the ESD current is discharged from the surface parasitic transistor P+/NW/P+ and PW (path 1), leading to a decrease in the ESD current flowing through the SCR path (path 2). That is, the additional ESD current path will break the positive feedback between the parasitic NPN and PNP. Hence, the holding voltage of MLSCR will be higher than that of traditional SCR.

The proposed EGDTSCR is constructed by adding two gated diodes D1 and D2 into the MLSCR, as shown in Fig. 1(b). When an ESD stress comes, the avalanche breakdown first occurs at the NW/P + junction, and the reverse gated diode D1 turns on immediately, thus the proposed EGDTSCR has a similar trigger voltage as the MLSCR. Then the ESD current is discharged through the reverse gated diode D1 and PW to the cathode, and the ESD current in NW will be converged at the floating N+ region, because the floating N+ region has a heavily doping concentration. Besides, the ESD current will apply a voltage to the gate of gated diodes D1 and D2 through the bridged P+ region, which will improve the current discharge capacity of the gated diode D1 on the one hand, and accelerate the conduction of the gated diode D2 on the other hand. For gated diode D1, the RC gate coupling effect formed by the gate capacitance and the P-well resistance helps to turn on the device. The increased VG further enhances the gate coupling effect, thereby improving the current discharge capacity of the gated diode D1.[12,13] As for gated diode D2, the polysilicon layer reduces current path length of gated diode D2, and allow for lower trigger and faster response time during stress without using additional trigger devices. The gate voltage VG accelerates such process, therefore, the gate voltage VG accelerates the conduction of the gated diode D2.[14,15]

Once the gated diode D2 is turned on, the surface gated diodes path (path 1) begins to discharge ESD current, and the parasitic transistor NPN will also be conducted. After the parasitic transistors NPN and PNP are turned on one after another, the SCR path (path 2) is ultimately triggered to discharge the main ESD current.

To further explore the physical mechanisms of the proposed EGDTSCR, non-isothermal technology computer-aided design (TCAD) simulation has been carried out by the Sentaurus tool, where the substrate of device was regarded as the only heat sink and the ambient temperature was set to 300 K. Doping dependence model, high-field saturation model, and PhuMob model are used as mobility degradation models. The SRH model, auger model, and Avalanche model were used as carrier generation & recombination model. Effective intrinsic density, thermodynamic models, and analyticTEP models are also used. The Poison equation, semiconductor transport equations, and electron/hole continuity equation are solved in simulation. The concentration of N+ and P+ implantations are both around 5×10^{20} cm^{-3}, and the average concentration of WELL is around 1×10^{16} cm^{-3}.

The TACD simulated current density distributions of proposed EGDTSCR under a positive ESD stress of the following points: (i) the triggering of the reverse gated diode D1, (ii) the triggering of parasitic NPN, and (iii) the triggering of SCR path are shown in Figs. 2(a), 2(b), and 2(c), respectively. In Fig. 2(a), after an avalanche breakdown occurs at the NW/P + junction, the reverse gated diode D1 has been turned on to discharge the ESD current. From Fig. 2(b), it can be seen that when the parasitic transistor NPN is turned on to discharge the ESD current, the surface gated diode path (path 1) also discharges the ESD current. At this time, there are two parasitic current paths in the device. In Fig. 2(c), after the parasitic transistors PNP is eventually turned on, the SCR path (path 2) begins to discharge the main ESD current.

The current density distribution of proposed EGDTSCR shows that the shunt path in the device has changed. Due to the higher doping concentration of floating N+ region, the parasitic PNP$^+$ path cannot be formed in the EGDTSCR, thus the surface gated diode path in the EGDTSCR substitutes the PNP$^+$ path in the MLSCR as the main shunt path. Besides, the ESD current discharge capacity of gated diode is stronger than that of PNP$^+$, so more ESD current is discharged from the surface gated diode path, which further weakens the positive feedback between the parasitic NPN and PNP in the SCR path, thereby the proposed EGDTSCR achieves a higher holding voltage than that of MLSCR.

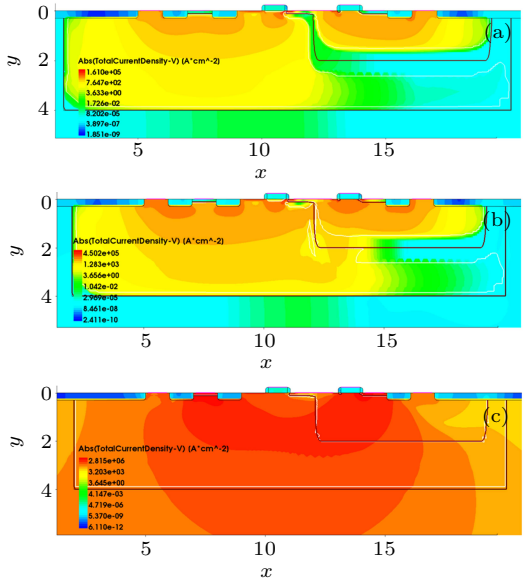


Fig. 2. The current density distributions of EGDTSCR under a 2A-TLP stress at (a) the triggering of the reverse gated diode D1, (b) the triggering of parasitic NPN, and (c) the triggering of SCR path.

Figure 3 shows the current density distribution of the MLSCR device with same dimension of EGDTSCR after triggering under a 2A-TLP stress. TCAD simulation shows that the current density in MLSCR is significantly lower than that in EGDTSCR under the same ESD stress. In MLSCR, the ESD current is mainly discharged through the parasitic SCR path, and the proportion of ESD current discharged through the surface parasitic PNP+ path is small, while the ESD current discharge capability of the gated diode path in EGDTSCR is stronger than that of the parasitic PNP+ path, and more ESD current is discharged from the surface gated diode path, which weakens the positive feedback between parasitic transistor NPN and PNP. Therefore, the proposed EGDTSCR achieves a higher holding voltage.

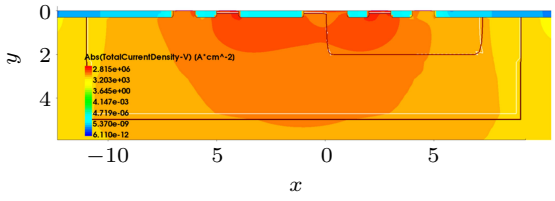


Fig. 3. TCAD simulated current density distributions of the MLSCR after triggering under a 2A-TLP stress.

4. TLP measurements and discussion

The ESD characteristics of the proposed EGDTSCR and conventional MLSCR were measured by a transmission Line Pulse (TLP) system with 10-ns rise time and 100-ns pulse width, and failure criterion is set to hundred times shift in leakage current. Measured TLP *I*–*V* curves and leakage currents are shown in Fig. 4. Both devices are implemented and verified in a 0.18-μm 5-V/24-V BCD process with a finger width of 50 μm. TLP results show that both devices have a similar trigger voltage of approximately 16 V, relaying on the avalanche breakdown of the NW/P+ junction. Besides, the EGDTSCR exhibits a holding voltage of 6.76 V and MLSCR has a holding voltage of 4.31 V. The lateral dimension of EGDTSCR is slightly larger than that of MLSCR by 2 μm due to the insertion of floating N+ region. The lateral dimension can indeed affect the holding voltage of EGDTSCR because it affects the length of the parasitic SCR path. However, the holding voltage of SCR devices are insensitive to the variation of lateral dimension.[4,10] Therefore, the lateral dimension increase of 2 μm is not the main reason for the increase in the holding voltage of EGDTSCR. In the proposed EGDTSCR, the ESD current discharge capacity of the surface gated diode is stronger than that of the parasitic PNP$^+$ in MLSCR, which is the main reason for that the EGDTSCR can achieve a higher holding voltage than the MLSCR. Moreover, the proposed EGDTSCR achieved a failure current I_{t2} of 3.08 A, which is much higher than the failure current of MLSCR (*i.e.* 2.26 A), with an increase of 36.3%. This can be attributed to the shunting effect of the surface gated diode path. As shown in Fig. 5, the impact ionization of EGDTSCR after the triggering of SCR path illustrates the impact ionization area extends from the NW/P$^+$ junction to the channel region of gated diode D1, which makes the current distribution in EGDTSCR more uniform and alleviates the heat accumulation in the EGDTSCR. Therefore, the proposed EGDTSCR achieves a higher failure current (I_{t2}) and a smaller on-resistance (R_{on}) than those of MLSCR.

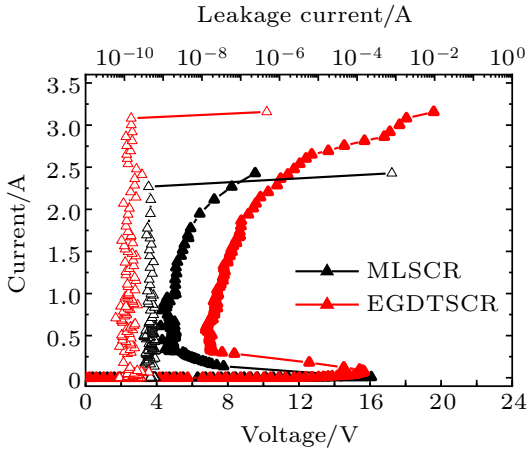


Fig. 4. Measured TLP *I*–*V* curves and leakage currents of the proposed EGDTSCR and MLSCR.

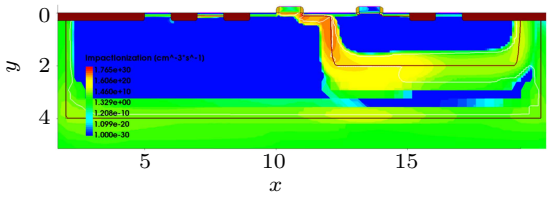


Fig. 5. The impact ionization of EGDTSCR after the triggering of SCR path.

Figure 6 illustrates the TLP *I*–*V* curves of proposed EGDTSCR with three different L_4 (defined as the width of the bridged P+ region). With the increase of L_4, the holding voltage of EGDTSCR has a similar modification to that of MLSCR, increasing obviously from 6.76 V to 10.21 V. At the same time, the failure current of EGDTSCR decreases from 3.08 A to 2.3 A. This is because the bridged P+ region is the common active region of the two gated diodes. As the holding voltage increases with the increase of L_4, it also increases the heat accumulation at the bridged P+ region, resulting in a decrease in the failure current (I_{t2}).

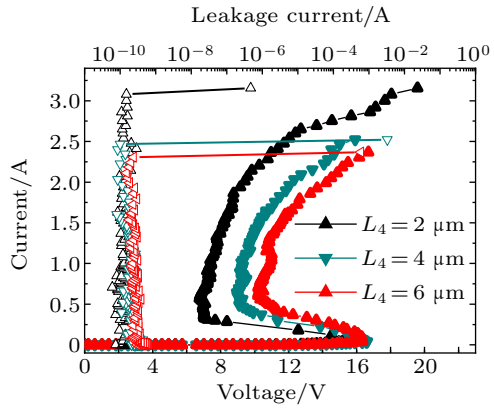


Fig. 6. TLP *I*–*V* curves and leakage currents of proposed EGDTSCR with three different L_4.

Figure 7 shows the *I*–*V* curves of EGDTSCR with three different L_6 (L_6 represents the width of the N-type region of the gated diode), and key ESD parameters are also extracted and listed in Table 1. With the increase of L_6, the holding voltage of EGDTSCR increases, and L_6 has a greater influence on the ESD performance than L_4. The failure current (I_{t2}) is significantly increased, and the on-resistance (R_{on}) is also prominently reduced at high currents with the increase of L_6. When L_6 is increased from 1 μm to 2 μm, the holding voltage (V_h) is increased from 6.76 V to 7.69 V, the failure current (I_{t2}) is increased by 21%, and R_{on} is decreased by 20.66%. When L_6 is increased from 2 μm to 4 μm, the holding voltage (V_h) is increased from 7.69 V to 10.67 V, and R_{on} is decreased by a further 84.6% from 10.036 Ω plunged to 1.548 Ω, and V_{t2} is decreased from 23.01 V to 16.08 V. This is because the increase of L_6 enhances the current conduction capacity of the gated diodes, and more ESD current is shunted from the floating N+ region, then discharged from the surface gated diode path (path 1), which effectively improves the holding voltage of EGDTSCR. At the same time, the increase of L_6 has less heat accumulation at the bridged P+ region than L_4, as shown in Fig. 5. In addition, the N+ region of the forward gated diode D2 is also the cathode N+ terminal of EGDTSCR. Increasing the width of the N+ terminal can effectively suppress the current saturation effect[10] while increasing conduction capability of the gate diode, which further increases the failure current (I_{t2}). Therefore, the holding voltage and failure current of the proposed EGDTSCR can be increased simultaneously.

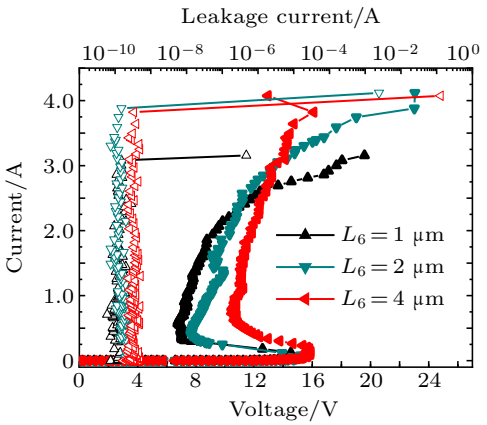


Fig. 7. TLP *I*–*V* curves and leakage currents of the proposed EGDTSCR with three different L_6.

Table 1. Key ESD parameters of MLSCR and proposed EGDTSCR with three different L_6.

Device	L_4/μm	L_6/μm	V_h/V	I_{t2}/A
MLSCR	2	–	4.31	2.26
EGDTSCR_1	2	1	6.76	3.08
EGDTSCR_2	2	2	7.69	3.88
EGDTSCR_3	2	4	10.47	3.82

5. Conclusion

A robust electron device called the enhanced gated-diode-triggered silicon-controlled rectifier (EGDTSCR) with substantially improved holding voltage and failure current has been proposed for electrostatic discharge (ESD) protection applications. The proposed device was built by adding two gated diodes into a conventional MLSCR device and was verified in a 0.18-μm 5V/24V BCD process. Measured TLP results illustrated that the proposed EGDTSCR could offer both higher holding voltage and higher ESD robustness than the conventional MLSCR. As such, the proposed EGDTSCR is an excellent choice for constructing ESD protection solutions for high-voltage integrated circuits.

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