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HuiFang Xu(许会芳), Xin-Feng Han(韩新风), Wen Sun(孙雯)

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Design and investigation of dopingless double-gate line tunneling transistor: Analog performance, linearity, and harmonic distortion analysis*

Hui-Fang Xu(许会芳)†, Xin-Feng Han(韩新风), and Wen Sun(孙雯)

Institute of Electrical and Electronic Engineering, Anhui Science and Technology University, Fengyang 233100, *China*

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The tunnel field-effect transistor (TFET) is proposed by using the advantages of dopingless and line-tunneling technology. The line tunneling is created due to the fact that the gate electric field is aligned with the tunneling direction, which dramatically enhances tunneling area and tunneling current. Moreover, the effects of the structure parameters such as the length between top gate and source electrode, the length between top gate and drain electrode, the distance between bottom gate and drain electrode, and the metal position on the on-state current, electric field and energy band are investigated and optimized. In addition, analog/radio-frequency performance and linearity characteristics are studied. All results demonstrate that the proposed device not only enhances the on/of current ratio and reduces the subthreshold swing, but also offers eight times improvement in cut-off frequency and gain band product as compared with the conventional point tunneling dopingless TFET, at the same time; it shows better linearity and small distortions. This proposed device greatly enhances the potential of applications in dopingless TFET.

Keywords: dopingless tunnel field effect transistor, line tunneling, linearity parameters

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1. Introduction

With the rapid increase of integration degree in integrated circuits and the continuous decrease of device size, the metal–oxide–semiconductor field effect transistor (MOSFET) gradually approaches to the physical limit. Since the downscaling of MOSFET greatly challenges the power consumption due to large leakage currents. It is very necessary to provide low power consumption and high switching speed devices, especially since we are now entering into the era of Internet of Things (IoT). Moreover, as far as the conventional MOSFET is concerned, it has a limited subthreshold swing (*SS*) due to its thermionic emission operation mechanism.[1] One way to solve the issue of MOSFET is to develop alternative devices. The tunnel field effect transistor (TFET) is in line with the trend of the shrinking of devices in circuit, chip level and ultra-low power consumption applications, since it has many advantages such as lower *SS*, lower off-state current ($I_{\rm off}$),[2–4] and lower supply voltage,[5,6] simultaneously, higher immunity against short-channel effects (SCEs). However, the TFET has some disadvantages such as low on-state current ($I_{\rm on}$) due to its tunneling inefficiency as well as ambipolar characteristics as compared with MOSFET. For better application from the perspective of circuit design, $I_{\rm on}$ should be enhanced greatly and the ambipolar behavior should be suppressed effectively, simultaneously, the fabrication process of doped source and drain regions for TFET should be simple and feasible. Therefore, tremendous efforts using optimizations of TFET from the process to material and structure engineering have been extensively made to improve the performances. Researchers have proposed many techniques for enhancing $I_{\rm on}$, such as hetero-structures with low bandgap material in the tunneling region,[7–9] gate-oxide layer dielectric engineering,[10] dual-material gate engineering,[11–13] innovative device architecture,[14–18] carrier tunneling in-line with gate field, *etc*. Hetero-oxide layer dielectric, lightly doped drain,[19] and gatedrain underlap structure[20,21] have been provided to solve the ambipolar current ($I_{\rm amb}$) issue. In order to obtain a fabrication advantage, the dopingless (or uniform) fabrication process is established based on the charge-plasma (CP) technique.[22–24] The CP technique is a high-temperature process that makes the source and drain metal electrodes with appropriate work functions create the doped source/drain region. It is easy to see that CP technique not only avoids random dopant fluctuations but also reduces the complex thermal budget, and at the same time that the abrupt junction can be easily formed in the region between the source and channel and also in the region between the drain and channel.

However, as far as the conventional silicon-based point tunneling dopingless TFET (PT_DLTFET) is concerned, on the one hand, large electron effective mass of silicon material and large tunneling barrier width in the tunneling region will reduce $I_{\rm on}$; on the other hand, $I_{\rm on}$ is low due to the fact that

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†Corresponding author. E-mail: xu0342@163.com

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the tunneling of carriers takes place in a small area at a surface near the source–channel junction along the gate length direction, and the bandtoband tunneling (BTBT) is independent of the tunnel cross-sectional area. Recently, I_{on} issue of PT_TFET has been mitigated by using line tunneling TFET (LT_TFET) to a certain extent.[25–28] Unlike the PT_TFET, the LT_TFET involves BTBT orthogonal to the gate length, so the BTBT is dependent on the tunnel cross-sectional area. In other words, relatively high BTBT can be achieved for LT_TFET due to an increased tunnel cross-sectional area, providing I_{on} is higher. Therefore, recently, on-chip implementation of LT_TFET based direct current (DC) and analog/radio frequency (RF) performance analysis has increased the interest of the research community. Tripuresh *et al.*[29] proposed an extended-source double-gate TFET (ESDG-TFET) in order to improve DC and analog/RF performance. The ESDG-TFET provides a threshold voltage of 0.42 V, an *SS* of 12.24 mV/decade, on-off current ratio (I_{on}/I_{off}) of 2.57×10^{12}, and a cutoff frequency (f_t) of 37.7 GHz. Prabhat *et al.*[30] reported T-shaped III–V heterojunction TFET with a larger tunneling area, which results in a 4.3-times improvement in I_{on}, a 4 times improvement in the transconductance (g_m), and a 2.36-times improvement in f_t as compared with the LTFET.

Li *et al.*[31] has reported a germanium-based line tunneling dopingless TFET (named LT_DLTFET), which integrates the benefits of CP technique and line tunneling together. But LT_DLTFET in the reported paper uses the same oxide, *i.e.* HfO_2, it will increase I_{off} and *SS*. For improving the performance of LT_DLTFET, a novel device (named M_LT_DLTFET) is proposed in this paper. A metal with an appropriate work function is implanted into the top-gate oxide layer for M_LT_DLTFET. Moreover, the different oxide layers are used in the M_LT_DLTFET in order to enhance the device performance, in which the HfO_2 dielectric provides greater electric field in the tunneling region for obtaining larger I_{on}, and SiO_2 can suppress I_{amb}. We intend to improve the DC, analog/RF performance, and linearity performance of the proposed device as compared with those of PT_DLTFET and LT_DLTFET.

2. Device structure

The structures of PT_DLTFET, LT_DLTFET, and M_LT_DLTFET are shown in Fig. 1. The above-mentioned devices are designed by using CP technique, where specific work functions of source electrode and drain electrode are 5.9 eV (platinum) and 3.9 eV (hafnium) respectively in order to induce the P+ doping and N+ doping in the source region and drain region. The doping concentration of the intrinsic region is 10^{15} cm^3. The width and height of metal layer for M_LT_DLTFET are denoted by L_M and T_M, respectively, as described in Fig. 1(c). The top gate and bottom gate have the same bias and work function for PT_ DLTFET, but for LT_DLTFET and M_LT_DLTFET as shown in Figs. 1(b) and 1(c), their bottom gates each are grounded and have a higher work function, while their top gates each have a higher bias and a lower work function. Moreover, the distance between bottom gate and drain electrode of PT_DLTFET is lower than those of the other devices. The structure of M_LT_DLTFET is the same as that of LT_DLTFET, but a metal with an appropriate work function is implanted into the top-gate oxide layer for M_LT_DLTFET. The material parameters and dimensions of the devices are given in Table 1.

Table 1. Material parameters and dimensions of devices.

Parameter	Symbol	PT_DLTFET	LT_DLTFET	M_LT_DLTFET
Top gate length	L_{TG}	55 nm	55 nm	55 nm
Bottom gate length	L_{BG}	55 nm	50 nm	50 nm
Source length	L_S	20 nm	20 nm	20 nm
Drain length	L_D	20 nm	20 nm	20 nm
Distance between top gate and source electrode	L_{TGS}	5 nm	5 nm	5 nm
Distance between top gate and drain electrode	L_{TGD}	10 nm	10 nm	10 nm
Distance between bottom gate and drain electrode	L_{BGD}	10 nm	20 nm	20 nm
Oxide layer thickness	T_{OX}	3 nm	3 nm	3 nm
Ge body thickness	T_{Ge}	10 nm	10 nm	10 nm
Top gate work function	WK_{TG}	4.2 eV	3.9 eV	3.9 eV
Bottom gate work function	WK_{BG}	4.2 eV	4.6 eV	4.6 eV
Metal work function	WK_M			3.9 eV
Source electrode work function	WK_S	5.9 eV	5.9 eV	5.9 eV
Drain electrode work function	WK_D	3.9 eV	3.9 eV	3.9 eV

The simulations are performed by using silvaco atlas simulator,[32] and the following models such as dynamic nonlocal band-to-band tunneling model, shockley-read-hall model, auger recombination model, and fermi statistics model are used in this work. The values of I_{on}, I_{off}, and I_{amb} defined at $V_{gs} = 1$ V, 0 V, and -0.5 V respectively are calculated with keeping V_{ds} fixed at 0.5 V. Here, V_{gs} and V_{ds} denote the gate–source voltage and drain–source voltage, respec-

tively. Moreover, the bottom–gate voltages of LT_DLTFET and M_LT_DLTFET are both defined as zero when these devices are operated.

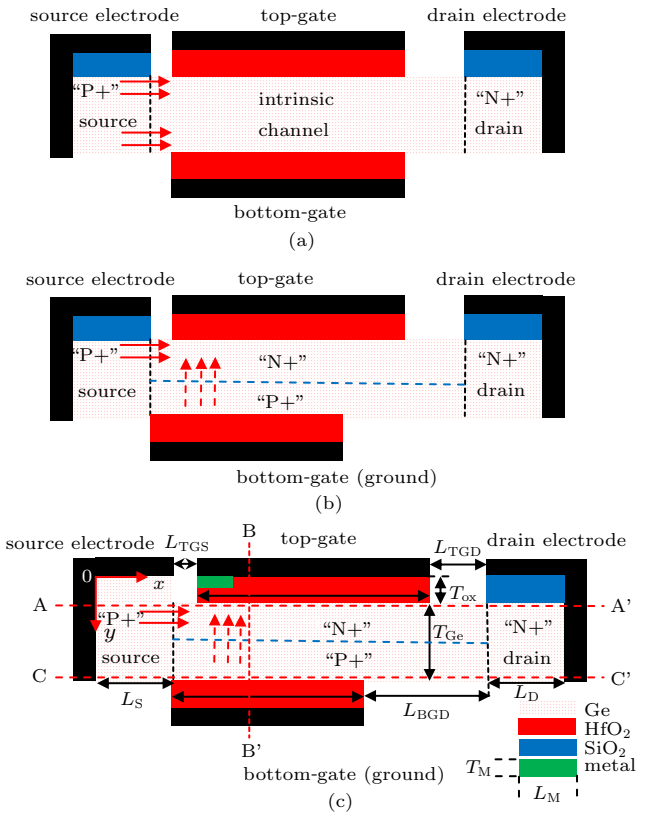


Fig. 1. Structure of devices of (a) PT_DLTFET, (b) LT_DLTFET, and (c) M_LT_DLTFET.

3. Results and discussion

In this section, DC performance, analog/RF characteristic, and linearity analysis for PT_DLTFET, LT_DLTFET, and M_LT_DLTFET are analyzed.

3.1. DC characteristics analysis

The energy bands along the cutline (A–A') and (B–B') for M_LT_DLTFET under on-state condition are shown in Figs. 2(a) and 2(b), respectively. Along the A–A' direction, it can be found that the barrier width of the proposed device is very small, so it satisfies the band-band tunneling condition, and the tunnel is defined as e-point tunnel in this condition. Moreover, a higher work function of bottom-gate makes the energy band at the bottom of the channel pulled up. Simultaneously, a lower work function of top-gate makes the energy band at the top of the channel pulled down. The energy band in the channel is bent, and thus leading the valence band to be aligned with the conduction band as observed in Fig. 2(b). In M_LT_DLTFET, the bottom channel accumulates holes because of grounded bottom gate with a higher work function. The top channel accumulates a lot of electrons due to the top gate possessing a lower work function and higher bias. Electron and hole concentration along the B–B' direction under on-state condition is shown in Fig. 2(c). Moreover, the higher the WK_{BG} the more the holes accumulated at the bottom channel will be. Thus, a pseudo abrupt PN junction is created in the channel region, which induces the tunneling from channel bottom to channel top, and the tunnel is defined as e-line tunnel in this condition. This e-line tunnel can also be proved by the

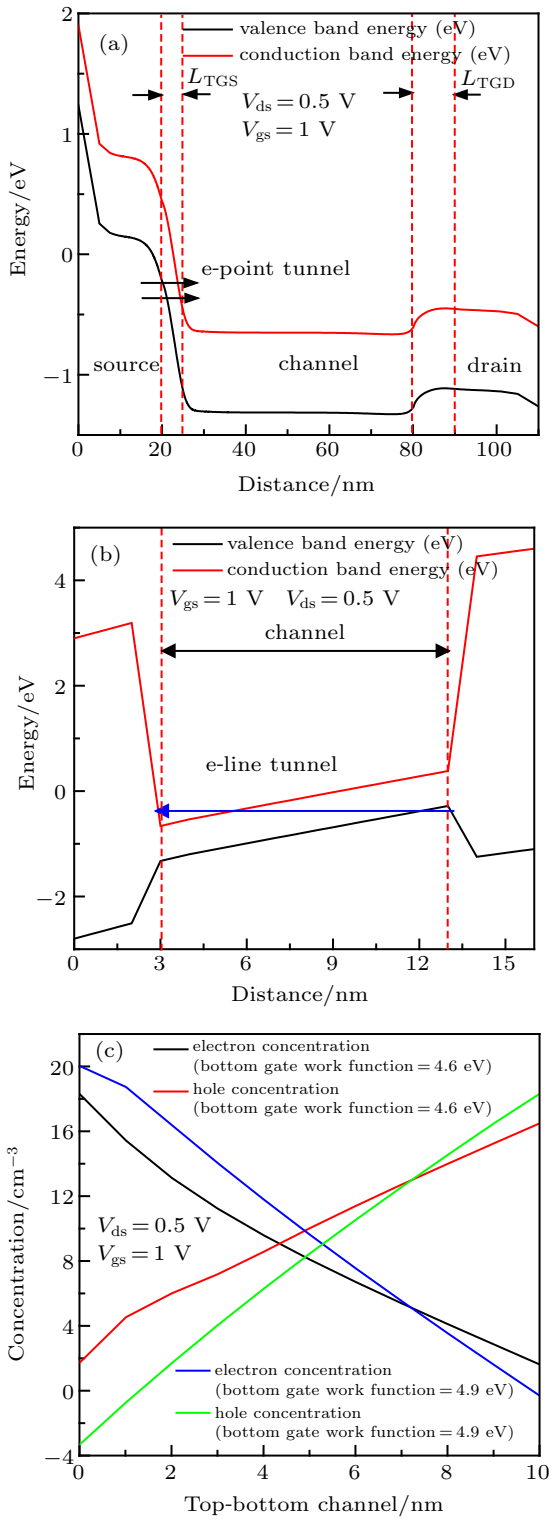


Fig. 2. Plot of energy varying with distance for M_LT_DLTFET along (a) A–A' direction, and (b) B–B' direction under on-state condition, (c) plots of electron and hole concentrations varying with top-bottom distance along B–B' direction under on-state condition.

energy band in Fig. 2(b). Therefore, there are two tunneling paths in the proposed device as depicted in Fig. 1(c). It should be noted that this bottom gate engineering for LT_DLTFET and M_LT_DLTFET offers the line tunneling current, meanwhile, sacrificing half of point tunneling current.[31]

The electric field, electron current density, transfer characteristics, and extracted *SS* of the devices are shown in Fig. 3. Figure 3(a) shows that the M_LT_DLTFET can obtain an increased electric field along the cutline A–A' (as marked in Fig. 1(b)) at source/channel interface, which is instrumental in getting higher tunneling rate of charge carriers at the tunneling junction. Moreover, figure 3(b) shows the plots of electron current density *versus* distance along the cutline A–A' (as marked in Fig. 1(b)) for three devices under the on-state condition. Due to the use of metal at source/channel interface in M_LT_DLTFET for improving the electron tunneling rate in the region from source to channel, therefore, a much larger electron current density is obtained in the channel region and drain region for the proposed device than for other devices. Therefore, an increased electric field at the interface between the source and channel and larger electron current density in channel region will result in higher I_{on} than that of other structures as shown in Fig. 3(c). Moreover, I_{off} for the proposed device is almost the same as those of the other devices. Therefore, M_LT_DLTFET does surpass the other devices in terms of I_{on}, and I_{on}/I_{off}, as listed in Table 2. The threshold voltage (V_{th}) of M_LT_DLTFET is lower than those of the other devices because a metal with an appropriate work function implanted into the top-gate oxide layer leads to the gate dielectric to thin out, which will enhance the coupling between the gate and the source tunneling junction. Average *SS* (SS_{avg}) is defined as $(V_T - V_{off})/\log(I_T/I_{off})$, where V_T is extracted using the constant current (CC) method, and CC (I_T) is defined as 10^{-10} A/μm.[33] The *SS* is defined as $dV_{gs}/d\log I_{ds}$ and the minimum *SS* (SS_{min}) is defined $\left(dV_{gs}/d\log I_{ds}\right)_{min}$. Here a steeper SS_{avg} is obtained for the proposed device than for other devices because the M_LT_DLTFET can obtain a much enhanced tunnel probability due to the increase of electric field caused by the thinning of the gate dielectric. Therefore, the M_ LT_DLTFET will offer better switching characteristics. From Fig. 3(d), the M_LT_DLTFET has achieved a sub-60 mV/decade *SS* for over five orders of magnitude of the drain current. Consequently, in addition to large I_{on} and I_{on}/I_{off}, the M_LT_DLTFET also exhibits a low value of V_{th} and SS_{avg} as well as nearly constant *SS* in a large drain current range.

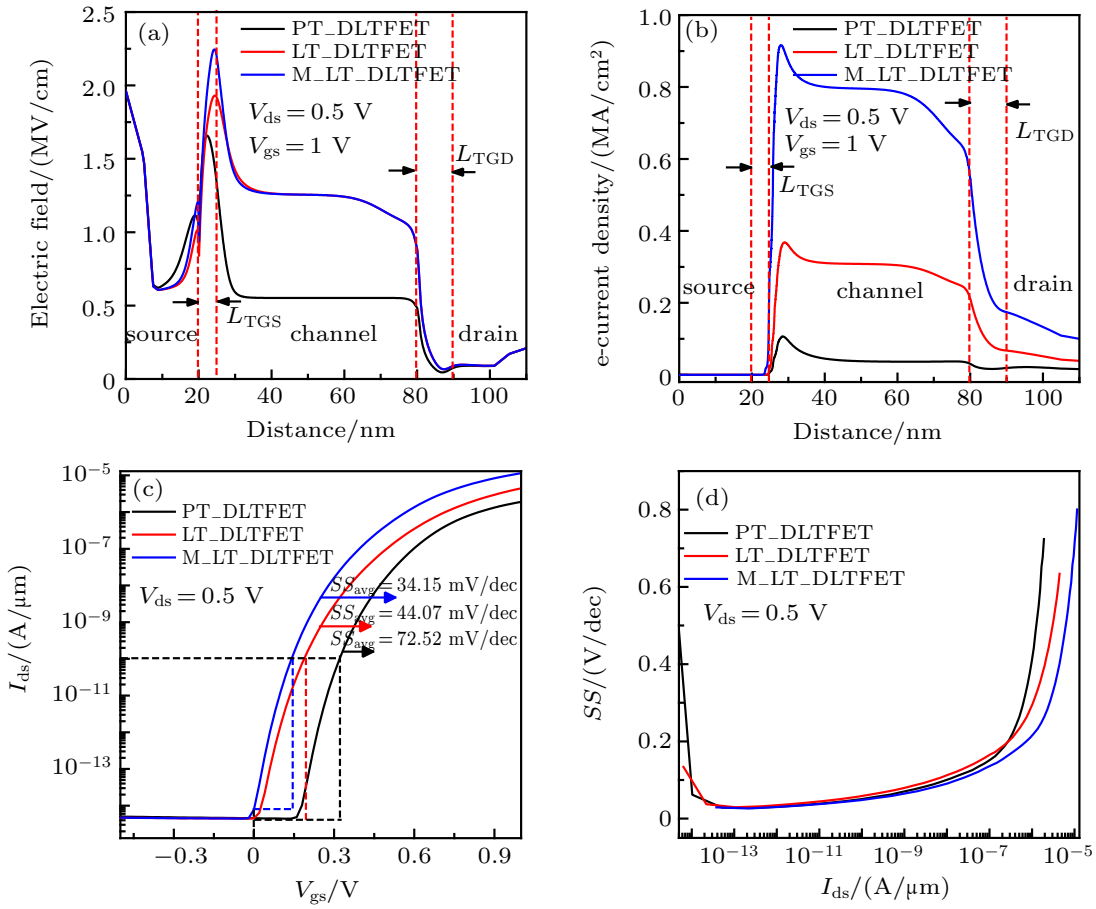


Fig. 3. (a) Electric field varying with distance along cutline A–A', (b) electron current density varying with distance along cutline A–A', (c) transfer characteristics, and (d) extracted *SS* varying with I_{ds} for the devices.

Table 2. Comparison of DC parameter among devices.

Parameter	PT_DLTFET	LT_DLTFET	M_LT_DLTFET
I_{on}/(A/μm)	1.90117×10^{-6}	4.44004×10^{-6}	1.14652×10^{-5}
I_{on}/I_{off}	4.19×10^{8}	9.81×10^{8}	1.48×10^{9}
I_{amb}/(A/μm)	5.01×10^{-15}	4.69×10^{-15}	4.67×10^{-15}
SS_{avg}/(mV/dec)	72.52	44.07	34.15
SS_{min}/(mV/dec)	27.47	29.36	26.23
V_{th}/V	0.34	0.2	0.16

3.2. Optimization of the proposed device

The proposed device with different parameters such as L_{TGS}, L_{TGD}, L_{BGD}, and metal position is explored to further improve the performances. The energy bands along the A–A' and B–B' direction for M_LT_DLTFET with different values of L_{TGS} and V_{gs} are shown in Fig. 4. It can be seen from Figs. 4(a) and 4(b) that L_{TGS} mainly affects the point tunneling barrier width (along the A–A' direction) between the source and channel region for M_LT_DLTFET operated at low and high V_{gs}, respectively. The smaller L_{TGS} is helpful in enhancing the point tunneling current. However, the line tunneling barrier width (along the B–B' direction) for M_LT_DLTFET operated at low or high V_{gs} is almost unaffected by L_{TGS}.

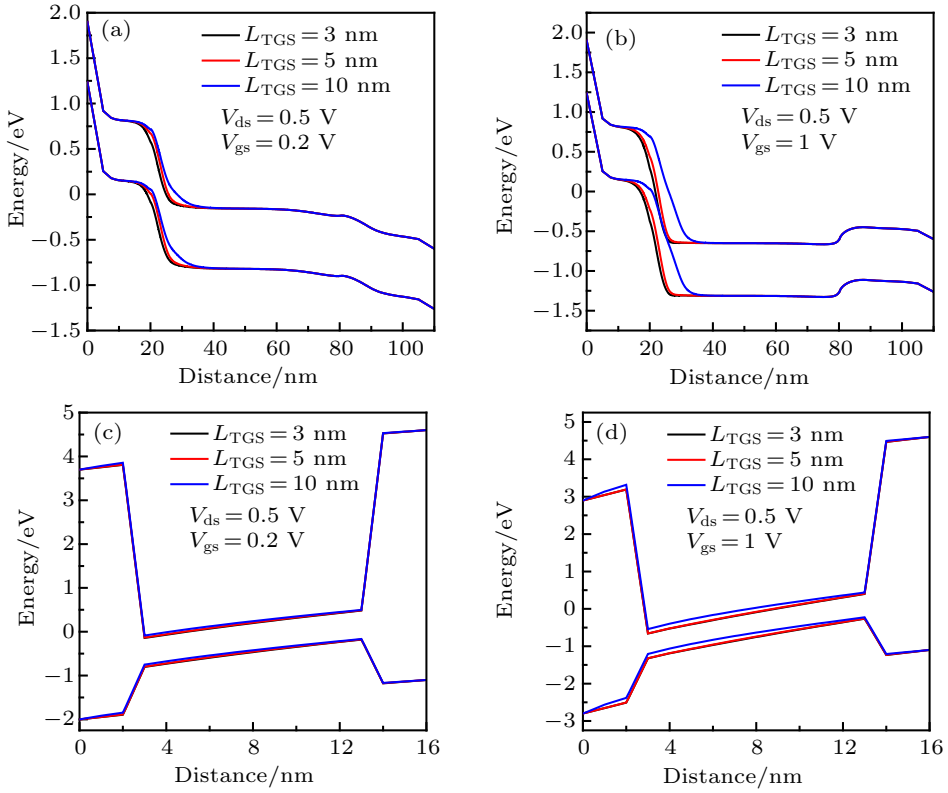


Fig. 4. Plots of energy varying with distance at different values of L_{TGS} (a) along cutline A–A' when V_{gs} is fixed at 0.2 V, (b) along cutline A–A' when V_{gs} is fixed at 1 V, (c) along cutline B–B' when V_{gs} is fixed at 0.2 V, and (d) along cutline B–B' when V_{gs} is fixed at 1 V.

Figure 5 shows the transfer characteristics and electric field *versus* distance along the cutline A–A' for M_LT_DLTFET with different values of L_{TGS} while metal position is kept unchanged. The off-state current is almost unaffected by L_{TGS}. On the one hand, the smaller L_{TGS} is helpful in enhancing the point tunneling current for M_LT_DLTFET as mentioned in Figs. 4(a) and 4(b). On the other hand, the smaller L_{TGS} will enhance the region of line tunneling between bottom-gate and top-gate, thereby increasing the on-state current. The on-state current for the proposed device with 5-nm L_{TGS} is slightly larger than that of the proposed device with 3 nm, which is due to the fact that the implementation of metal at the tunneling junction exploits larger electric field and sharper band bending in the maximum tunneling region, *i.e.* at the source corners, thereby making the tunneling width narrower. Therefore, the on-state current increases, and the optimal value of L_{TGS} is set to be 5 nm.

The transfer characteristics and energy band along the A–A' direction for the proposed device with different values of L_{TGD} are shown in Fig. 6. When L_{TGD} increases from 5 nm to 15 nm, the off-state current and on-state current are almost unaffected by L_{TGD}. However, the on-state current decreases

when L_{TGD} is 25 nm. It can be found from Fig. 6(b) that the barrier of energy band between channel and drain regions increases with the value of L_{TGD} increasing. The increasing barrier in the region between channel and drain will prevent electrons from flowing to the drain region, thereby reducing the drain current.

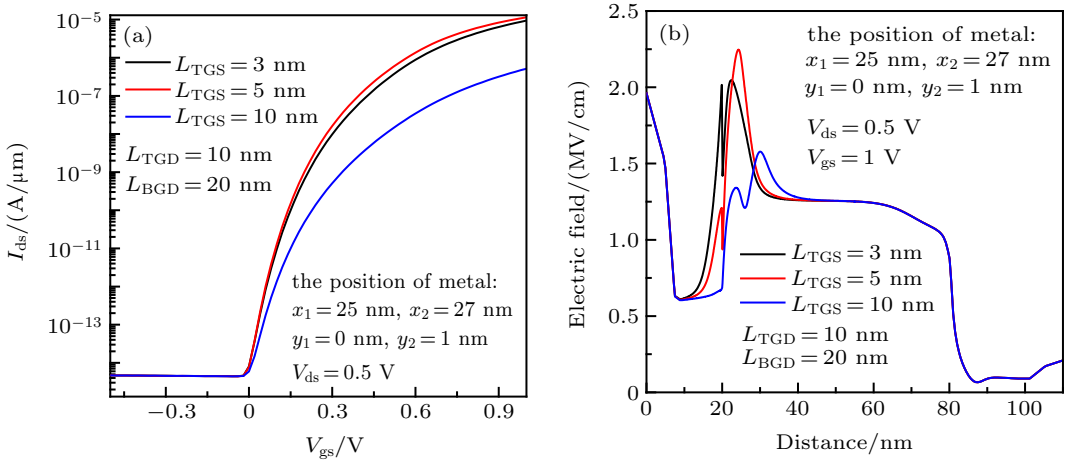


Fig. 5. (a) Transfer characteristics, and (b) electric fields varying with distance along A–A' direction for proposed device with different distances between source and top-gate electrode.

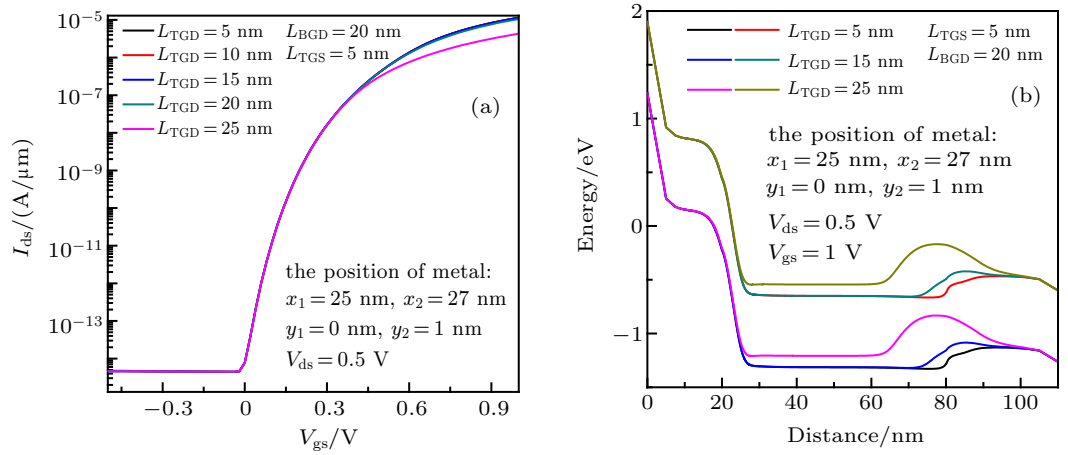


Fig. 6. (a) Transfer characteristics, and (b) energy varying with distance along A–A' direction for proposed device with different distances between top-gate and drain electrode.

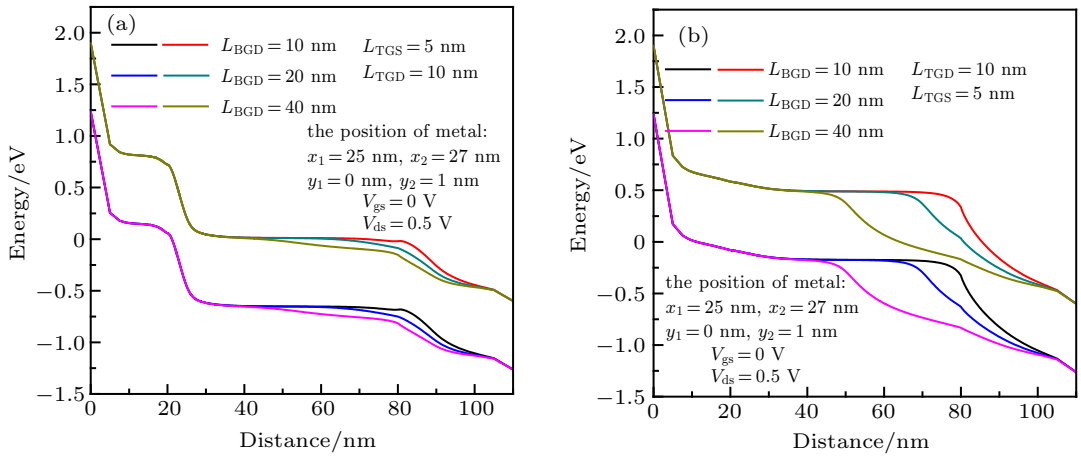


Fig. 7. Plots of energyvarying with distance along (a) A–A', and (b) C–C' direction for proposed device with different distances between bottom-gate and drain electrode.

The effects of varying L_{BGD} on energy band along the A–A' direction and the C–C' direction for the proposed device under the off-state condition are shown in Fig. 7. It is observed from the figure that when L_{BGD} decreases from 40 nm to 10 nm, the barrier width between channel and drain region also reduces, thus leading I_{off} to augment. Moreover, the tun-

neling junction at the bottom of channel is turned on (in the C–C' direction). Therefore, I_{off} is mainly generated by the tunneling current from the bottom of channel. Note that the region of line tunneling between bottom-gate and top-gate will decrease with L_{BGD} increasing, thereby reducing the on-state current. Therefore, the value of L_{BGD} is neither too large nor too small, so the optimal value of L_{BGD} for the proposed device is set to 20 nm.

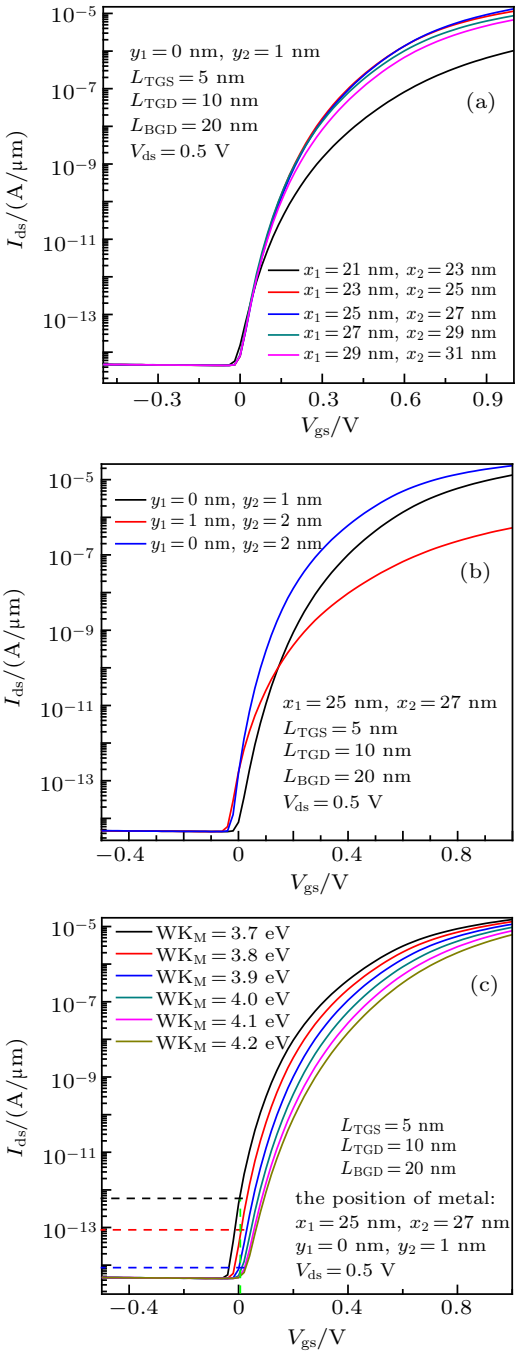


Fig. 8. Plots of I_{ds} *versus* V_{gs} for M_LT_DLTFET with metal at different positions along (a) x direction and (b) y direction, (c) for different work functions of metal.

Figures 8(a) and 8(b) show the plots of I_{ds} varying with V_{gs} of the proposed device at different metal positions. The position of metal will affect the electric field and tunneling width at the tunneling junction, so it results in the variation of I_{ds}. Consequently, for considering the characteristics of the proposed device, the parameters about x_1, x_2, y_1, and y_2 for the position of the metal are set to be 25 nm, 27 nm, 0 nm, and 1 nm, respectively. The plots of I_{ds} of the proposed device varying with V_{gs} for different work functions of metal (WK_M) are shown in Fig. 8(c). It is very clear that I_{on} and I_{off} increase with the decrease of WK_M. The improvement in I_{on} for lower value of WK_M can be explicated with the help of electric field variation in the maximum tunneling region, *i.e.* at the source corners. Therefore, the best work function of the metal ($WK_M = 3.9$ eV) is selected due to the fact that it achieves better performance in terms of I_{on} and I_{on}/I_{off}. All the structure parameters of M_LT_DLTFET are optimized to obtain an improvement in the DC characteristics.

3.3. Analog and radio-frequency performance analysis

This section is dedicated to the study of the analog and radio-frequency performance for the three devices. It is noteworthy that in the M_LT_DLTFET the optimized structure parameters are used in the following analysis. The transconductance (g_m) of the device is expressed as the slope of $\log(I_{ds}) - V_{gs}$ plot while V_{ds} is kept constant. Therefore, the value of g_m depends on I_{ds}. From Fig. 9(a), a larger g_m value for M_LT_DLTFET is achieved due to the fact that the variation of I_{ds} with V_{gs} is greater as shown in Fig. 3(c), which represents that the M_LT_DLTFET has higher sensitivity for converting V_{gs} into I_{ds}. The parasitic gate capacitance (C_{gd} and C_{gg}) is also an important indicator for improving the device characteristics, which has an important influence on the amplification ability of the analog circuits and switching frequency of the digital circuits. Figures 9(b) and 9(c) show the plots of C_{gd} and C_{gg} *versus* V_{gs} for the three devices.

Further, RF parameters relating to f_t, gain bandwidth product (GBP), and transconductance frequency product (TFP) for the three devices are analyzed. The parameter f_t defined as $g_m/[2\pi(C_{gd}+C_{gs})]$ is expressed as the frequency where short-circuit current gain is unity. The GBP defined as $g_m/(20\pi C_{gd})$ can be used to determine the maximum working frequency for a DC gain of 10. It can also be found that f_t and GBP of the three devices each reach a peak value. However, the value begins to decrease as V_{gs} increases due to the limitation of g_m caused by the mobility degradation and the increasing of the parasitic gate capacitance. The M_LT_DLTFET offers eight times improvement in f_t and GBP as compared with PT_DLTFET. Moreover, the M_LT_DLTFET offers four times improvement in f_t and GBP as compared with LT_DLTFET. High GBP illustrates larger gain as well as bandwidth, the increase in f_t results in small switching delay. The TFP defined as $g_{m*}f_t/I_{ds}$ is another important parameter to investigate the device characteristics for

high-speed design, and the TFP represents a trade-off between bandwidth and power. The TFP also increases for the three devices, and after attaining a maximum value it starts to decrease for higher V_{gs}. The results show that the M_LT_DLTFET has a better RF performance than the other devices as depicted in Fig. 10. Therefore, the proposed device has a better prospects for high-speed and high-frequency applications in the advanced integrated circuits.

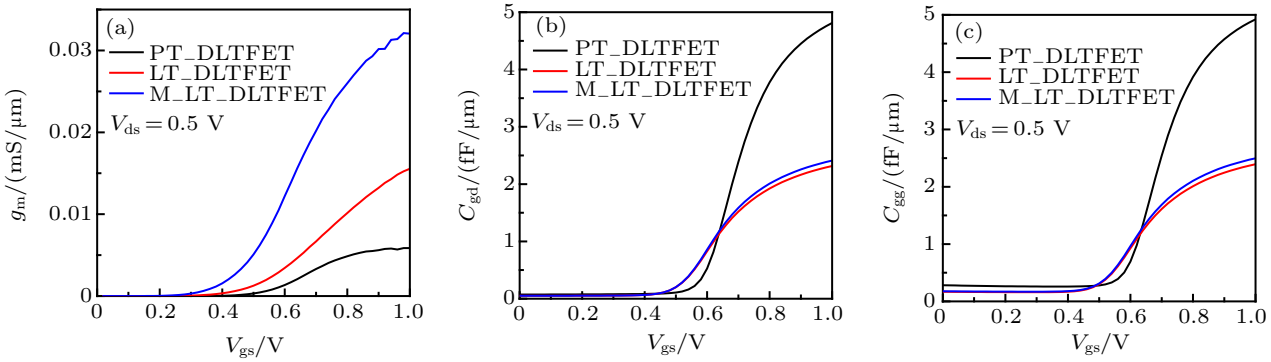


Fig. 9. Plots of (a) g_m, (b) C_{gd}, (c) C_{gg} *versus* V_{gs} for three devices.

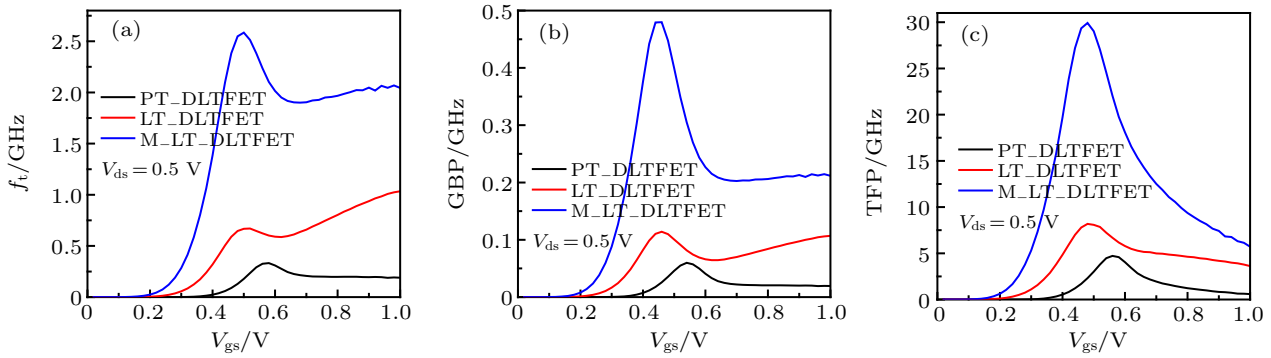


Fig. 10. RF parameters of (a) f_t, (b) GBP, and (c) TFP for three devices.

3.4. Linearity and distortion performance analysis

As is well known, the best linearity and minimum high-order harmonics are the criteria achievable for a device. If better linearity for the device is not obtained, nonlinear distortion happens to the output, thus the signal can be distorted . Therefore, it is necessary that the g_m value of the device should be constant over V_{gs} in order to obtain better linearity. However, g_m value of TFET and MOSFET vary with V_{gs}, which relates mainly to the transfer characteristics. Therefore, the linearity distortion parameters in terms of the second and third-order voltage intercept points (V_{IP2}, V_{IP3}), the third-order input interception point (IIP_3), and the third-order intermodulation distortion (IMD_3) for the three devices are analyzed for addressing the nonlinearity issue. The figure-of-merit parameters are calculated from the following equations:

$$V_{IP2} = 4 \times g_{m1}/g_{m2}, \tag{1}$$

$$V_{IP3} = \sqrt{24 \times g_{m1}/g_{m3}}, \tag{2}$$

$$IIP_3 = 2/3 \times g_{m1}/(g_{m3} \times R_S), \tag{3}$$

$$IMD_3 = \left(4.5 \times (V_{IP3})^3 \times g_{m3}\right)^2 \times R_S, \tag{4}$$

where $g_{mn} = 1/n! \times (\partial^n I_{ds}/\partial V_{gs}^n)$ are higher-order harmonics of transconductance, g_{m1} is the same as the afore-mentioned g_m, and R_S is usually set to be 50 Ω in most of RF applications. It can be seen from the above equation that g_{mn} is the main reason for producing distortion components in the device. Figure 11 shows the variations of g_{m2} and g_{m3} with V_{gs} for three devices. It is obvious from Fig. 11 that g_{m2} and g_{m3} for M_LT_DLTFET fluctuate greatly at higher V_{gs} due to the fact that g_m for M_LT_DLTFET varies obviously at higher V_{gs} as shown in Fig. 9(a).

The V_{IP2} and V_{IP3} indicate that the extrapolated input voltages that the first- and second (third-)-order harmonic voltages are equal. In order to obtain better linearity, it is important to make the values of V_{IP2} and V_{IP3} as high as possible. From Figs. 12(a) and 12(b), it can be inferred that the M_LT_DLTFET shows an improvement in V_{IP2} and V_{IP3} as compared with the other devices thus increasing the linearity of the proposed device and making it more reliable. The IIP_3 is another important parameter for determining the linearity, and the value of IIP_3 should be high in order that the device is more linear. When the V_{gs} is lower than 0.9 V, the M_LT_DLTFET has a better IIP_3 than the other devices, thus making the proposed device more reliable as shown in Fig. 12(c). The IMD_3 is called the third-order intermodulation distortion at which the first- and third-order harmonic power are equal. The value of

IMD_3 should be kept as low as possible. However, figure 12(d) shows that the IMD_3 degrades for M_ LT_DLTFET as compared with the other devices. It is noteworthy that the linearity parameters in terms of V_{IP2}, V_{IP3}, IIP_3, and IMD_3 fluctuate greatly at higher gate bias due to the fact that g_{m2} and g_{m3} vary obviously when V_{gs} is higher.

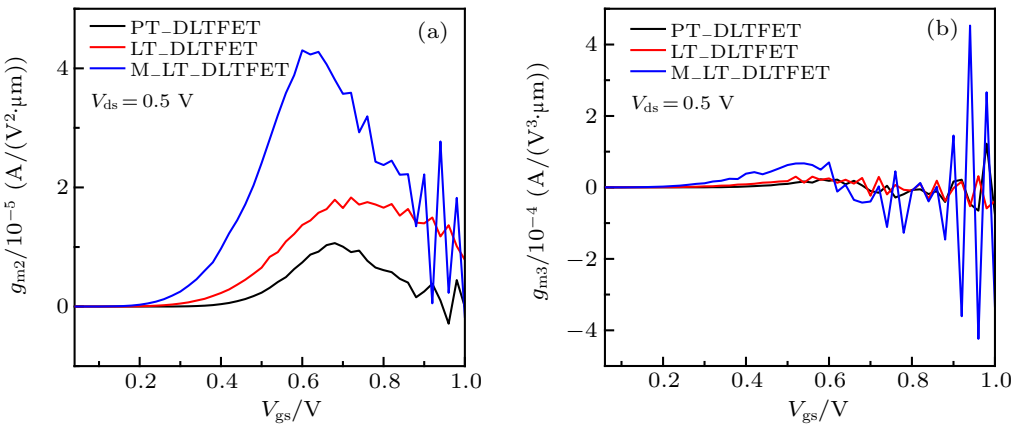


Fig. 11. Plots of (a) g_{m2}, and (b) g_{m3} *versus* V_{gs} for three devices.

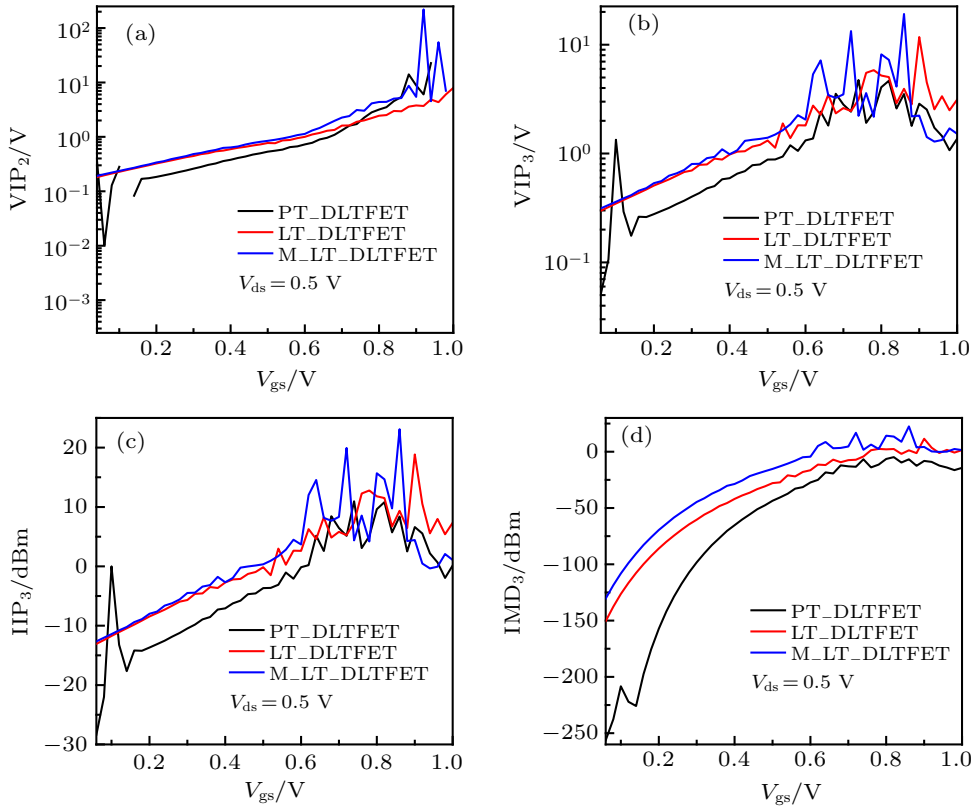


Fig. 12. Linearity parameters of (a) V_{IP2}, (b) V_{IP3}, (c) IIP_3, and (d) IMD_3 for three devices.

For understanding the distortion characteristics of the device, the second- and third-order harmonic distortion (HD_2, HD_3) are considered from the analytical model expressed as the following equations:

$$HD_2 = 1/2 \times V_a \times \frac{\partial g_{m1}}{\partial V_{gs}} / (2 \times g_{m1}), \tag{5}$$

$$HD_3 = 1/4 \times V_a^2 \times \frac{\partial^2 g_{m1}}{\partial V_{gs}^2} / (6 \times g_{m1}), \tag{6}$$

where V_a is the amplitude of the input signal and it is considered to be 50 mV. Figure 13 shows the variations of HD_2 and HD_3 with V_{gs} for three devices. Due to drain current fluctuations (noise), the values of HD_2 and HD_3 are higher near the lower gate–source voltage and decrease afterward. It is obvious that the proposed device provides lesser HD_2 and HD_3 than the other devices. Therefore, the noise in the proposed device will be lesser than those in the other devices. Consequently, it can be concluded that the proposed device is more linear with higher reliability.

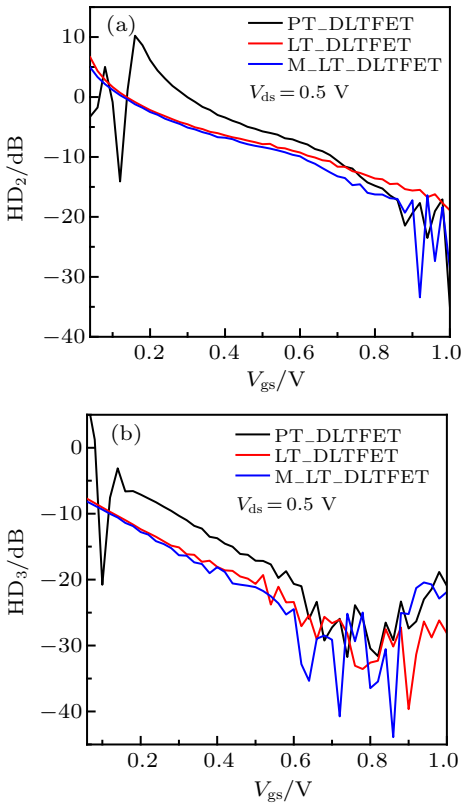


Fig. 13. Plots of (a) HD_2, and (b) HD_3 *versus* V_{gs} for three devices.

4. Conclusions

The optimization of M_LT_DLTFET is proposed and investigated based on DC characteristics, analog/RF parameters and linearity parameters by comparing with those of the other device. The results show that the M_LT_DLTFET can generate higher I_{on} and realize higher I_{on}/I_{off}; at the same time, it retains a sub-60 mV/decade *SS* for over five orders of magnitude of the drain current, and obtains smaller SS_{avg} as well as lower V_{th} due to the implementation of a metal at the tunneling junction. Moreover, the M_LT_DLTFET offers eight times improvement in f_t and GBP compared with the PT_DLTFET. The M_LT_DLTFET shows better analog and RF characteristics, better linearity, as well as small distortions, which makes the proposed device also very attractive for low power, low noise and sensing applications.

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