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Investigation of single event effect in 28-nm system-on-chip with multi patterns*

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Single event effects (SEEs) in a 28-nm system-on-chip (SoC) were assessed using heavy ion irradiations, and susceptibilities in different processor configurations with data accessing patterns were investigated. The patterns included the sole processor (SP) and asymmetric multiprocessing (AMP) patterns with static and dynamic data accessing. Single event upset (SEU) cross sections in static accessing can be more than twice as high as those of the dynamic accessing, and processor configuration pattern is not a critical factor for the SEU cross sections. Cross section interval of upset events was evaluated and the soft error rates in aerospace environment were predicted for the SoC. The tests also indicated that ultra-high linear energy transfer (LET) particle can cause exception currents in the 28-nm SoC, and some even are lower than the normal case.

Keywords: system-on-chip, heavy ion, single event effect

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1. Introduction

The state-of-the-art multi-processor system-on-chip (SoC) is attractive to aerospace applications, thanks to its high performance and low power consumption.[1,2] Nevertheless, the harsh environment in space forces it to overcome some challenges,[3–5] such as single event effect (SEE) including single event upset (SEU), single event functional interruption (SEFI), single event transient (SET), single event latch-up (SEL), and others.[6–8] Currently, the scaled semiconductor manufacture technology makes SEE more serious. Hence, it is extremely necessary to take SEE into account and evaluate this risk comprehensively.[9–12]

SoC integrates multiple high-performance processing units in one single chip. The advantages of weight, performance, and power consumption assist it to be listed in the space application candidates. National Aeronautics and Space Administration (NASA) and other space agencies also hope to evaluate more SoC to pave the way for future space exploration missions.[13] As a typical SoC, Xilinx Zynq-7000 SoC embeds a dual ARM (advanced RISC machine) core processors and FPGA (field-programmable gate array). It makes the SoC work in different processor configuration patterns, including lockstep and the asymmetrical multiprocessing (AMP) patterns.[14,15] For these patterns, SEE vulnerability needs to be examined.

Up to now, although some irradiation tests on the SoC had been carried out, and SEE in several conditions were reported, most tests resolved around sole processor (SP) design.[16–23] A few manuscripts mentioned dual core processor patterns but that just discussed the lockstep pattern.[24,25] Different from these efforts, heavy ion irradiations were performed with different processor configuration patterns, including SP and AMP, in this work to investigate the SEE in SoC comprehensively. Furthermore, the soft error rates in aerospace were also predicted for the SoC based on the test results.

2. Irradiation tests

The SoC was irradiated at the National Innovation Center of Radiation Application (NICRA), China Institution Atomic Energy (CIAE), and Heavy Ion Research Facility in Lanzhou (HIRFL) using ions at several different linear energy transfers (LETs).

2.1. Device under test

The Xilinx Zynq-7020 SoC was irradiated in this study, which is fabricated with 28-nm high-k metal gate (HKMG)

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complementary metal–oxide–semiconductor (CMOS) technology. The processing system and programmable logic are two important parts of the SoC. Dual ARM Cortex-A9 processors, on-chip memory (OCM), Cache, direct memory access (DMA) controller, watchdog, and various interfaces are integrated in the processing system.[26,27] Its BGA (ball grid array) package has been de-capped in both irradiations. The irradiation tests have been carried out under normal voltage condition which is 12 V for the entire board and 1 V for the processors.

2.2. The irradiation platform

The first irradiation was performed using the HI-13 Tandem Accelerator (HI-13) at NICRA, and the second was conducted at HIRFL. The irradiation at the HI-13 took place in a vacuum, while the test at HIRFL was in the air. Table 1 lists the ions, LETs, and ranges in this work.[28]

Table 1. The used ions in the heavy ion irradiation.

Facility	Ions	Energy/MeV	LET/MeV·cm^2·mg^{-1}	Range in silicon/μm
HI-13	Cl	160	13.1	46.0
	Si	135	9.3	50.7
	C	80	1.7	127.1
HIRFL	Ta	1697.4	78.3	99.3

In both irradiations, a programmable power supply provided the 12-V input for test board. It was also used to investigate possible current abnormalities. Under normal conditions, the current is about 330 mA. The UART (universal asynchronous receiver/transmitter) over USB (universal serial bus) interface provided communication between the host and the test board.

2.3. Test patterns

The OCM block is in charge of loading the first stage boot loader program of the system. Its reliability is critical to the entire SoC. During irradiations, 32KB OCM was tested statically and dynamically under SP and AMP patterns.

SP pattern: the SoC runs applications on one ARM processor only, namely Core0. In this pattern, 0xA5A5A5A5 is written, readback and compared by Core0 to detect SEU.

AMP pattern: the applications are co-executed by two ARM core processors. Generally, the Core1 acts as the slave and should be woken by Core0 as master. In this case, the two processors are asymmetric. In the AMP pattern, OCM is shared by two cores. Core0 wakes up Core1 while system launches and then writes the data to OCM. After that, Core1 is responsible for checking SEU events. It reads the data back and compares them with the expected ones to determine whether an SEU occurs.

3. Results and discussion

Four different LET ions were used in two irradiations as shown in Table 1. For the striking of each LET ion, SEU and SEFI events were detected. The SEFI events were detected as the UART output exception. It is more important to note is that abnormal currents, which were lower than normal one, were detected in the HIRFL irradiation.

3.1. HI-13 irradiation results

In HI-13 irradiation, the LETs of ions used were lower than that of HIRFL irradiation. The fluxes of the ions are approximately (1.0–3.0)$\times 10^3$ cm^{-2}·s^{-1} and for each LET ion, the cumulative fluence is about 10^6 cm^{-2}.

Table 2 presents the detected events in this irradiation. It can be seen that the numbers of SEEs induced by ions of different LETs vary. For the same LET ion, the AMP and SP patterns suffer from different SEE sensitivities. For both patterns, the numbers of SEU increase as the LET increases. Similar trend can be found for SEFI events. Figure 1 depicts the cross sections in different patterns with three LETs. The cross section is calculated by Eq. (1) while the error is obtained from Eq. (2) since the number of SEE events is the dominate error contribution.[29]

$$\delta = n/(FN), \tag{1}$$

$$\delta_e = \sqrt{n}/(Fn), \tag{2}$$

where δ is the cross section in the unit of cm^2·bit^{-1} and δ_e is the error, n is the number of the detected events, F is the fluence in unit cm^{-2}, and N is the total tested bits.

Table 2. The detected errors in the HI-13 irradiation.

LET/ MeV·cm^2·mg^{-1}	CPU pattern	Data test	SEU	SEFI
13.1	AMP	Static	504	44
	SP	Dynamic	175	33
9.3	AMP	Static	252	38
	SP	Dynamic	124	26
1.7	AMP	Static	91	7
	SP	Dynamic	40	4

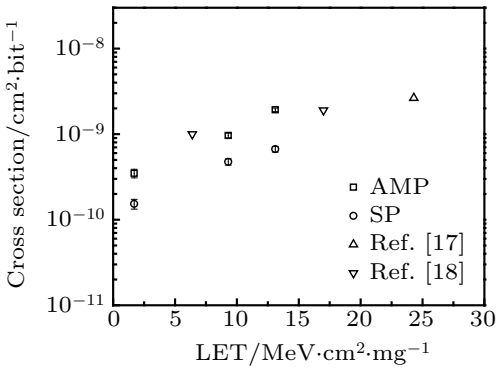


Fig. 1. SEU cross sections in HI-13 irradiation.

The LET of Cl is 13.1 MeV·cm^2·mg^{-1}, and the cross sections in AMP and SP patterns are $(1.92 \pm 0.09) \times 10^{-9}$ cm^2·bit^{-1} and $(6.77 \pm 0.60) \times 10^{-10}$ cm^2·bit^{-1}, respectively. The LET of Si is 9.3 MeV·cm^2·mg^{-1}, and the cross sections in AMP and SP patterns are $(9.65 \pm 0.6) \times 10^{-10}$ cm^2·bit^{-1} and $(4.75 \pm 0.40) \times 10^{-10}$ cm^2·bit^{-1}, respectively. Compared with the cross sections in the SP pattern, that of the AMP pattern is more agreed with the reported ones in Refs. [17] and [18] which were obtained in SP patterns with static tests. That is because the data test in the AMP pattern is static. It means SEU influenced by data test type more rather than processor patterns. The SEFI cross sections calculated by Eqs. (1) and (2) without N parameter are depicted in Fig. 2. It can be seen that the AMP pattern seems to experience more SEFI events compared with the SP pattern.

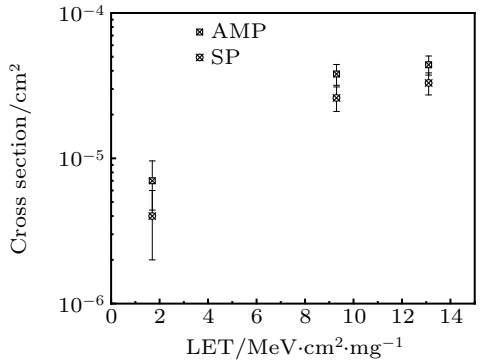


Fig. 2. SEFI cross sections in the HI-13 irradiation.

3.2. HIRFL irradiation results

The LET is much higher in the HIRFL irradiation test, which reaches 78.3 MeV·cm^2·mg^{-1}. In this irradiation, besides SEU and SEFI events, abnormal currents are investigated too.

The tests included AMP dynamic (AMP-D), SP static (SP-S), and SP dynamic (SP-D). For each test, the flux is 10^3 cm^{-2}·s^{-1} and the fluence is in the ranges of (2.1–3.0)$\times 10^5$ cm^{-2}. The parameters of each test can be observed in Table 3.

Table 3. The parameters of the tests in HIRFL irradiation.

CPU pattern	Data test	Fluence/cm^{-2}
AMP	Dynamic	2.1×10^5
SP	Static	3.0×10^5
	Dynamic	2.5×10^5

Table 4. The detected SEE in HIRFL irradiation.

CPU pattern	Data test	SEU	SEFI
AMP	Dynamic	284	47
SP	Static	1277	33
	Dynamic	254	41

Table 4 summarizes the detected SEE events in this irradiation. For the SEU events, which cover the single bit upset and multi cells upset events. The upset events are illustrated in Fig. 3. The most upset cell reaches 20 in the SP static test.

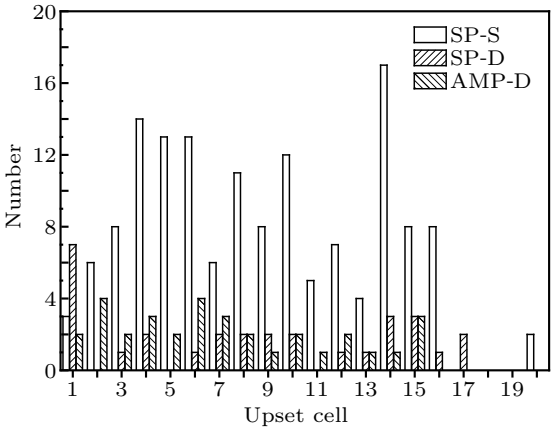


Fig. 3. The detected upset cells in the HIRFL irradiation.

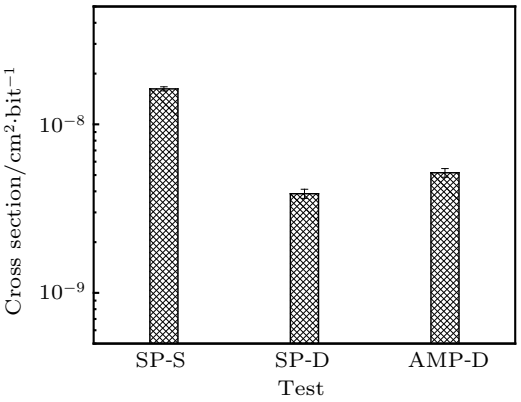


Fig. 4. The cross sections of the tests in HIRFL irradiation.

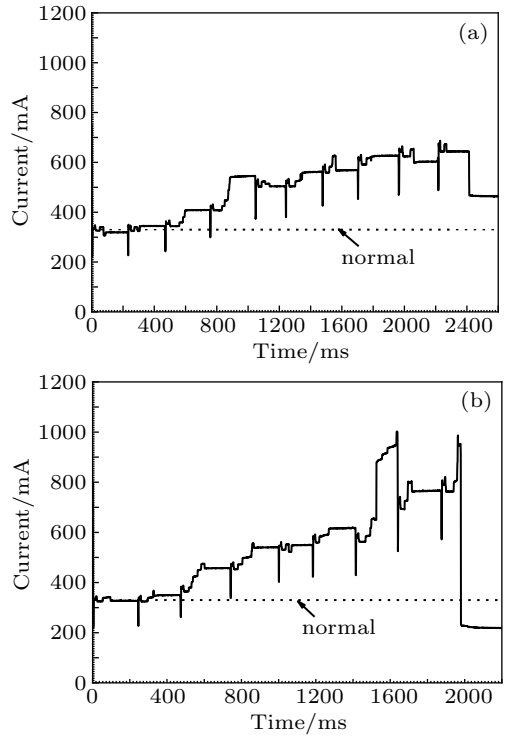


Fig. 5. The detected currents in the HIRFL irradiation, (a) the currents are higher than the normal case, (b) a part of the currents are less than the normal case.

Figure 4 describes the SEU cross sections of each test in this irradiation. Compared with cross sections of the SP and AMP dynamic data test which are at the 10^{-9} level, that of the SP static data test is $(1.6\pm0.05)\times10^{-8}$ cm^2·bit^{-1}.

Another noteworthy phenomenon is the exception of the supply power current in the HIRFL irradiation. As it was not observed in the HI-13 irradiation, it proclaims that the SEE in a high LET environment is more complicated. Figure 5 shows the currents in the irradiation. Figures 5(a) and 5(b) present two sets of variable abnormal currents. These variable currents were detected while the output of the UART still worked well. It should be noticed is that some current is lower than the normal case in Fig. 5(b).

3.3. Discussion

In the HI-13 irradiation, no matter the AMP and SP patterns, the cross sections increase as the increment of the LETs. In Fig. 1, the results also evidence a static cross section can be higher than the dynamic ones as much as twice. As Table 5 shows, the least cross sections ratio between static and dynamic tests is 2.03. Compared with the static data test, the dynamic test rewrites the memories repeatedly. This operation can refresh the memory cells and reduces the accumulative risk of some vulnerable cells.

Table 5. The cross sections ratio between static and dynamic tests in HI-13 irradiation.

LET/MeV·cm^2·mg^{-1}	13.1	9.3	1.7
Cross section ratio (static/dynamic)	2.88	2.03	2.28

In the HIRFL irradiation test, the LET is 78.3 MeV·cm^2·mg^{-1}, which is much higher than that of the HI-13 irradiation. The static cross section in the SP pattern is $(1.6\pm0.05)\times10^{-8}$ cm^2·bit^{-1}, compared with the dynamic cross sections in SP and AMP patterns, the discrepancy is even more than twice. It reveals processors pattern is not a critical factor for SEU, again. Through comprehensive analysis of the SEU cross sections in the HI-13 and HIRFL irradiations, it can be concluded that the SEU cross section more depends on the data test modes instead of the processors' patterns.

The static and dynamic cross sections of both irradiations can be fitted into two Weibull curves with Eq. (3) shown in Fig. 6. The parameters are listed in Table 6. It means the stature static and dynamic cross section for the OCM blocks are about 1.9×10^{-8}cm^2·bit^{-1} and 3.7×10^{-9} cm^2·bit^{-1}. Usually, the 28-nm SoC works in general applications, some data in the OCM are accessed statically and some are refreshed frequently. It can be speculated the SEU probability exists in the region between two curves.

$$\sigma(\mathrm{LET}) = \sigma_{\mathrm{sat}}(1-\exp\{-[(\mathrm{LET}-L_{\mathrm{th}})/W]^S\}), \quad (3)$$

where σ_{sat} is the stature cross section in units cm^2·bit^{-1}, L_{th} is the threshold of the LET in units MeV·cm^2·mg^{-1}, W and S are fitting parameters.

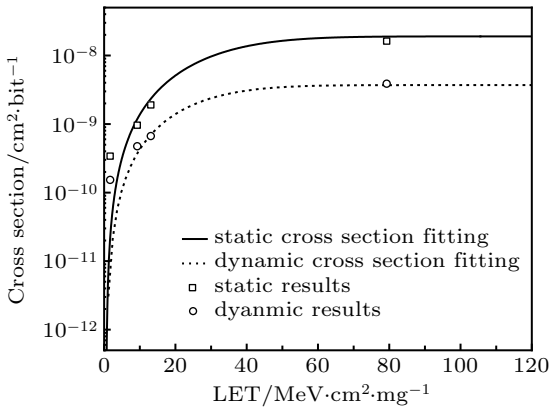


Fig. 6. The Weibull fitting from the irradiation tests.

Table 6. The Weibull function parameters for both fittings.

	σ_{sat}/cm^2·bit^{-1}	L_{th}/MeV·cm^2·mg^{-1}	W	S
Static cross section fitting	1.9×10^{-8}	0.55	35	1.98
Dynamic cross section fitting	3.7×10^{-9}	0.55	29	1.87

Depending on the obtained Weibull curves, the space SEU error rates of static and dynamic memory accessing are evaluated with CREME96 (Cosmic Ray Effects on Micro-Electronics) at solar quite circumstances. The orbit is 450 km, and the inclination angle is 51.6° with 100-mil aluminum.[30,31] Table 7 describes the predicted error rates.

Table 7. The predicted SoC orbit soft error rate.

	Bit error /bit^{-1}·day^{-1}	Device error /device^{-1}·day^{-1}
Static	2.46×10^{-8}	5.16×10^{-2}
Dynamic	1.35×10^{-8}	2.83×10^{-2}

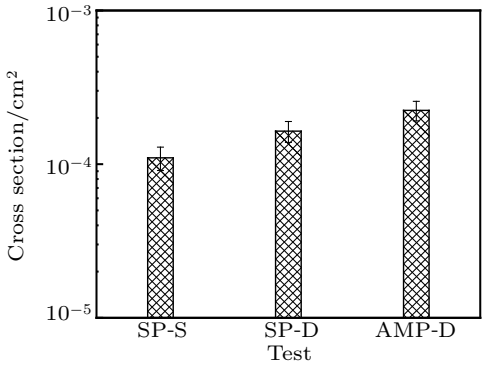


Fig. 7. SEFI cross section of different tests in HIRFL irradiation.

Different from the SEU cross sections, SEFI cross sections seem to be more sensitive to the processors' patterns. Figure 2 depicts the SEFI cross sections in the HI-13 irradiation test. It is visible that the AMP pattern experiences more SEFI events compared with the SP pattern. Figure 7 shows the SEFI cross section of the HIRFL irradiation. It signifies

the AMP pattern suffering most SEFI compared with others, again. For the AMP pattern, two processors, in turn more registers, are utilized, this increases the SEFI possibility.

Apart from SEU and SEFI events, eight to eleven current steps can be viewed in Fig. 5(a) after 500 ms, and six to ten current steps are visible in Fig. 5(b) after 600 ms. A commonality in Figs. 5(a) and 5(b) is the currents experiencing a sharp decrement. In these cases, though no error was detected at the UART output, in order to protect the test board, the supply was cut off arbitrarily. The abnormal currents were investigated from the board power interface not the OCM directly. The cause of such abnormal current events can be speculated theoretically as follows. Firstly, SoC is the HKMG CMOS technology, it can emerge parasitic structure to stimulate SEL current when a high LET ion strikes, usually, the SEL events can cause step increment currents.[32,33] Secondly, different circuits spread over the chip with different SEL sensitivities, some vulnerable circuits may encounter SEL repeatedly in a high LET ion striking. The two sets of abnormal currents may occur in the same circuit or different ones. Power management unit, input/output circuit, memory cell, sense amplifier circuit, and others may be the suffered circuit units. Thirdly, different circuit units have different power supply rails in the SoC. Since we cannot monitor every power rail, it is difficult to accurately determine which rail suffers from the current exception, whether and how it propagates. It is a complicated system, to clear this phenomenon, we should do lots of work in the future.

4. Conclusion

The Xilinx Zynq-7020 SoC was irradiated by heavy ions of several LETs. SEE events in different conditions were investigated. The results illustrate that the static test encounters higher SEU cross sections compared with the dynamic test, and which is not affected by the processor configuration patterns. The cross section discrepancy is more than twice between the static and dynamic tests. For a general application of the SoC, the interval of SEU cross section and space error rates were evaluated. The cross section is 3.7×10^{-9} cm^2·bit^{-1}–1.9×10^{-8} cm^2·bit^{-1} and the soft error rate is in the range of $(1.35–2.46)\times10^{-8}$ bit^{-1}·day^{-1}. For the high LET particle, besides inducing the multi cell upsets up to 20 cells, it also causes obvious expectation currents in 28-nm SoC.

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