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Citation: Chin. Phys. B . 2020, 29(10): 107401 . **doi:** 10.1088/1674-1056/ab99b5
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Simulation study of device physics and design of GeOI TFET with PNN structure and buried layer for high performance*

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(Received 23 April 2020; revised manuscript received 26 May 2020; accepted manuscript online 5 June 2020)

Large threshold voltage and small on-state current are the main limitations of the normal tunneling field effect transistor (TFET). In this paper, a novel TFET with gate-controlled $P^+N^+N^+$ structure based on partially depleted GeOI (PD-GeOI) substrate is proposed. With the buried P^+-doped layer (BP layer) introduced under $P^+N^+N^+$ structure, the proposed device behaves as a two-tunneling line device and can be shut off by the BP junction, resulting in a high on-state current and low threshold voltage. Simulation results show that the on-state current density I_{on} of the proposed TFET can be as large as 3.4×10^{-4} A/μm, and the average subthreshold swing (*SS*) is 55 mV/decade. Moreover, both of I_{on} and SS can be optimized by lengthening channel and buried P^+ layer. The off-state current density of TTP TFET is 4.4×10^{-10} A/μm, and the threshold voltage is 0.13 V, showing better performance than normal germanium-based TFET. Furthermore, the physics and device design of this novel structure are explored in detail.

Keywords: Ge-based TFET, two line tunneling paths, point tunneling, on-state current density

PACS: 74.55.+v, 85.30.Tv, 85.30.De **DOI:** 10.1088/1674-1056/ab99b5

1. Introduction

With the complementary metal–oxide–semiconductor (CMOS) transistor scaling down, power dissipation becomes a most crucial issue in high-density integration and low-standby-power operation systems. Since the power dissipation is proportional to the device operating voltage, a single effective way to reduce the power dissipation is to lower the subthreshold swing of the devices, which enables the using of a lower supply voltage.[1,2] However, due to the carrier injection mechanism, the subthreshold swing of traditional MOSFET is limited to 60 mV/dec at room temperature.[3,4] Hence, tunneling field-effect transistor (TFET) which is essentially a gated P–i–N diodehas been explored and attracted much interest in recent years.

Due to its band-to-band tunneling (BTBT) operation mechanism, the TFET is characterized as steep subthreshold swing at room temperature, low leakage current in off state and excellent short channel effects.[5,6] However, since a thin inversion layer on the surface of the channel of normal TFETs is necessary to exploit the gate-controlled BTBT between the channel and drain/source, the normal TFET is characterized as "point" tunneling device, resulting in the low on-state current and high threshold voltage, which are below the requirement set in ITRS[7] and are the main limitation of TFET.[8,9]

To increase the on-state current, L-shaped channel TFET (LTFET),[10] U-shaped channel TFET (UTFET),[11,12] T-shaped gate TFET (TG-TFET),[13] Z-shaped TFET (ZS-TFET),[14] L-shaped gate TFET (LG-TFET),[10] elecron–hole bilayer TFET (EHB TFET),[8] electro-statically doped source/drain double-gate tunnel field effect transistors (EDSDDG-TFETs),[15] L-shaped Ge source TFET (LS-TFET),[16] *etc.*, are developed. Although they are successful in increasing the on-state current by enlarging tunneling junction cross-sectional area, these types of TFETs also based on strong inversion mode, result in the hardly reduction of threshold voltage. To reduce the threshold voltage, the TFET based on fully depleted SOI substrate is studied.[17] Furthermore, since germanium is recognized as a potential material for TFET due to its 0.67 eV of bandgap energy and the integration with the Si CMOS process,[18–21] the performance of fully depleted germanium on insulator (FD-GeOI) TFET has been investigated.[22–26] Through depleting channel by gate at zero bias, the threshold voltage of FD-GeOI TFET can be as low as 0.05 V, but it is also based on P–i–N structure and worked in strong inversion mode.

To enhance the on-state current furthermore, a new n-type TFET based on FD-GeOI substrate with P^+–N^+–N^+ structure (PNN TFET) was proposed in our previous work (as shown in Fig. 1).[27] The metal with large work function (such as Au, Pt, *etc.*) is adopted as a gate electrode to deplete the entire channel region as it works in junctionless FET[28,29] at zero-biased gate voltage ($V_{GS} = 0$ V). In the on-state, due to the heavy doping of channel, significant tunneling occurs in the

*Project supported by the National Natural Science Foundation of China (Grant No. 61704130), the Science Research Plan in Shaanxi Province, China (Grant No. 2018JQ6064), and the Science and Technology Project on Analog Integrated Circuit Laboratory, China (Grant No. JCKY2019210C029).

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whole region of the source/channel p^+/n^+ junction. Thus, the PNN TFET behaves as "line" tunneling device and works in flat band mode or accumulation mode.

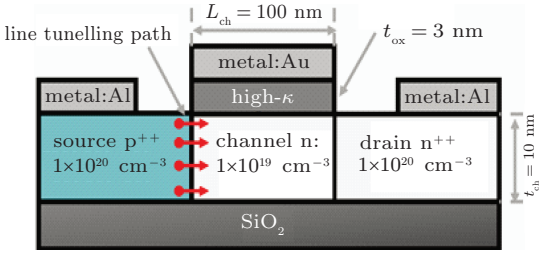


Fig. 1. Cross section of device structure of normal PNN TFET based on FD-GeOI.

However, to ensure the full depletion of the channel by gate at zero bias, the gate electrode with a larger work function and the channel with a thinner thickness are preferred. In our design, Gold with a 5.1-eV work function is chosen as a gate electrode and the thickness of Ge should be less than 10 nm. Thus, the threshold voltage is also too large and serious gate induced drain leakage (GIDL) effect is caused in the off state.[27] Moreover, the tunnel line of the PNN TFET is less than 10 nm, which is not long enough to enhance the on-state current to the level of MOSFET.

Thus, in this work, a novel n-TFET with gate-controlled $P^+N^+N^+$ structure based on partially depleted PD-GeOI substrate is proposed. With the buried P^+ doped layer (BP layer) introduced under $P^+N^+N^+$ structure, the proposed device behaves as a two-tunneling line device and can be shut off by the BP junction. Aluminum is chosen as the gate electrode, which can suppress the GIDL current much more in the off-state. Simulations are carried out to study the performance of the proposed TFET and its on-state current, off-state current, subthreshold swing, threshold voltage are investigated. Furthermore, the physics and device design of this novel structure are studied in detail.

2. Device structure and simulation approach

Figure 2 shows the cross section of the proposed TFET with two tunneling paths (TTP TFET) based on PD GeOI. Unlike PNN TFET, the proposed TFET has a buried P^+-doped layer (BP layer) under channel, and aluminum with a work function of 4.2 eV is used for the TFET gate metal. Thus, this type of TFET has two line tunneling paths: line tunneling path 1 and line tunneling path 2, which can enhance its on-state current greatly. Also, due to the heavy doping, there is a significant point tunneling that occurs between buried layer and drain when the device is in its off-state. So the slightly doped region (LD region, LDR), and the gap between buried layer and the edge of gate electrode (L_{gap}) are introduced to restrict the point tunneling at zero gate bias.

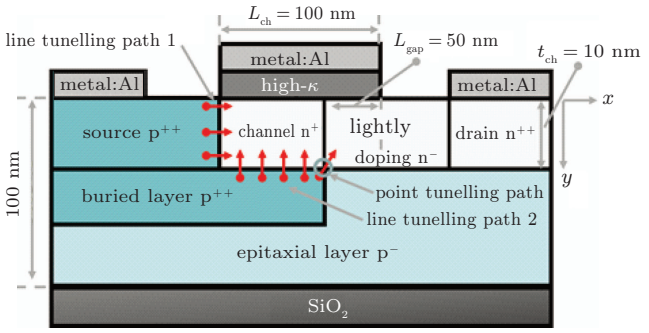


Fig. 2. Cross-section of two tunneling paths (TTP) TFET based on PD-GeOI substrate.

The device operation can be understood from the simulated band diagrams of line tunneling paths 1 and 2 shown in Figs. 3(a) and 3(b). At zero gate bias ($V_{GS} = 0$ V), since depletion region of the unilaterally abrupt p^+/n junction is mainly distributed in the slightly doped region, the channel above buried layer is fully depleted by BP layer, thus the device is in its off-state (solid lines) and there occurs no line tunneling.

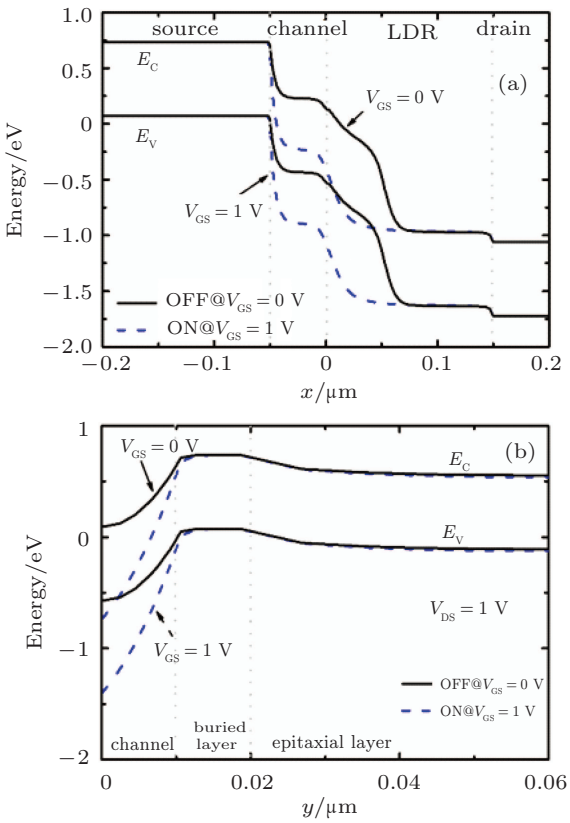


Fig. 3. Computed energy-band diagrams of TTP TFET for both off-state (solid line, $|V_{DS}| = 1$ V, $V_{GS} = 0$ V) and on-state (dashed line, $|V_{DS}| = 1$ V, $V_{GS} = 1$ V) along (a) line tunneling path 1 and (b) line tunneling path 2.

With a 1-V gate bias, channel exits in the depletion state and band-to-band tunneling is turned on (dashed lines) in the line tunneling paths 1 and 2 directions, respectively. In this working mechanism, the channel is depleted by the pn junction of buried layer and channel, and the on-state current can be enhanced greatly by two line tunneling paths, which is very

different from the scenarios in PNN TFET and normal PiN TFET.

Simulations were carried out by using Sentaurus TCAD. The nonlocal BTBT model was considered forband-to-band tunneling. And the bandgap narrowing (BGN) model was also included due to the influence of the effective bandgap on the tunneling current. Also, the Shockley–Read–Hall (SRH) recombination model was included due to the presence of high impurity atom concentration in the channel and Fermi–Dirac statics to calculate the intrinsic carrier concentration. For more accurate current calculations, the field-dependent and doping-dependent mobility degradation model, drift-diffusion current transport model, were also considered. The parameters used in our simulation are shown in Table 1.

Table 1. Simulated device parameters used in this study.

Parameter	TTP TFET	PNN TFET
Gate length L_{ch}/nm	100	100
Channel doping/cm^{-3}	1×10^{19}	1×10^{19}
HfO_2 thickness T_{ox}/nm	3	3
Buried layer length L_{BP}/nm	50	–
Epitaxial layer doping N_{epi}cm^{-3}	1×10^{17}	–
Buried doing N_{BP}/cm^{-3}	1×10^{20}	–
Lightly doped region N_{LD}/cm^{-3}	5×10^{18}	–
Gate metal	aluminum	gold
Source/drain-metal	aluminum	aluminum
Source/drain-doping/cm^{-3}	1×10^{20}	1×10^{20}

3. Results and discussion

Figure 4 shows the transfer characteristics of the proposed TTP TFET and PNN TFET. Owing to the two line tunneling paths existing, an on-state current density of 3.4×10^{-4} A/μm is achieved at $V_{GS}=1$ V, increased by two orders of magnitude compared with that of normal PNN TFET. Since GIDL effect is restricted due to the surface electrical field decreasing by 4.2-eV work function of aluminum, the off-state current density of TTP TFET is 4.4×10^{-10} A/μm, decreasing almost by four orders of magnitude compared with that of the normal PNN TFET. Therefore, the proposed TTP TFET exhibits an extremely high I_{on}/I_{off} ($\sim10^6$). The threshold voltage (V_{TH}) is 0.13 V obtained by a constant current method with a current of 100 nA,[16] which is much less than that of PNN TFET. The average subthreshold swing (*SS*) is 55 mV/decade.

Figure 5 shows the composition of current of the proposed TTP TFET. It can be seen clearly that the on-state current density I_{on} of TTP TFET is almost the sum of the on-state current density in the TFET with tunneling path 1 and the on-state current density in the TFET with tunneling path 2, and the off state current density I_{off} of TTP TFET is the same as that of TFET only has tunneling path 2. That means the performance of the device is mainly determined by the structure of line tunneling path 2.

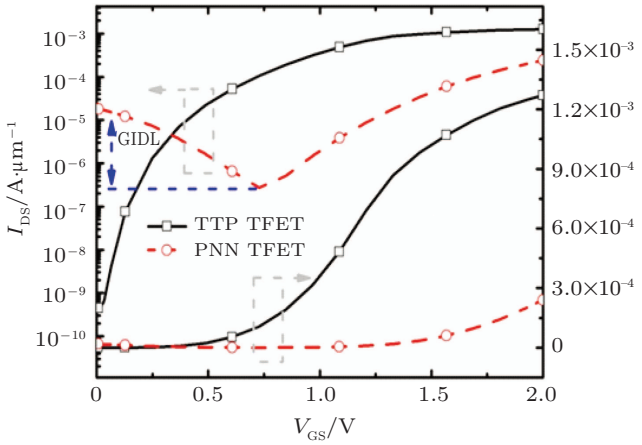


Fig. 4. Transfer characteristics of FD-GOI TFET and proposed TTP TFET.

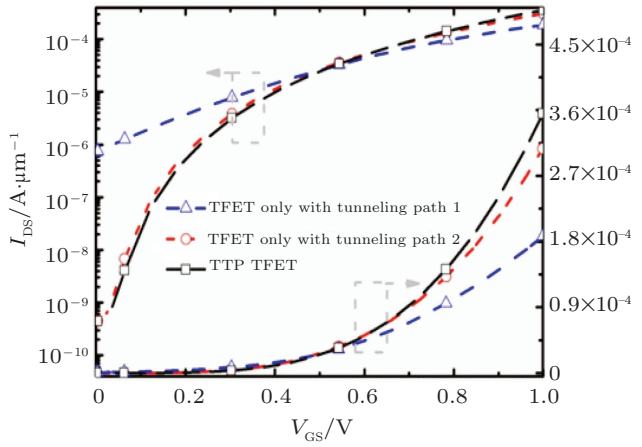


Fig. 5. Composition of current of the proposed TTP TFET.

Figure 6 shows the transfer characteristics of the TTP TFET biased at $V_{DS}=1$ V for the case of the length of buried layer L_{BP} increasing from 50 nm to 100 nm. Since the tunnel length of path 2 is enlarged with the increase of L_{BP}, the on-state current density I_{on} at $V_{GS}=1$ V and $V_{DS}=1$ V augments from 3.3×10^{-4} A/μm to 5.1×10^{-4} A/μm when L_{BP} increases from 50 nm to 90 nm as expected. However, when $L_{BP}=100$ nm, I_{on} at $V_{GS}=1$ V and $V_{DS}=1$ V decreases instead, which can be explained below.

When L_{BP} is much less than the length of channel L_{CH} ($L_{BP}<L_{CH}$), the whole depletion region of buried PN junction is beneath the gate electrode, which can be effectively controlled by V_{GS}. But when $L_{BP}=L_{CH}$, due to the lateral diffusion of the buried PN junction, the depletion region outside the gate edge cannot be modulated by gate bias voltage, which pinches the channel off. So, the on state resistance of the device when $L_{BP}=L_{CH}$ is much larger than that when $L_{BP}<L_{CH}$, resulting in the reduction of I_{on} at $V_{GS}=1$ V, $V_{DS}=1$ V. Figure 7 shows the surface electron density of

TTP TFET for different L_{BP} at $V_{GS} = 1$ V, $V_{DS} = 1$ V. It can be clearly seen that the minimum value of electron density is 8.53×10^{-16} cm^{-2} when $L_{BP} = L_{CH} = 100$ nm. It means that the electrons at the lightly doping region outside the gate edge when $L_{BP} = 100$ nm is depleted, verifying the discussion above.

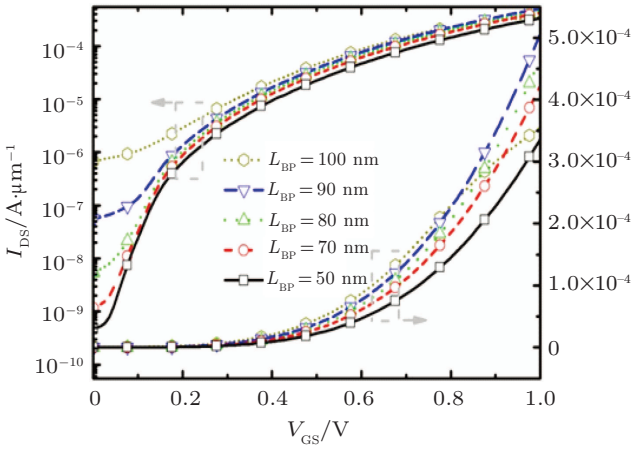


Fig. 6. Transfer characteristics of TTP TFET for different lengths of buried layer L_{BP}.

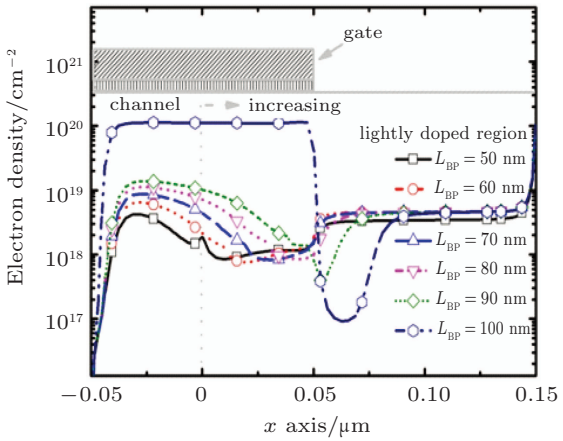


Fig. 7. Distributions of surface electron density along x axis of TTP TFET for different values of L_{BP} at $V_{GS} = 1$ V and $V_{DS} = 1$ V.

From Fig. 6, it can also be seen that I_{off} at $V_{GS} = 0$ V and $V_{DS} = 1$ V increases about 3 orders of magnitude when L_{BP} changes from 50 nm to 100 nm. The increase of L_{BP} results in the decrease of L_{gap}, and the point tunneling from buried layer to slightly doped region shown in Fig. 2 in the off-state is improved.

Figure 8 shows the tunneling width of the point tunnel when $L_{BP} = 50$ nm and 100 nm, respectively. The T_{w1} and T_{w2} represent their corresponding tunneling widths. It can be observed that T_{w1} is much thinner than T_{w2}. A smaller tunneling width improves the tunneling of electrons from the channel region to the slightly doped region,resulting in the significant increase of I_{off}.

As discussed above, the introduction of LDR is to restrict the point tunnel at the upper right-hand corner of the buried layer shown in Fig. 2. Figure 9 shows the calculated point tunnel width at $N_{LDR} = 5 \times 10^{18}$ cm^{-3} and $N_{LDR} = 1 \times 10^{19}$ cm^{-3}, when the device works in the on-state and off-state, respectively. It is found that with a larger N_{LDR}, energy band bending from channel to LDR both in the on state and off state is steeper. The steeping in energy band bending narrows the tunneling width, thus increasing both of I_{on} and I_{off} as indicated in Fig. 10.

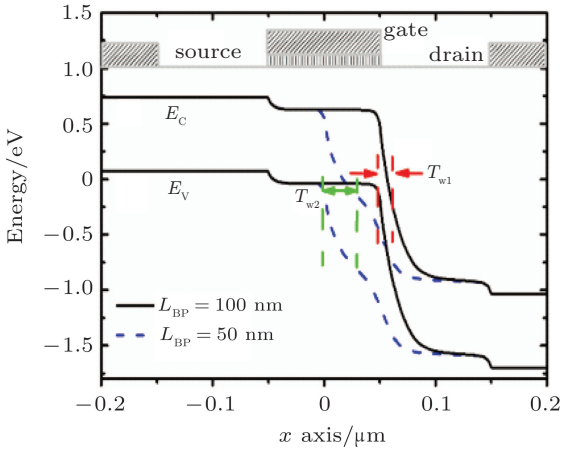


Fig. 8. Point tunneling width when $L_{BP} = 50$ nm and 100 nm at $V_{GS} = 0$ V and $V_{DS} = 1$ V.

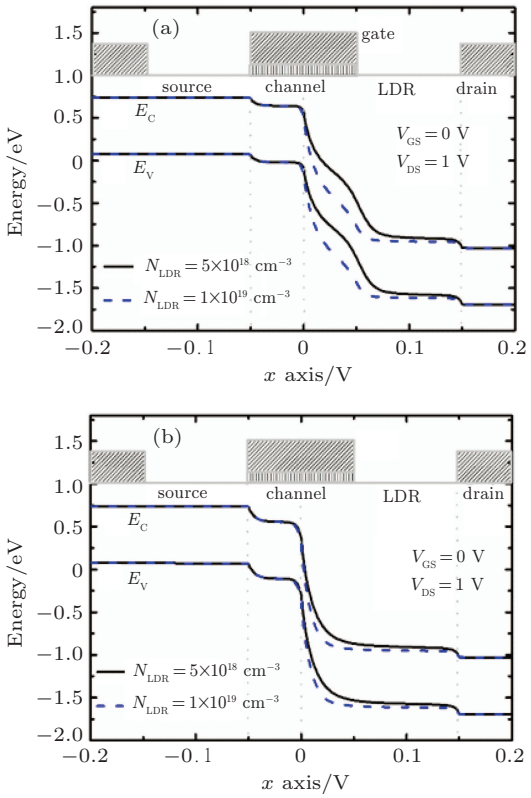


Fig. 9. Band bending from channel to LDR along x axis at the upper right-hand corner of the buried layer for (a) off-state at $V_{DS} = 1$ V, $V_{GS} = 0$ V and (b) on-state at $V_{DS} = 1$ V, $V_{GS} = 1$ V.

Figure 10 shows the simulated influence of the doping concentration of slightly doped region (N_{LDR}) on the performance of TTP TFET. It can be seen that the I_{off} of the TTP TFET at $V_{DS} = 1$ V and $V_{GS} = 0$ V increases almost two

orders of magnitude and I_{on} at $V_{DS} = 1$ V and $V_{GS} = 1$ V increases 11.8%, when N_{LDR} varies from 5×10^{18} cm^{-3} to 1×10^{19} cm^{-3}. That means that I_{off} is more sensitive to the doping concentration of LDR, thus the doping concentration of 5×10^{18} cm^{-3} for the LDR is chosen in our design.

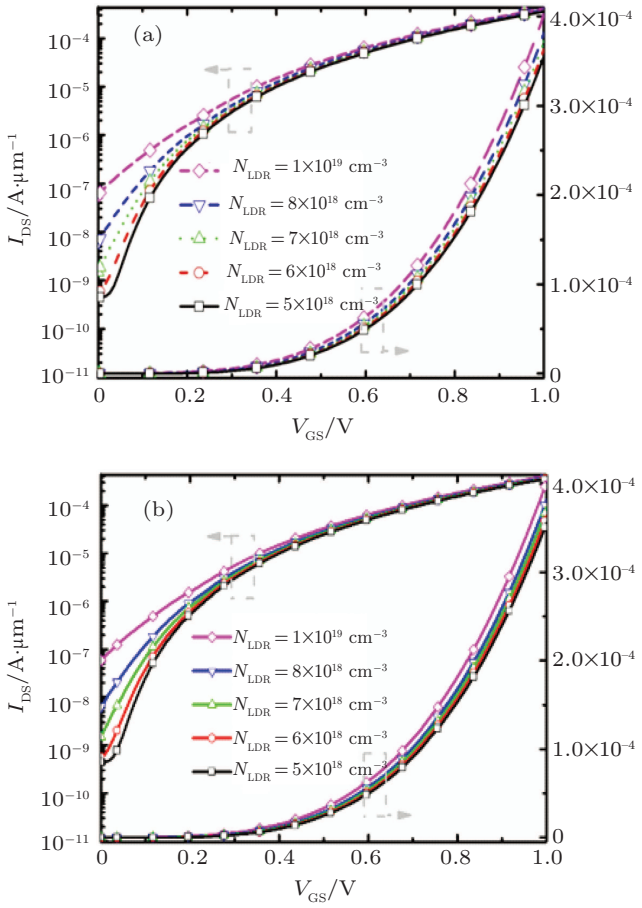


Fig. 10. Transfer characteristics of TTP TFET for different doping concentrations of slightly doped region (N_{LDR}).

Since I_{on} of the TTP TFET is mainly determined by line tunneling path 2 and I_{off} is mainly determined by point tunneling path, the performance of the TTP TFET can be improved by increasing L_{BP} and L_{gap}. Figure 11 shows the optimized performance of the TTP TFET. When the length of buried layer L_{BP} changes from 50 nm to 650 nm while L_{gap} is fixed at 50 nm (which is large enough to restrict the point tunnel shown in Fig. 2 in the off-state), the on-state current density I_{on} improves from 3.6×10^{-4} A/μm to 2.1×10^{-3} A/μm, the threshold voltage V_{TH} decreases from 0.13 V to 0.08 V, and the average *SS* improves from 54 mV/dec to 34 mV/dec. That means that I_{on}, V_{TH}, and *SS* of the TTP TFET can be optimized by enlarging gate length L_{CH} since $L_{CH} = L_{BP} + L_{gap}$, which is very different from those of the normal TFET and MOSFET.

Figure 12 shows the output characteristics of the TTPT-FET with different gate voltages. Due to the tunneling width decreasing with V_{DS}, I_{DS} values, separately, at $V_{GS} = 0.2$ V, 0.4 V, 0.6 V, 0.8 V, and 1 V first increases and then reaches saturation at their corresponding high drain voltages. In our simulations, the drain current I_{DS} at $V_{DS} = 1$ V increases from 7.3×10^{-7} A/μm to 3.4×10^{-4} A/μm when V_{GS} increases from 0.2 V to 1 V, showing good conduction characteristics.

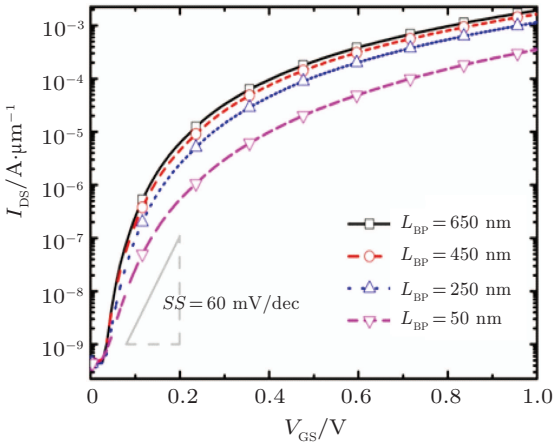


Fig. 11. Plots of optimized performance of TTP TFET for $L_{BP} = 50$ nm, 250 nm, 450 nm, and 650 nm at $L_{gap} = 50$ nm.

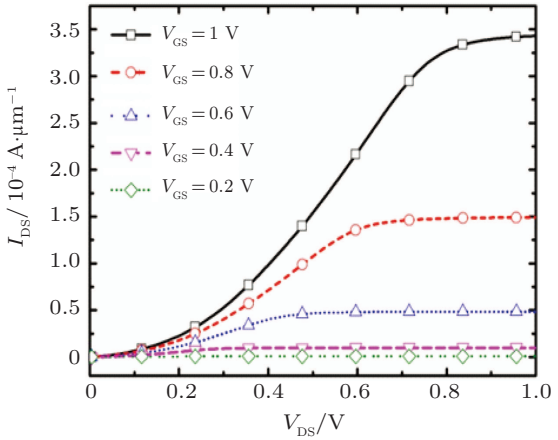


Fig. 12. Output characteristics of TTP TFET.

4. Conclusions

A novel GeOI n-TFET with PNN structure and buried layer is proposed in this work, which behaves as a two-tunneling line device to enhance the on-state current density. Since there is no requirement for a gate with large work function to deplete the channel, the threshold voltage of the TTP TFET is much small and the GIDL current is suppressed. Simulation results show that the on-state current density of the proposed TFET can be as large as 3.4×10^{-4} A/μm, and the average subthreshold swing (*SS*) is 55 mV/decade. Moreover, both of I_{on} and *SS* can be optimized by lengthening the channel and BP layer. The off-state current density of TTP TFET is 4.4×10^{-10} A/μm, and the threshold voltage is 0.13 V, showing better performance than PNN TFET for ultra-low power applications.

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