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Citation: Chin. Phys. B . 2020, 29(8): 087305 . **doi:** 10.1088/1674-1056/ab96a4
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Trap analysis of composite 2D–3D channel in AlGaN/GaN/graded-AlGaN:Si/GaN:C multi-heterostructure at different temperatures*

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(Received 13 March 2020; revised manuscript received 21 May 2020; accepted manuscript online 27 May 2020)

The graded AlGaN:Si back barrier can form the majority of three-dimensional electron gases (3DEGs) at the GaN/graded AlGaN:Si heterostructure and create a composite two-dimensional (2D)–three-dimensional (3D) channel in AlGaN/GaN/graded-AlGaN:Si/GaN:C heterostructure (DH:Si/C). Frequency-dependent capacitances and conductance are measured to investigate the characteristics of the multi-temperature trap states of in DH:Si/C and AlGaN/GaN/GaN:C heterostructure (SH:C). There are fast, medium, and slow trap states in DH:Si/C, while only medium trap states exist in SH:C. The time constant/trap density for medium trap state in SH:C heterostructure are (11 μs–17.7 μs)/(1.1×10^{13} $cm^{-2}\cdot eV^{-1}$–3.9×10^{13} $cm^{-2}\cdot eV^{-1}$) and (8.7 μs–14.1 μs)/(0.7×10^{13} $cm^{-2}\cdot eV^{-1}$–1.9×10^{13} $cm^{-2}\cdot eV^{-1}$) at 300 K and 500 K respectively. The time constant/trap density for fast, medium, and slow trap states in DH:Si/C heterostructure are (4.2 μs–7.7 μs)/(1.5×10^{13} $cm^{-2}\cdot eV^{-1}$–3.2×10^{13} $cm^{-2}\cdot eV^{-1}$), (6.8 μs–11.8 μs)/(0.8×10^{13} $cm^{-2}\cdot eV^{-1}$–2.8×10^{13} $cm^{-2}\cdot eV^{-1}$), (30.1 μs–151 μs)/(7.5×10^{12} $cm^{-2}\cdot eV^{-1}$–7.8×10^{12} $cm^{-2}\cdot eV^{-1}$) at 300 K and (3.5 μs–6.5 μs)/(0.9×10^{13} $cm^{-2}\cdot eV^{-1}$–1.8×10^{13} $cm^{-2}\cdot eV^{-1}$), (4.9 μs–9.4 μs)/(0.6×10^{13} $cm^{-2}\cdot eV^{-1}$–1.7×10^{13} $cm^{-2}\cdot eV^{-1}$), (20.6 μs–61.9 μs)/(3.2×10^{12} $cm^{-2}\cdot eV^{-1}$–3.5×10^{12} $cm^{-2}\cdot eV^{-1}$) at 500 K, respectively. The DH:Si/C structure can effectively reduce the density of medium trap states compared with SH:C structure.

Keywords: AlGaN/GaN HEMT, multi-heterostructure, composite 2D–3D channel, multi-temperature trap states

PACS: 73.61.Ey, 85.30.Tv, 85.30.De **DOI:** 10.1088/1674-1056/ab96a4

1. Introduction

GaN-based high electron mobility transistors (HEMTs) are attractive candidates and have bright market prospects in high efficiency and high-power switching applications due to their superior figure of merits.[1,2] The high-power devices need semi-insulating buffer to suppress the leakage and punch-through.[3,4] This can be achieved by introducing acceptor-like trap states with intentional dopants such as iron (Fe) or carbon (C),[5,6] thus reducing the vertical leakage components,[7] the punch-through currents,[8] and may result in a better confinement of the carrier into the two-dimensional electron gas (2DEG).[9] Unlike Fe and Mg, C-doping profile shows neither segregation nor memory effect[10] in the epitaxial stack itself and allows a sharp transition to a UID-GaN channel.[11] At the same time, the C-doping delivers higher breakdown voltage and lower off-state leakage.[12] However, the drawback of this method is poor channel conductivity due to the large potential barrier caused by the highly resistive GaN:C buffer.[13] In previous work, a combination of Si-doped AlGaN back barrier and C-doped GaN buffer heterostructure can yield an increase of channel conductivity.[14] At the same time, the distribution of channel carriers changes from 2DEG to the composite 2DEG–3DEG, due to the polarization modulation of graded AlGaN:Si back barrier, and this new epitaxial structure also introduces some new trap states. It is necessary to systematically study the characteristics of carrier distribution and trap states in AlGaN/GaN/Si-doped AlGaN/GaN:C multi-heterostructures.

In this work, we investigate the GaN-based HEMTs with two kinds of heterostructures, specifically with Si-doped graded AlGaN back barrier to enhance the channel conductivity grown on GaN:C buffer layer. A thin Si-doped graded AlGaN back barrier is chosen rather than Si-doped AlGaN back barrier, because it can provide higher 2DEG and elec-

*Project supported by the National Key Research and Development Program of China (Grant No. 2018YFB1802100), the Natural Science Foundation of Shaanxi Province, China (Grant Nos. 2020JM-191 and 2018HJCG-20), the National Natural Science Foundation of China (Grant Nos. 61904135, 61704124, and 61534007), the China Postdoctoral Science Foundation (Grant Nos. 2018M640957 and 2019M663930XB), and the Wuhu and Xidian University Special Fund for Industry–University-Research Cooperation, China (Grant No. XWYCXY-012019007).

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trons in the graded AlGaN:Si back barrier will be easily transferred to the lower band gap material, *i.e.*, the unintentionally doped GaN channel. The composite 2D–3D channel characteristic is demonstrated by CV measurement in DH:Si/C. Frequency-dependent capacitance and conductance measurements are employed to investigate the trap states in SH:C and DH:Si/C. The high temperature characteristics of channel electron distribution and trap states in SH:C and DH:Si/C are systematically studied. The gate voltage swing range of the trap state response in the DH:Si/C heterostructure is wider than that in SH:C heterostructure. At the same time, there are new types of trap states (fast and slow trap states) in the DH:Si/C heterostructure. These active trap energy levels in SH:C and DH:Si/C gradually become deeper as the measurement temperature increases, and the amplitude of the active medium trap energy levels in DH:Si/C is lower than that in SH:C.

2. Device fabrication

For comparison, the SH:C and DH:Si/C were grown by MOCVD on 3-inch (111) Si substrates (1 inch = 2.54 cm). For the DH:Si/C, the epi-structure consists of a 1.5-μm C-doped GaN buffer/transition layer, 15-nm graded AlGaN back barrier (Al content changed from 30% to 10% and Si-doped), a 14-nm GaN channel layer, and 23-nm barrier layer (including a 1-nm AlN, a 22-nm $Al_{0.25}Ga_{0.75}N$) from bottom to top. The Al composition in the graded AlGaN:Si back barrier varies linearly from 30% to 10%, which exhibits high electron mobility and high electron density.[15] The AlGaN barrier and GaN channel thickness of SH:C and DH:Si/C were the same (23 nm and 14 nm, respectively). The SH:C and DH:Si/C yielded a total 2DEG density of 5.0×10^{12} cm^{-2} and 9.2×10^{12} cm^{-2}, and an electron mobility of 1200 cm^2/V·s and 1125 cm^2/V·s, respectively as determined by Hall measurements. The same device fabrication process was used for the two structures. Device processing started with Ti/Al/Ni/Au source/drain electrodes, and then were annealed at 830 ℃ for 30 s in N_2 environment in order to form the ohmic contact. An SiN of 60 nm was deposited to provide a passivation by PECVD. An opening in SiN for gate diameter was 130 μm, and then Ni/Au/Ni e-beam evaporation and lift-off were carried out subsequently to form the gate. Circle-shaped Schottky barrier diodes (SBDs) used for frequency-dependent capacitance and conductance measurements were fabricated for the two types of samples. Figures 1(a) and 1(b) show the schematic cross section of the SH:C and DH:Si/C, respectively. The energy band profile and electron distributions are simulated to optimize the position, aluminum composition, Si doping concentration and profile, and thickness of the graded AlGaN back barrier, and the simulations results for SH:C and DH:Si/C are shown in Figs. 1(c) and 1(d), respectively. Appropriate models, such as Blaze III–V compound material, Shockley–Read–Hall recombination, low-field mobility and polarization, were used. The AlGaN back barrier was chosen to be 14 nm away from the AlGaN/GaN interface. This distance was large enough to keep the continuous distribution of high electron concentration in the GaN channel, and it was short enough to avoid depleting the channel electrons. The Si-doped graded AlGaN can form most part of 3DEG at the GaN/graded AlGaN heterostructure and create enough potential barrier height.

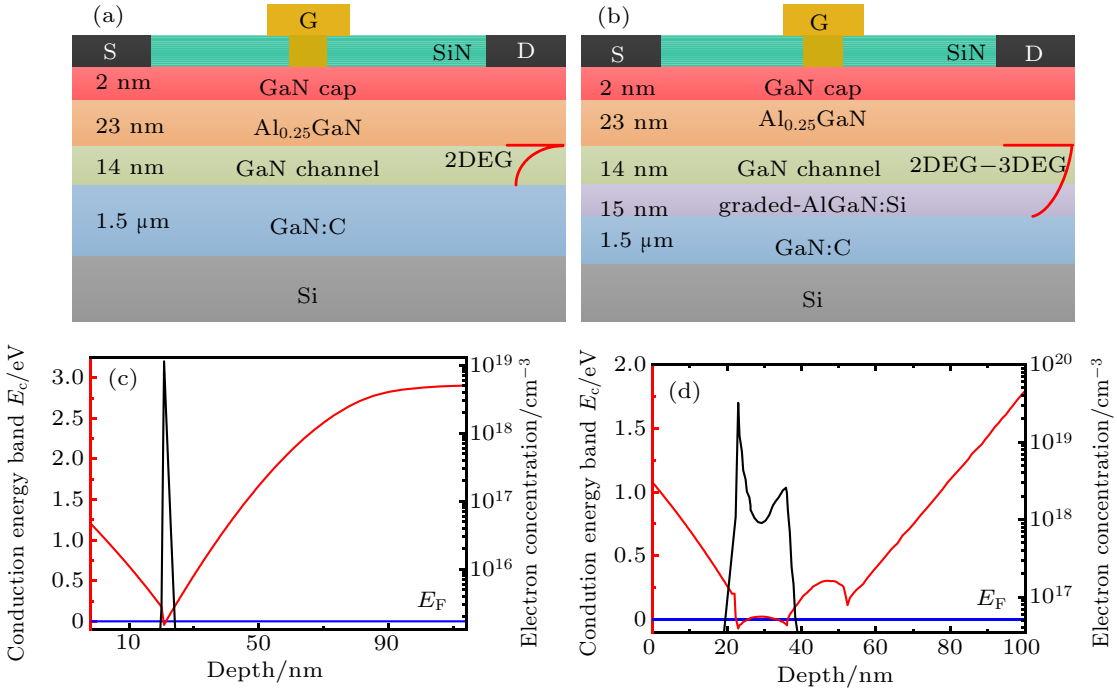


Fig. 1. Schematic cross-section of fabricated (a) SH:C and (b) DH:Si/C HEMT. Energy band diagram and electron distribution of (c) SH:C and (d) DH:Si/C.

3. Results and discussion

The *C–V* characteristics of SH:C and DH:Si/C are shown in Fig. 2. Since Si-doped graded AlGaN:Si back barrier can enhance the conductivity of channel, the threshold voltage of DH:Si/C is more negative than that of SH:C. In the accumulation region (shown by arrow 1), the larger dispersions in multi-temperature *C–V* characteristics of DH:Si/C imply that its equivalent capacitance increases and the equivalent barrier thickness decreases at high temperature. It is because the more electrons diffuse into the AlGaN barrier with temperature rising up to 500 K. In the transition region (shown by arrow 2), there is one sharp rising slope in the *C–V* characteristics of SH:C and there are two rising slopes in the *C–V* characteristics of DH:Si/C. Two rising slopes are corresponding to the AlGaN/GaN heterostructure and the GaN/graded AlGaN:Si heterostructure in DH:Si/C. For the SH:C, the positive shift of *C–V* curve becomes more obvious with temperature increasing due to the buffer-related trap states in the GaN:C buffer layer.[16] For the DH:Si/C, the positive shift of *C–V* curve with temperature increasing just happens in the bottom channel rather than upper channel. It is because the Si-doped graded AlGaN back barrier blocks the electron from being captured/de-trapped by the upper channel through the buffer-related trap states.

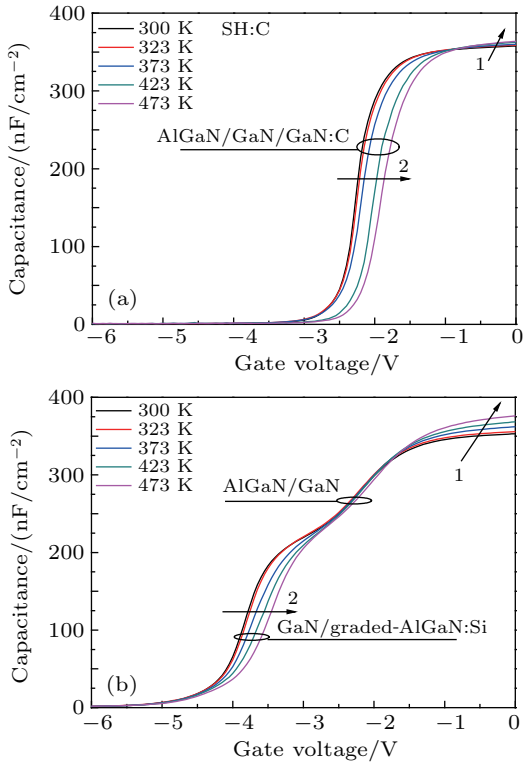


Fig. 2. *C–V* characteristics of (a) SH:C and (b) DH:Si/C with temperature increasing from 300 K to 500 K.

The electron distribution profiles of the two heterostructures are extracted from the *C–V* curves and plotted in Fig. 3. The channel electron densities of 4.8×10^{12} cm^{-2} and 9.4×10^{12} cm^{-2} in SH:C and DH:Si/C are calculated from Fig. 3. It indicates that the Si-doping graded AlGaN back barrier is an attractive technique to significantly increase channel electron density and it can achieve peak concentration up to a few 10^{20} cm^{-3}. The comparison of energy band diagram between the two heterostructures shows that the DH:Si/C has the higher electron density in UID-GaN channel layer due to Si-doped graded AlGaN back barrier (inset of Fig. 1(d)). With temperature increasing, the electron densities located in AlGaN/GaN heterostructure decrease to 4.4×10^{19} cm^{-3} and 6.58×10^{19} cm^{-3} in SH:C and DH:Si/C respectively. This is because the electrons in the channel gain higher kinetic energy and are more likely to overflow from the potential well, thus reducing the carrier concentration in the channel.[17]

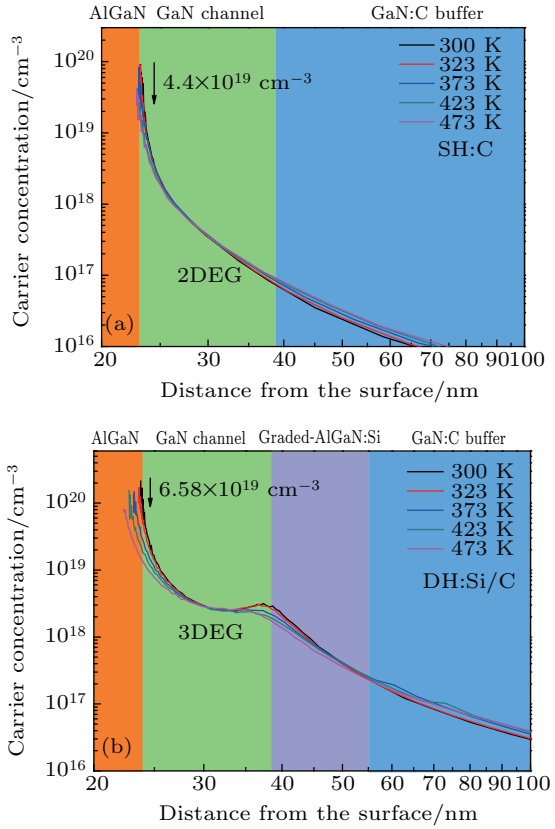


Fig. 3. Capacitance–voltage (*C–V*) characteristics calculated the approximate charge density profiles of (a) SH:C and (b) DH:Si/C at different temperatures.

Figure 4 shows the plots of conductance *versus* radial frequency for SH:C at selected gate voltages at temperatures 300 K and 500 K. Frequency dependent conductance (G_p) is analyzed to extract the trap parameters, trap time constant (τ_T) and trap state density (D_{it}). The detailed extraction process can be found in Ref. [18]. With resulting G_p, the D_{it} and τ_T quantities are extracted directly by fitting the experimental G_p/ω values as a function of radial frequency (ω) according to the equation $G_p/\omega = qD_{it}/2\omega\tau_T \cdot \ln(1+(\omega\tau_T)^2)$ on the assumption that trap is comprised of energy levels. The curve

of G_p/ω has a maximum at $\omega \approx 2/\tau_T$ and $D_{it} = 2.5G_p/q\omega$ at the maximum point. From the fitting results in Fig. 4, the medium time constants and trap densities are τ_T = (11 μs–17.7 μs)/D_{it} = 1.1×10^{13} cm^{-2}·eV^{-1}–3.9×10^{13} cm^{-2}·eV^{-1} and τ_T = (8.7 μs–14.1 μs)/D_{it} = 0.7×10^{13} cm^{-2}·eV^{-1}–1.9×10^{13} cm^{-2}·eV^{-1} for SH:C, respectively at 300 K and 500 K.

The excellent agreement between the experimental data and fitting curves indicates that the assumption is reasonable that the three different trap states (shown in Fig. 5): fast, medium, and slow trap states: are present in the DH:Si/C. The time constants and trap densities for fast, medium and slow trap states are τ_T = (4.2 μs–7.7 μs)/D_{it} = 1.5×10^{13} cm^{-2}·eV^{-1}–3.2×10^{13} cm^{-2}·eV^{-1}, τ_T = (6.8 μs–11.8 μs)/D_{it} = 0.8×10^{13} cm^{-2}·eV^{-1}–2.8×10^{13} cm^{-2}·eV^{-1}, τ_T = (30.1 μs–151 μs)/D_{it} = 7.5×10^{12} cm^{-2}·eV^{-1}–7.8×10^{12} cm^{-2}·eV^{-1} at 300 K, respectively. The amplitude of medium trap state in DH:Si/C (from the AlGaN/GaN heterostructure) is lower than that of the SH:C. Compared with the trap type of SH:C, the GaN/graded-AlGaN:Si heterostructure possesses the fast and slow trap states. When the temperature increases to 500 K, the time constants and trap densities for fast, medium, and slow trap states are τ_T = (3.5 μs–6.5 μs)/D_{it} = 0.9×10^{13} cm^{-2}·eV^{-1}–1.8×10^{13} cm^{-2}·eV^{-1}, τ_T = (4.9 μs–9.4 μs)/D_{it} = 0.6×10^{13} cm^{-2}·eV^{-1}–1.7×10^{13} cm^{-2}·eV^{-1}, τ_T = (20.6 μs–61.9 μs)/D_{it} = 3.2×10^{12} cm^{-2}·eV^{-1}–3.5×10^{12} cm^{-2}·eV^{-1}, respectively.

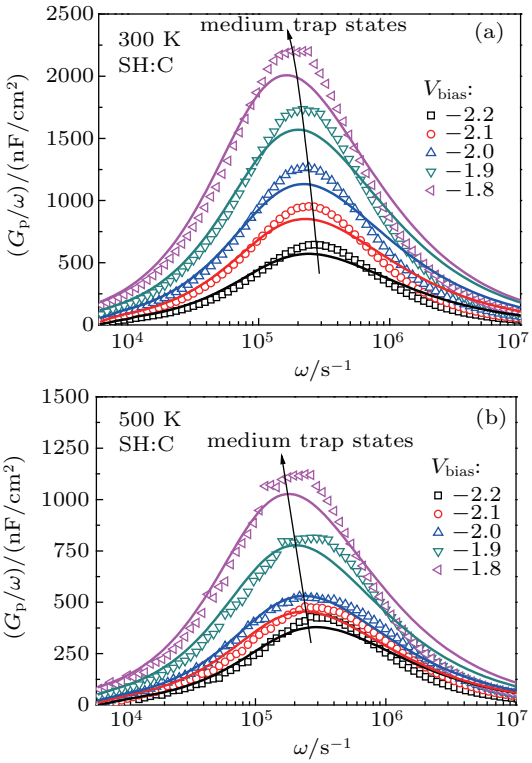


Fig. 4. Plots of conductance *versus* radial frequency for SH:C at (a) 300 K and (b) 500 K for some selected gate voltages, respectively.

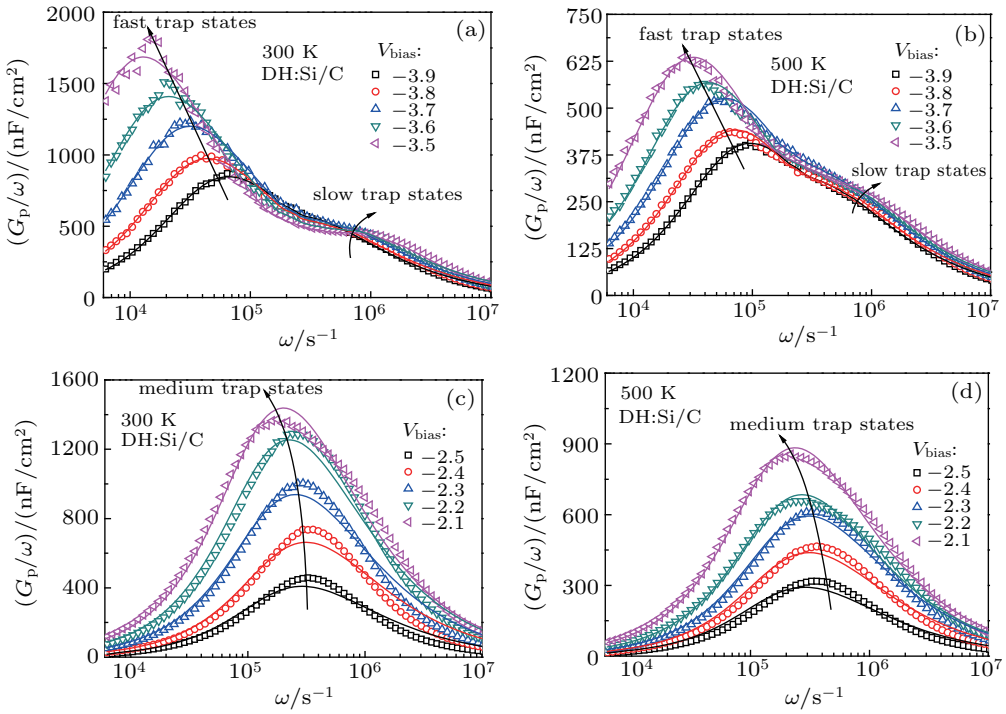


Fig. 5. Plots of conductance *versus* radial frequency for DH:Si/C at (a) 300 K and (b) 500 K for some selected low gate voltages, and plots of conductance *versus* radial frequency at (c) 300 K and (d) 500 K for DH:Si/C at some selected high gate voltages.

Figure 6(a) shows the plots of resulting τ_T *versus* gate voltage for SH:C and DH:Si/C at 300 K and 500 K. The relation τ_T–V_{gate}, obtained from frequency-dependent conductance measurement in SH:C and DH:Si/C, is nearly exponential evidently. The variation trend of time constant with gate voltage reflects the location distribution of trap energy

level in a bottom-up direction. In Fig. 6(a), each of the time constants of the slow trap states increases as the gate voltage becomes more positive. It indicates that the location distribution of slow trap energy level is from shallow level to deep level in the bottom-up direction. However, the time constants of other trap states each exhibit a negative trend. It indicates that the location distribution of other trap energy level is from deep level to shallow level in the bottom-up direction. Figure 6(b) shows the plots of trap state density *versus* energy level for SH:C and DH:Si/C. The trap state energy is estimated by using the expression $E_T/kT = \ln(\sigma_T N_c \nu_t \tau_T)$, where capture cross section of trap state is $\sigma_T = 3.4 \times 10^{-15}$ cm^2,[19] the density of states in the conduction band is $N_c = 4.3 \times 10^{14} \times T^{3/2}$ cm^{-3},[20] the thermal velocity of the carrier is $\nu_t = (3kT/m^*)^{0.5}$,[21] and the effective mass of the density of states is $m^* = 1.5m_0$.[20] In SH:C, the trap state density (1.1×10^{13} cm^{-2}·eV^{-1}–3.9×10^{13} cm^{-2}·eV^{-1}) is located at E_T between 0.353 eV and 0.359 eV at 300 K. These trap states are possibly attributed to vacancy-type defects such as V_N-complexes at $E_C - 0.35$ eV located in the GaN buffer layer.[22] In DH:Si/C, the fast trap state density (1.5×10^{13} cm^{-2}·eV^{-1}–3.2×10^{13} cm^{-2}·eV^{-1}) is located at E_T between 0.322 eV and 0.341 eV, and the medium trap state density (0.8×10^{13} cm^{-2}·eV^{-1}–2.8×10^{13} cm^{-2}·eV^{-1}) is located at E_T between 0.342 eV and 0.348 eV, and the slow trap state density (7.5×10^{12} cm^{-2}·eV^{-1}–7.8×10^{12} cm^{-2}·eV^{-1}) is located at E_T between 0.377 eV and 0.418 eV at 300 K. According to previous studies,[23] the energy level of trap states (extended defects, such as threading dislocations) ranges from 0.19 eV to 0.41 eV, located in Si-doped AlGaN layer. The Silicon is commonly used as shallow donor dopant, and it can create other deep levels, respectively, at $E_C - 0.37$ eV and $E_C - 0.4$ eV.[24] Therefore, these trap states are possibly attributed to extended defects such as threading dislocations and Si-doping related defects.

As the measurement temperature rises from 300 K to 500 K, the trap state density of SH:C decreases from (1.1×10^{13} cm^{-2}·eV^{-1}–3.9×10^{13} cm^{-2}·eV^{-1}) to (0.7×10^{13} cm^{-2}·eV^{-1}–1.9×10^{13} cm^{-2}·eV^{-1}) over the energy range from 0.594 eV to 0.611 eV. The fast trap state density of DH:Si/C decreases from (1.5×10^{13} cm^{-2}·eV^{-1}–3.2×10^{13} cm^{-2}·eV^{-1}) to (0.9×10^{13} cm^{-2}·eV^{-1}–1.8×10^{13} cm^{-2}·eV^{-1}) over the energy range from 0.558 eV to 0.573 eV, and the medium trap state density of DH:Si/C decreases from (0.8×10^{13} cm^{-2}·eV^{-1}–2.8×10^{13} cm^{-2}·eV^{-1}) to (0.6×10^{13} cm^{-2}·eV^{-1}–1.7×10^{13} cm^{-2}·eV^{-1}) over the energy range from 0.579 eV to 0.588 eV, and the slow trap state density of DH:Si/C decreases from (7.5×10^{12} cm^{-2}·eV^{-1}–7.8×10^{12} cm^{-2}·eV^{-1}) to (3.2×10^{12} cm^{-2}·eV^{-1}–3.5×10^{12} cm^{-2}·eV^{-1}) over the energy range from 0.62 eV to 0.665 eV. Previously reported nitrogen antisites are coherent and these traps located in the narrow range from $E_C - 0.5$ eV to $E_C - 0.664$ eV,[25–32] which corresponds to our measured deep trap energy states both in SH:C and in DH:Si/C by frequency-dependent capacitances and conductance measurements at 500 K. Therefore, the deep trap energy states both in SH:C and in DH:Si/C are likely to be attributed to native defects such as nitrogen antisites located in GaN buffer, GaN channel or Si-doped AlGaN back barrier. The shifts of energy levels of the active traps in SH:C and DH:Si/C are almost the same (about 0.24 eV), which indicates that the Si-doped graded AlGaN back barrier can also effectively prevent the channel electron from entering into the buffer layer at the high temperature.

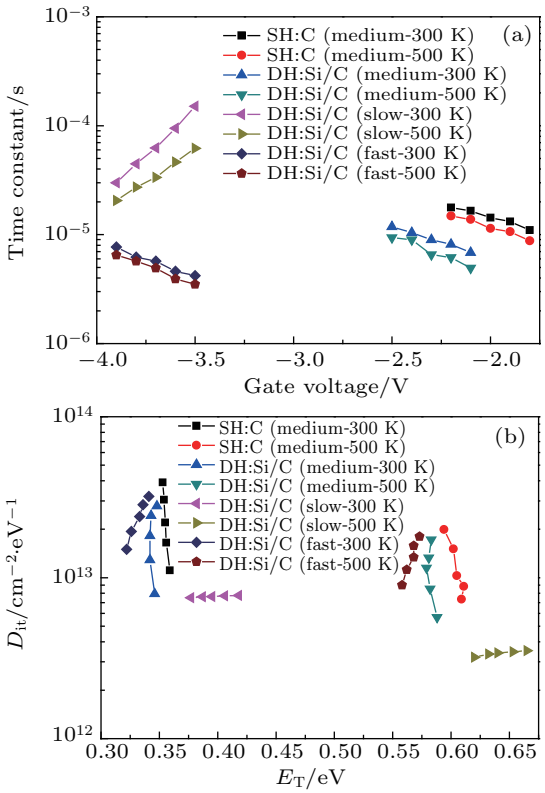


Fig. 6. Plots of (a) time constant of trap state *versus* gate voltage and (b) trap state density *versus* trap state energy of SH:C and DH:Si/C.

4. Conclusions

In this study, the channel electron distribution and frequency-dependent capacitance in a temperature range from 300 K to 500 K are measured to analyze the trap states both in SH:C and DH:Si/C. The Si-doped graded AlGaN back barrier can form most part of 3DEG at the GaN/graded AlGaN heterostructure and create a composite 2D–3D channel in the GaN channel layer, and therefore enhance the channel conductivity by graded AlGaN:Si back barrier. Three different trap states: fast, medium, and slow are present in the DH:Si/C, while only medium traps exist in the SH:C. The trap energy levels become deeper and more kinds of trap states appear in the DH:Si/C than in the SH:C. In addition, the trap energy lev-

els both in the DH:Si/C and in the SH:C gradually become deeper as the measurement temperature increases.

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