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Citation: Chin. Phys. B . 2020, 29(6): 067404 . **doi:** 10.1088/1674-1056/ab90e3
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Quadruple-stacked Nb/Nb_xSi_{1-x}/Nb Josephson junctions for large-scale array application*

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(Received 28 April 2020; accepted manuscript online 7 May 2020)

Large-scale Josephson junction (JJ) arrays are essential in many applications, especially quantum voltage standards application for which hundreds of thousands of junctions are required to realize a high quantum voltage. For almost all applications, high-quality JJ arrays must be realized in a small chip area. This study proposes vertically quadruple-stacked Nb/$(Nb_xSi_{1-x}/Nb)_4$ JJs to increase the integration density of junctions in an array. The current–voltage (I–V) characteristics of a single stack of Nb/$(Nb_xSi_{1-x}/Nb)_4$ JJs have been measured at 4.2 K. The uniformity of junctions in one stack and the uniformity of several stacks over the entire 2 inches wafer have been analyzed. By optimizing the fabrication parameters, a large-scale quadruple-stacked Nb/$(Nb_xSi_{1-x}/Nb)_4$ array consisting of 400000 junctions is realized. Good DC I–V characteristics are obtained, indicating the good uniformity of the large-scale array.

Keywords: niobium, Josephson junction array, voltage standard

PACS: 74.78.–w, 74.81.Fa, 06.20.fb **DOI:** 10.1088/1674-1056/ab90e3

1. Introduction

If a Josephson junction (JJ) is driven at frequency f, then its current–voltage (I–V) curve will develop constant voltage regions at $nhf/2e$, where n is an integer; e is the elementary charge; and h is the Planck constant. With a typical applied microwave frequency of 18 GHz, one junction can only output a quantum voltage of ~ 37 μV for the first step. Therefore, hundreds of thousands of JJs must be connected in series to output a high quantum voltage. Large-scale JJ arrays are essential in many applications, especially for quantum voltage standards applications.[1–4] For example, ~ 0.3 million JJs are required for a quantum voltage of 10 V.[5–7] High-quality large-scale JJ arrays are clearly crucial for quantum voltage chip applications. Superconductor–normal metal–superconductor (SNS) JJs are usually used in the voltage standards.[4]

To increase the number of JJs in an array, they are often stacked vertically. This arrangement not only saves space in a chip but also reduces the branches of the coplanar waveguide (CPW). For programmable voltage standards, this can increase the output voltages for a given microwave drive frequency and chip area; for the ac voltage standard, it can increase the output voltage, output bandwidth, and operating margins. Therefore, to optimize the performance of the voltage standards, studies have tried to pack junctions more densely. The National Institute of Standards and Technology (NIST), USA, uses triple-stacked JJs,[5] whereas Physikalisch-Technische Bundesanstalt, Germany,[6] and National Institute of Advanced Industrial Science and Technology, Japan,[7] use double-stacked JJs. Currently, the National Institute of Metrology, China, has achieved a quantum voltage output of 0.5 V by using triple-stacked JJs.[8] In the present study, we propose large-scale quadruple-stacked SNS JJs to verify the fabrication ability for obtaining large quantum voltages. This junction is designed with the structure Nb/$(Nb_xSi_{1-x}/Nb)_4$, where Nb is the superconducting layer and Nb_xSi_{1-x} is the normal metal layer. In this design, four JJs are stacked vertically. When 100000 junctions are stacked in a plane, the total number of junctions will be quadrupled. Through improvements in fabrication processes, quadruple-stacked JJs have been fabricated. Large-scale JJ arrays consisting of 100000 stacks or 400000 junctions have been designed and realized. Although NIST has fabricated stacks up to 10 junctions tall of $MoSi_2$ barrier junctions, there are only 1000 stacks in an array.[9] In this study, tall stacks of Nb_xSi_{1-x} barrier JJs are realized; furthermore, the integration density is increased compared with that achieved by NIST. The DC I–V curves of these devices are measured and analyzed to test the junction uniformity.

2. Fabrication

Nb/$(Nb_xSi_{1-x}/Nb)_4$ layers are sputtered *in situ* in a high-vacuum chamber. The sputtering power for the superconducting Nb film is 500 W, and the deposition rate is ~ 0.75 nm/s. The Nb_xSi_{1-x} film is co-sputtered with sputtering powers of 33 W or 36 W for Nb and 248 W for Si, respectively, as shown in Fig. 1. The deposition rate for the barrier layer of the Nb target at 50 W is about 0.033 nm/s, corresponding to a change of 0.003 nm/s per 5 W. It is a very small change compared with the Si deposition rate of 0.15 nm/s at 248 W. So a common rate of 0.16 nm/s for calculating the barrier thickness is used. During the deposition of the tri-layer films, the substrate

*Project supported by the National Key R&D Program of China (Grant No. 2016YFF0200402).

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is backside cooled by flowing water. The temperature of the wafer is about 20 ℃ after the tri-layer deposition. The barrier layer and middle Nb layer have thicknesses of about 24 nm and 56 nm, respectively.

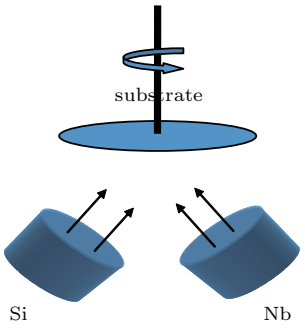


Fig. 1. Schematic of co-sputtering deposition of the Nb_xSi_{1-x} barrier.

The main challenge is to fabricate a vertical profile for the junction definition etch of all stacked junctions so that the stacked junctions can have nearly the same junction area and, in turn, the same critical current. A reactive ion etching (RIE) compound with inductively coupled plasma is used to etch the top Nb layer, the alternating Nb middle layer, and the Nb_xSi_{1-x} barrier layer. The junction area definition process is optimized compared with previously reported processes.[9,10] Apart from SF_6 and C_4F_8, CHF_3 is added to the etching mixture gas. SF_6 and CHF_3 act as etching gases, whereas C_4F_8 acts as a passivating gas to protect the junction profile and keep the side facade steep and clean so that the junctions in the stack can remain uniform.

SiO_2 is deposited in a plasma-enhanced chemical vapor deposition system and used as an insulating layer. The Nb base electrode is etched using SF_6. By contrast, SiO_2 is etched using CHF_3 and O_2. Before depositing the 500-nm-thick Nb wiring electrode, the contact area is subjected to DC-biased RF cleaning. The wire layer is etched by RIE with SF_6 again. Figure 2 shows the picture of one sample of the stacked junction arrays. There are single stacks, 10000 stacks, and 100000 stacks designed on the chip.

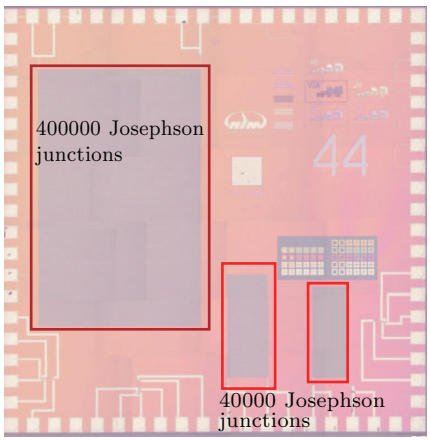


Fig. 2. Photo of the Josephson junction array device.

3. Measurement

The quality of the etch process is directly observed by transmission electron microscopy (TEM), as shown in Fig. 3. The sample is double-side milled and polished to a thickness of less than 100 nm by using a focused ion beam to realize appropriate thinned areas for high-resolution TEM. The figure reveals a vertical profile with a little undercut. The scale of the figure indicates that the variation in the lateral dimension is less than 100 nm. Compared with the junction area size of 6 μm ×10 μm, this leads to a nonuniformity of less than 5%, which is tolerable for voltage standard applications.

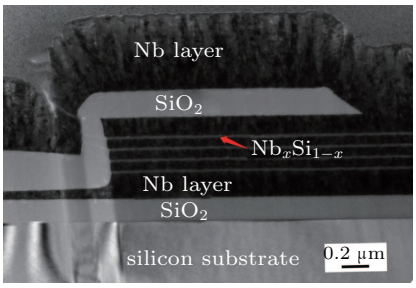


Fig. 3. Structure of quadruple-stacked $Nb/(Nb_xSi_{1-x}/Nb)_4$ Josephson junctions as observed by TEM.

There are three samples which have been measured at 4.2 K. Table 1 shows the characteristics of the samples. Through changing the thickness and Nb content of the barrier, the critical current and I_cR_n can be adjusted. For sample No. 2, the Nb content in the barrier is decreased from that of No. 1. So the barrier resistance is increased and the critical current is smaller compared to those of No. 1. For sample No. 3, the barrier thickness is increased compared with that of No. 1. Then the barrier resistance is increased too and the critical current also become smaller than those of No. 1. Although the critical current is different for No. 2 and No. 3, the I_cR_n is nearly the same. So through adjusting the barrier parameters, junctions with various properties can be achieved, and for 40 μV of I_cR_n, which is ideal for voltage standard application.

Table 1. Characteristics of the quadruple-stacked samples.

Sample No.	1	2	3
Barrier thickness/nm	23	23	26
Nb sputtering power/W	36	33	36
I_c/mA	12.5	7.8	10.16
I_cR_n/μV	59.4	41.7	40.38
Junction area size	6 μm ×10 μm	6 μm ×10 μm	6 μm ×10 μm

Figure 4 shows the *I*–*V* curve of one stack of quadruple-stacked $Nb/(Nb_xSi_{1-x}/Nb)_4$ Josephson junctions from No. 1. The critical current spread for a single stack is from 12.2 mA to 12.5 mA as shown in the insert of Fig. 4. It presents a non-uniformity of 2.5%, which is consistent with the analysis above. We use the average critical current value of the stacks

to represent the critical current of one stack. Four quadruple-stacked junctions from No. 1 are measured. The current spread of the four samples ranges from 12.35 mA to 12.8 mA (Table 1), corresponding to a nonuniformity of 3.6% that should be caused by the inconsistency of the photolithography patterns. Therefore, the nonuniformity caused by lithography or etching should be within a tolerance of $\sim 5\%$ for voltage standard applications.[9]

Table 2. Critical current spread over in sample No. 1.

No.	44	45	55	64
I_c/mA	12.25	12.34	12.8	12.8

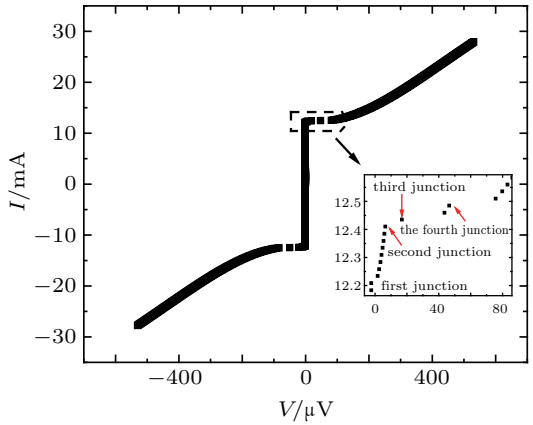


Fig. 4. The *I*–*V* curve of one stack of Nb/(Nb$_x$Si$_{1-x}$/Nb)$_4$ Josephson junctions.

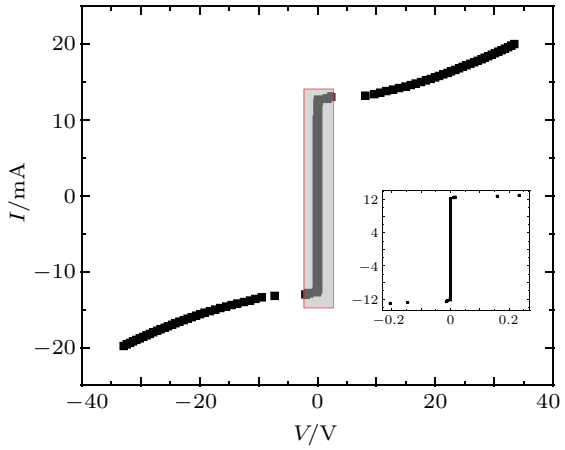


Fig. 5. The *I*–*V* curves of 10000 stacks consisting of 40000 junctions in series.

The *I*–*V* curves for 40000 and 400000 junctions arrays are also measured at 4.2 K, as shown in Figs. 5 and 6, respectively. These figures show that the critical current for the large-scale stacked junction arrays is uniform. Furthermore, 400000 junctions are large enough for a 10-V Josephson voltage standard. Therefore, we did not further expand the scale of the junction array. For taller stacks, the uniformity will worsen, and a heating effect will be seen because of the heat dissipation problem of the junctions at the top of the stack. Furthermore, the *I*–*V* curve will become rounder. Therefore, we did not increase the stack height or integrate more junctions in an array.

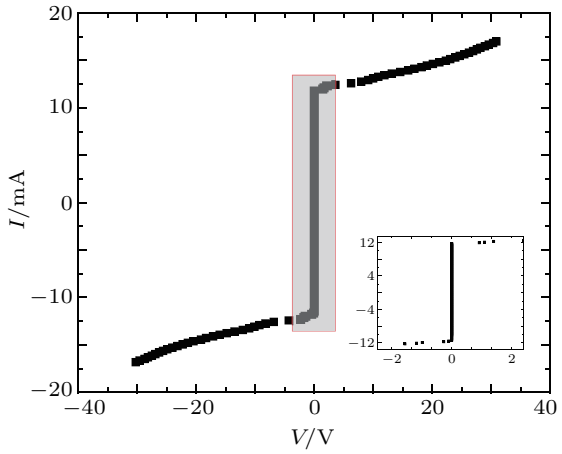


Fig. 6. The *I*–*V* curves of 100000 stacks consisting of 400000 junctions in series.

4. Conclusion and perspectives

Single stacks and large-scale arrays of stacks of Nb/(Nb$_x$Si$_{1-x}$/Nb)$_4$ JJs have been fabricated and measured. The junctions in one stack over the 2 inches substrates exhibit a uniform critical current. This result shows that JJ arrays can be designed and fabricated to output a higher quantum voltage. Further, the *I*–*V* curve of the junctions arrays containing 100000 stacks or 400000 junctions also exhibits a uniform shape and critical current. This study represents a breakthrough in the efforts toward realizing a higher voltage standard at NIM.

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