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Stress and strain analysis of Si-based III–V template fabricated by ion-slicing*

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Strain and stress were simulated using finite element method (FEM) for three III–V-on-Insulator (III–VOI) structures, *i.e.*, InP/SiO_2/Si, InP/Al_2O_3/SiO_2/Si, and GaAs/Al_2O_3/SiO_2/Si, fabricated by ion-slicing as the substrates for optoelectronic devices on Si. The thermal strain/stress imposes no risk for optoelectronic structures grown on InPOI at a normal growth temperature using molecular beam epitaxy. Structures grown on GaAsOI are more dangerous than those on InPOI due to a limited critical thickness. The intermedia Al_2O_3 layer was intended to increase the adherence while it brings in the largest risk. The simulated results reveal thermal stress on Al_2O_3 over 1 GPa, which is much higher than its critical stress for interfacial fracture. InPOI without an Al_2O_3 layer is more suitable as the substrate for optoelectronic integration on Si.

Keywords: III–VOI template, finite element method (FEM), critical thickness

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1. Introduction

The microelectronics industry had developed exponentially following the Moore's law,[1] until the 2010s when the technological challenge is overwhelming to continuing shrinking down the transistor node size. Moreover, the improvement of processor performance cannot keep proportional to the enlargement of the number/density of transistors,[2] and the ever decreasing size of the transistors leads to the emergence of quantum tunneling effects, and increased energy consumption. It has been widely accepted that the Moore's law has ended.[3] Silicon (Si) photonics is one of the most promising routes for "more than Moore" by utilizing photons instead of electrons to transmit and/or process information.[4] Under extensive research and investment, Si photonics has been developing rapidly and most of the optical/optoelectronic components, including the Si-based optical waveguides,[5] switches,[6] modulators,[7] detectors,[8] *etc.* have already been close to mature, leaving the light sources as the primary bottleneck since Si is an indirect bandgap semiconductor with very low light emission efficiency.

Extensive efforts have been put in inventing and developing Si-based light sources, especially lasers. Although lasers made from Si and other group IV semiconductors have achieved significant processes, such as the silicon Raman laser[9] and the GeSn laser,[10] they are still far from competing with the commercial GaAs and InP-based group III–V compound lasers. Direct mounting of processed laser, wafer bonding, and direct hetero-epitaxial growth of III–V template/devices on Si are the main-stream technologies to integrate III–V lasers on Si.[11] Direct mounting promises superior laser performances and good thermal dissipation, while the main problem is high precision alignment with Si waveguide and difficulty to realize high density integration. Monolithically growing III–V lasers directly on Si substrate is a straightforward technical route promising high density and low-cost lasers without complex processing procedures. For example, the Si-based InAs/GaAs quantum dot lasers have made tremendous progresses in recent years.[12] However, due to the crystal type, lattice constant and thermal expansion coefficient mismatches, the monolithic III–V lasers on Si commonly have a high density of structural defects, such as antiphase domains and dislocations, and face reliability and lifetime problems. Wafer bonding (including wafer-to-wafer and die-to-wafer bonding) is not subject to crystal type and lattice

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mismatch problems. Furthermore, the directly laser bonding to a Si circuit eliminates the alignment problem and allows a high integration density. Although complex fabrication processes are required for wafer bonding, it is the most successful technical route up to date.

Ion-slicing can be viewed as one type of wafer bonding technologies, by which, light element ions (*e.g.*, H, He) are first implanted into a III–V wafer, then, the III–V wafer is boned to a Si or Si-on-insulator (SOI) wafer, and finally the majority of the III–V wafer is split after post-annealing, resulting in a III–V thin film template on Si/SOI (III–VOI) wafer. Recently, our group has demonstrated high-quality 2-inch (1 inch = 2.54 cm) InP-on-insulator-Si (InPOI) wafers through a novel ion-slicing technique with sequential He and H ion implantation at room temperature.[13] The InPOI wafers were later used as substrates to grow optoelectronic devices by molecular beam epitaxy (MBE). Local delamination phenomenon was observed for certain samples after MBE growth. An Al_2O_3 layer was later introduced between the InP and the SiO_2 layer with the intention of improving adherence. GaAs-on-insulator-Si (GaAsOI) wafer was successfully demonstrated with the same technique (the results will be published elsewhere). After MBE growth, the delamination problem remains. Figure 1(a) shows an example of a GaAsOI surface with delamination after deoxidation at about 600 ℃. The materials involved in the III–VOI structures have different thermal expansion coefficients. The growth temperature in MBE is commonly between 400 ℃ and 700 ℃, which is far higher than the annealing temperature of typically 100 ℃–200 ℃ during the ion-slicing. Naturally, thermal strain/stress will be introduced during the heating processes and it is one of the most probable reasons to cause the delamination.

In this work, the strain/stress in three structures of InPOI and GaAsOI at an MBE growth temperature is modeled and simulated by finite element method (FEM). Different layers above the Si wafer show different strain/stress polarities while the absolute value always increases with temperature. The stress in the Al_2O_3 layer is found to be of the most potential risk. Some samples have been characterized and the simulations are in consistent with the experimental results.

2. Structures and simulations

Three material structures, shown in Figs. 1(b)–1(d) with the detailed layer information summarized in Table 1, have been studied in this work. Structure A is similar to the structure reported in Ref. [13], which is 450-nm ion-sliced InP thin film bonded on a SiO_2/Si substrate. The detailed fabrication process can be found in Ref. [13]. The major difference between structures B and A is that an additional Al_2O_3 layer is added between the SiO_2 layer and the III–V template layer to increase adherence. The III–V template layer of structure B1 is InP and that of B2 is GaAs. The detailed information on how to fabricate the B structures using low temperature ion-slicing will be published elsewhere. All structures have been utilized as substrates to grow III–V optoelectronic materials and devices by MBE. The III–VOI wafers were cut into 10 mm×10 mm pieces and adhered to 4-inch Si wafers by indium. During the deoxidation and epitaxy processes, the samples were heated to normal III–V MBE temperatures around 500 ℃–600 ℃. All samples exhibited delamination to different extents. Figure 1(a) shows an example of a B2 sample surface after deoxidation at 600 ℃ in MBE with rectangle-like shapes captured by optical microscope. This sample was later characterized by a JEOL scanning electron microscope (SEM) at 15 kV.

The heat transfer and strain/stress resulting from the differences in thermal expansion coefficients of each relevant layers in the three structures when heated to different temperatures in MBE were investigated by FEM. The three-dimensional (3D) material model of the three structures is shown in Figs. 1(b)–1(d). The simulated structure is square shaped with a side length of 10 mm which is the same as the real sample size for MBE growth. Heat transfer process and mechanics were both included to study the temperature and strain/stress distribution at different time and temperatures. The strain in the following context is defined as

$$\varepsilon = (a'(T) - a_1(T))/a_1(T), \tag{1}$$

where $a_1(T)$ is the free lattice constant at a designated temperature, T, and $a'(T)$ is the lattice constant at T after deformation caused by lattice mismatch. The stress is obtained correspondingly from the Hooke's law. Critical thickness of the epitaxial layer is estimated by the People–Bean (PB) model[14] as a result of the thermal mismatch.

Several assumptions are made to simplify the physical model and numerical simulations.

First, the materials involved in the study are assumed to be isotropic and obey the continuum elasticity theory. It has been shown that these assumptions provide high enough accuracy on strain/stress analysis for III–V structures even in nanoscale.[15,16]

Second, the initial strain/stress was assumed to be zero at room temperature in the whole structure. The bottom surface is constrained in a way that it can freely deform laterally while no deformation is allowed in the vertical direction. Thus, the situation that the bottom surface of the samples is adhered to a Si wafer is validly simulated.

Third, it should be noted that the III–VOI has a crystal/amorphous interface. This implies that the thin III–V film on SiO_2 or Al_2O_3 behaves like a free standing substrate template to some extent depending on the bonding strength at the

interface as well as the viscosity of the amorphous layer at the growth temperature. If it is a fully free standing template, it can be modeled as a compliant substrate[17] implying that the III–V template can expand/contract horizontally with respect to the underneath amorphous layer to accommodate the overall strain. In such a case, the generated threading dislocations upon strain relaxation will propagate downward terminating at the crystal/amorphous interface while the epitaxial structure above the template is free from threading dislocations and resumes high material quality. In this work, we assume the interface is rigid (equivalent to very strong bonding). The simulated temperature is lower than the glass transition temperatures of SiO_2 and Al_2O_3.[18] Therefore, the compliant effect is neglected and the III–VOI can be modeled in a similar way like a lattice mismatched heterostructure on a conventional crystal substrate.

Finally, we employ the PB model to estimate critical thickness of the epitaxial layers on III–VOI. The PB model is based on the energy balance between the strain energy (fully strained) and the dislocation energy (fully relaxed), and is not a thermodynamic model predicting the onset of initial strain relaxation by forming the first dislocation. The well-known Matthews–Blakeslee (MB) model[19] is based on the force balance to predict the onset of strain relaxation (thus critical thickness) and is equivalent to the thermodynamic model. The MB model predicts a much smaller value of critical thickness compared with that of PB model, and the difference increases for small misfit. During practical epitaxy, there exists a kinetic barrier for initial dislocations gliding to relax partial strain due to the limited growth temperature, and strain relaxation is delayed, in particular when the growth temperature is low. Therefore, it is possible to "extend" the critical thickness beyond the value predicted by the MB model at a reduced growth temperature. On the other hand, for any experimental tool to detect dislocations, there is always a resolution indicating the minimal detectable number of dislocations, *e.g.*, about 10^4 cm^{-2}–10^5 cm^{-2} for TEM. For the above reasons, the critical thicknesses predicted from the MB model has been found to fit experimental values for small misfit.[17] In this work, we use the MB model to estimate critical thickness since the strain induced by thermal mismatch is not big.

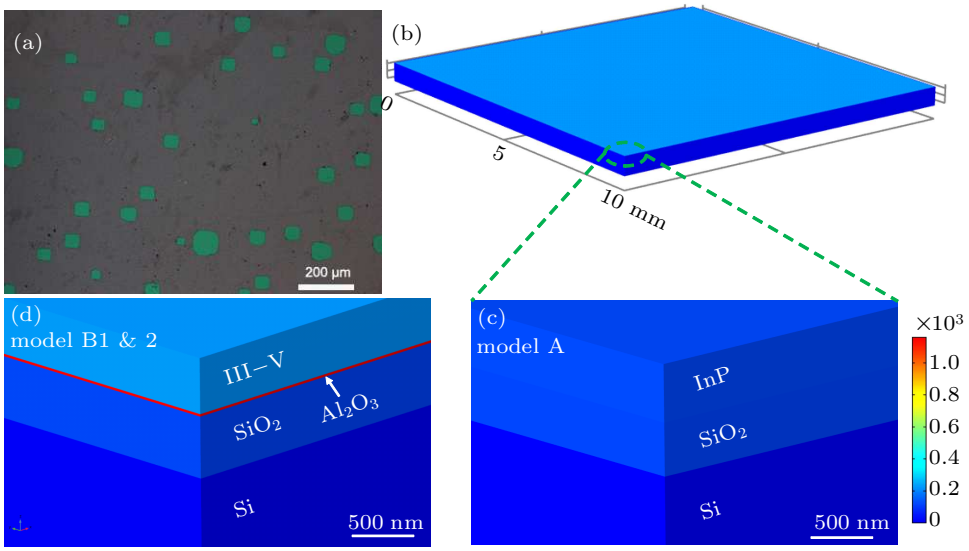


Fig. 1. (a) Optical microscope photo of a B2 sample surface with delamination after deoxidation at about 600 ℃. (b)–(d) 3D model of the three structures studied. Panels (b) is the overall structure and panels (c) and (d) are zoomed-in view of structure A and structure B1 & B2, respectively. The color indicates the absolute value of the stress component σ_{xx} at 600 ℃, and the III–V in panel (d) is taken from structure B2. The lateral dimension of the structure is 10 mm×10 mm. The layer thicknesses are summarized in Table 1 and some key material parameters in Table 2.

The properties of the single crystals involved in the study, *i.e.*, Si, GaAs, and InP are well determined while those for the dielectrics, *i.e.*, SiO_2 and Al_2O_3, vary depending on deposition methods and conditions. The ones in this simulation are chosen from the most common values of atomic layer deposition (ALD) deposited thin films close to our experiment condition.[20] The shear strain/stress components were found orders of magnitudes smaller than the in-plane ones. In the following sections, only the in-plane strain/stress components of $\varepsilon_{xx}/\sigma_{xx}$ are discussed, unless specified. When discussing the critical conditions, strain is commonly utilized for the single crystals, *i.e.*, Si, GaAs, and InP, while stress is usually mentioned for the dielectrics, *i.e.*, SiO_2 and Al_2O_3.

Table 1. Layer information of the three structures.

Structure	Si	SiO_2	Al_2O_3	III–V
A	500 μm	500 nm		450-nm InP
B1	500 μm	500 nm	20 nm	450-nm InP
B2	500 μm	500 nm	20 nm	450-nm GaAs

Table 2. Key material parameters utilized in the simulation.

Material	Coefficient of thermal expansion/10^{-6} K^{-1}	Thermal conductivity/(W/(m·K))	Young's modulus/GPa	Poisson ratio
Si	2.6	130	170	0.28
SiO_2	0.5	1.4	70	0.17
Al_2O_3	6.5	35	400	0.22
InP	4.6	68	61.1	0.36
GaAs	5.7	33	85.9	0.31

3. Results and discussions

3.1. Time domain analysis

Several heating and cooling processes will exist within one epitaxy round. The heating is provided by thermal radiation from the heater onto the backside of the substrate followed by thermal conduction and the temperature changing rate is one of the important factors to be considered in epitaxy programming. Therefore, the time dependent vertical temperature gradient in the wafer needs to be considered. Here, we study the heat transfer process in the III–VOI structure during a heating process. Structure A is taken as an example and the heating process is simplified by providing a constant temperature source at 600 ℃ at the bottom of the Si wafer.

Figure 2(a) shows the vertical temperature gradient within the structure A during the sudden heating process from room temperature to 600 ℃. In the beginning, a large temperature difference exists between the bottom and the top. The top temperature gradually increases and eventually the whole structure reaches thermal equilibrium. As it can be seen, the heat transfer process takes only about 4 ms–5 ms. During an epitaxial process in MBE or metalorganic chemical vapor deposition (MOCVD), the substrate temperature ramping rate is usually far less than 100 °C per minute, which corresponds to around 1 mK per ms. Therefore, even though the temperature is gradually increased during the heating process in epitaxy, the temperature across the whole substrate is almost under equilibrium at any time. The situation is very similar for all the structures since the thicknesses of other layers are significantly smaller than that of Si. Furthermore, it has been tested that the temperature of the substrate heater in the MBE is well regulated through a proportional-integral-derivative (PID) controller, and the temperature overshoot is within 1 °C for all tested heating rates. In later study, time is no longer considered as a factor.

Figure 2(b) shows the strain component ε_{xx} in each layer of the structure A. The strain in Si increases slightly since it is the absolute majority of the structure and basically free in deformation. The strain in SiO_2 is tensile and increases with a decreasing rate and finally saturates to a value of 0.12% after roughly 6 ms. The relatively long saturation time compared with that of Si is due to the very low thermal conductivity (almost two orders of magnitude smaller). The strain in InP is firstly tensile and increases with time before reaching a peak at around 0.3 ms and then decreases. It becomes negative (compressive) at 1.2 ms and eventually reaches a maximum value of about 0.11%. The initial tensile phase is due to the fact that the Si has a double thermal conductivity value compared with that of InP and is quickly heated and expanded, thus stretching the top InP layer, while the subsequent compressive phase originates from the larger thermal expansion coefficient of InP than that of Si when reaching thermal equilibrium. From the temperature transfer process, the strain in the layers reaches an equilibrium after around 6 ms.

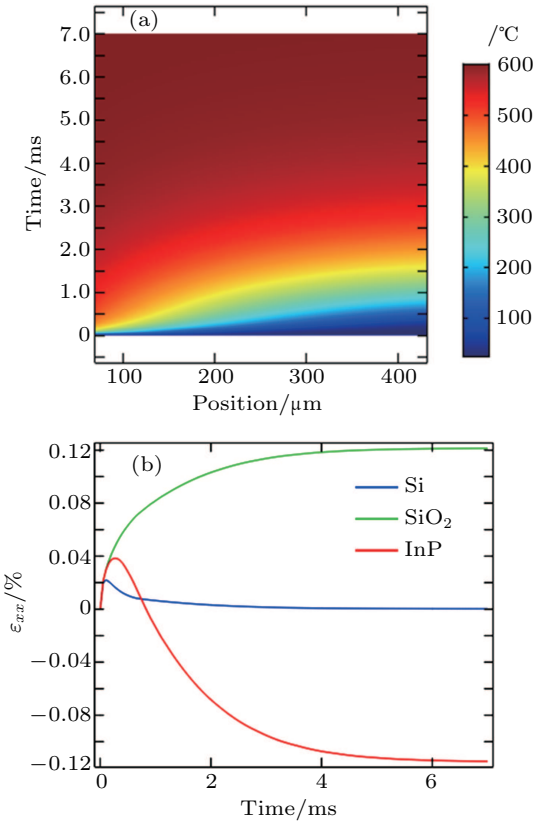


Fig. 2. (a) The chronicle vertical temperature gradient within the structure A and (b) the strain component ε_{xx} at the center of the layers *versus* time during heating process.

3.2. Strain and stress analyses for structure A

Growth temperature of 600 ℃ is slightly higher than the de-oxide temperature of GaAs substrate in MBE and is within the common growth temperature window of GaAs and AlGaAs, *etc*. In this section, the strain and stress in the structure

A at 600 ℃ is simulated. Figure 3(a) shows the distribution of the in-plane strain component ε_{xx} in the center cross section adjacent to the structure sidewall. An exaggerated deformation is employed to illustrate the relative strain in each layer. Figures 3(b) and 3(c) show the extracted lateral strain (ε_{xx}) and stress (σ_{xx}) profiles in the layers and panel (d) shows the vertical ε_{xx} profile far from the sidewall. The SiO_2 layer shrinks due to the tensile strain while the InP layer expands due to the compressive strain at the edge. Si is the majority of the structure, so it basically defines the final lateral lattice constant of the whole structure. SiO_2 has the smallest thermal expansion coefficient and therefore expands least. Both the InP and the Si layer will stretch it, resulting in tensile strain/stress. The InP has the largest thermal expansion coefficient leading to the largest lattice expansion and subsequently compressive strain/stress originated from the lower layers. The strain at the edge of all layers is found efficiently relaxed. The ε_{xx} distributes non-uniformly close to the edge due to deformation and becomes uniform about 2 μm from the edge which is also reflected from the ε_{xx} profile in Fig. 3(b). The max value of the in-plane strain component ε_{xx} in the InP layer is about 0.11%, which is a quite small value. The critical thickness of strain relaxation through generation of dislocation at such strain is estimated to be about 15 μm by the PB model.[14] Such a large critical thickness ensures little risk for strain relaxation in almost all optoelectronic devices including vertical-cavity surface-emitting lasers (VCSELs) and quantum-cascade lasers (QCLs) grown on InPOI. Figure 3(d) shows the ε_{xx} profile in the vertical direction through the center of the structure. The strain is uniform within the layers.

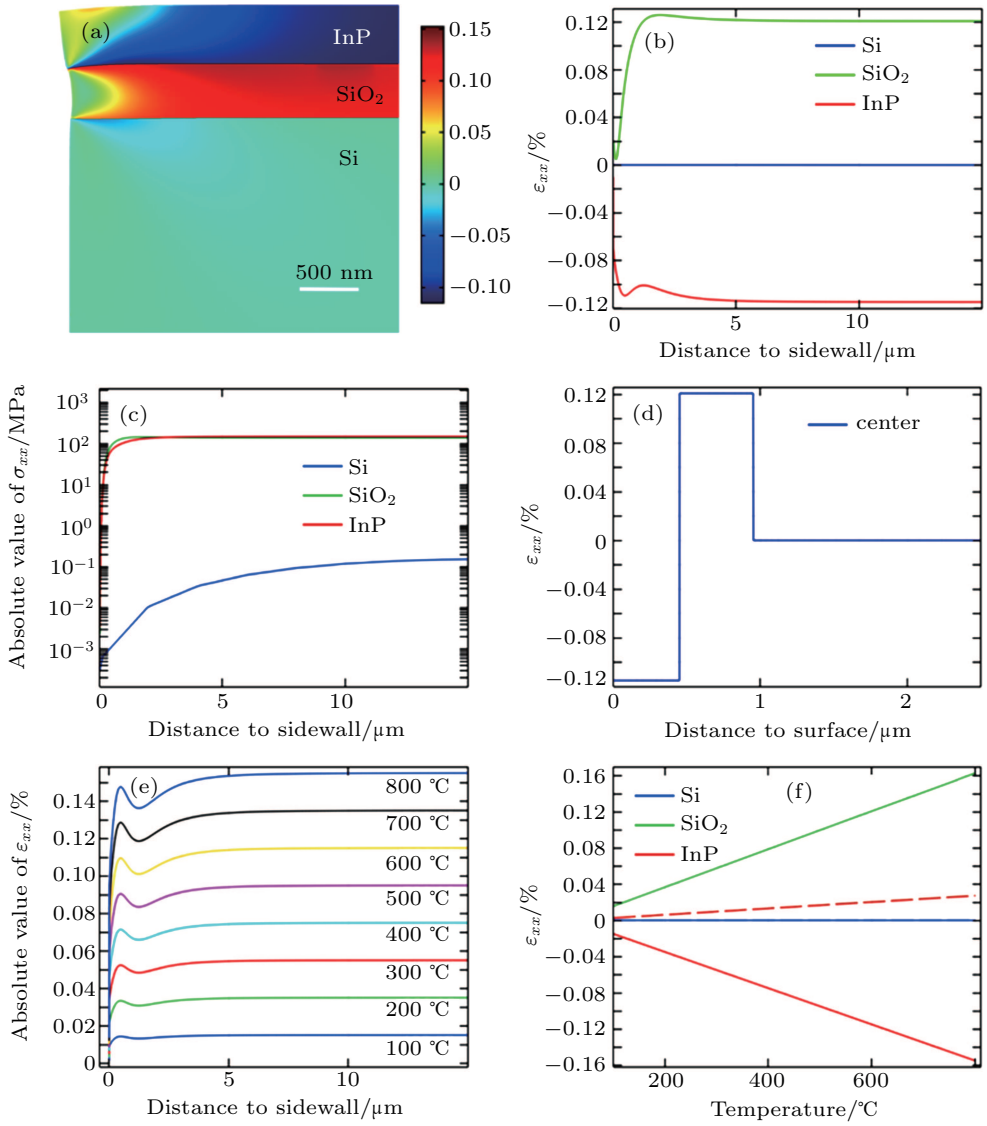


Fig. 3. Strain and stress analyses of structure A. (a) A slice of ε_{xx} distribution close to the sidewall, extracted from the center plane at 600 ℃. The deformation is exaggerated by 50 times. (b) and (c) Lateral ε_{xx} and σ_{xx} (absolute value) profiles close to the structure sidewall at 600 ℃, in the center (both vertically and in one of the lateral directions) of the SiO_2 and the InP layer and a depth of 20 μm in the Si layer. (d) Vertical ε_{xx} profile in the structure center at 600 ℃. (e) Lateral ε_{xx} profile in the InP layer at different temperatures adjacent to the sidewall. (f) ε_{xx} in the layers *versus* temperature. The solid curves are extracted from the layer center while the dashed lines are from the edge.

Figure 3(e) shows the lateral distribution of ε_{xx} (absolute value) in the InP layer at different temperatures. Again, the strain/stress is effectively relaxed at the structure edge at all temperatures. The strain in the center monotonically increases with temperature and reaches a value of about 0.14% at 750 ℃. The corresponding critical thickness is estimated to be around 8 μm, which is enough for edge emitting lasers while risky for VCSELs and QCLs. 750 ℃ is above the normal growth temperatures of all GaAs and InP-based III–V materials in MBE. However, it is a common growth temperature for MOCVD,[21] indicating that chance of strain relaxation is large when growing thick devices, such as VCSELs and QCLs by MOCVD.

Figure 3(f) shows the ε_{xx} within the layers under different temperatures. All of them are linearly dependent on temperature. The strain in the SiO_2 and the InP layer has the opposite sign but similar value. The stress in SiO_2 is 137 MPa at 800 ℃, much lower than the tensile strength of SiO_2 in vacuum which is above 1 GPa,[22] indicating no risk in the SiO_2 layer.

3.3. Comparison of the three structures

An Al_2O_3 layer was added between the SiO_2 and the InP layer for structure B1 with the aim of increasing the adherence. The procedure was also implemented for the structure B2 of a GaAsOI template. The effect of this Al_2O_3 layer on strain and stress under MBE growth temperature is investigated. Figure 4(a) shows the distribution of ε_{xx} in a center slice adjacent to the structure sidewall for structure B1. An exaggerated deformation is employed to illustrate the relative strain in each layer. Similar to structure A, the strain is non-uniform at the edge while becomes uniform far into the structure. The Al_2O_3 layer is under relatively larger compressive strain than that of InP, while the stress in the Al_2O_3 layer is unexpectedly high as seen in Fig. 4(b) as well as Fig. 1(d), due to not only the largest thermal expansion coefficient of Al_2O_3, but also the several times larger Young's modulus compared with those of Si. At the normal MBE growth temperature of 600 °C, it reaches over 1 GPa.

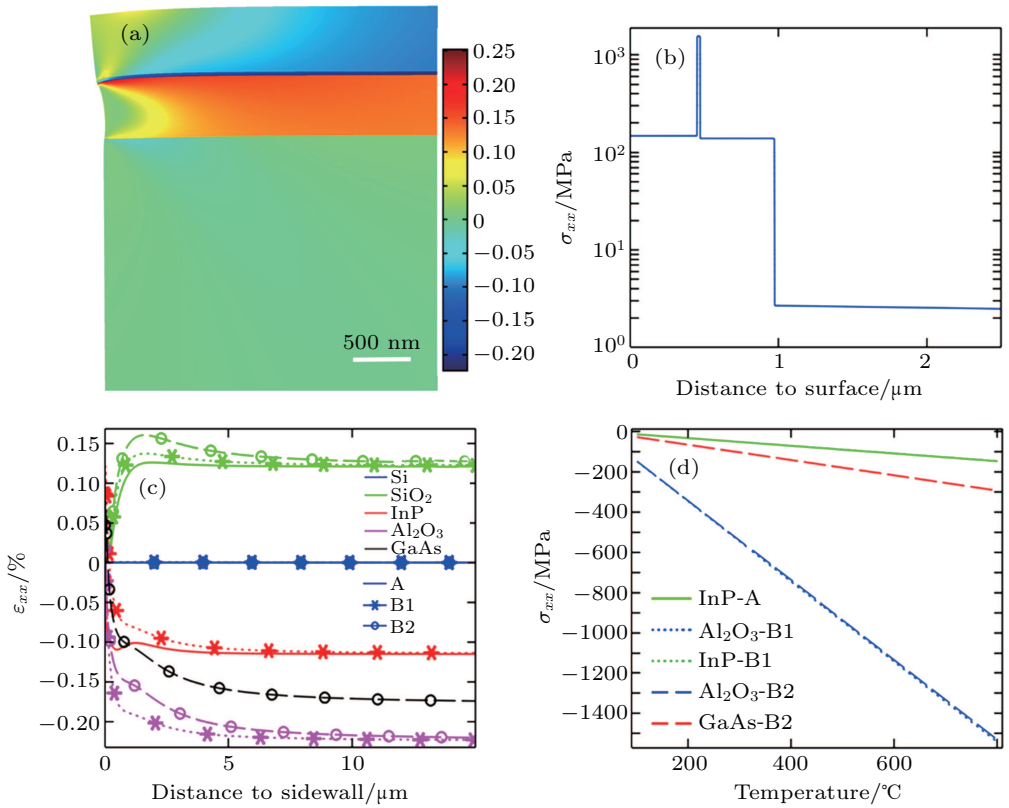


Fig. 4. (a) A slice of ε_{xx} distribution close to the sidewall, extracted from the center plane of structure B1 at 600 ℃. The deformation is exaggerated for 50 times. (b) Vertical σ_{xx} profile adjacent to the surface, extracted from the center of structure B1 at 600 ℃. (c) Lateral ε_{xx} profile in the layers in different structures adjacent to the sidewall at 600 ℃. The layers are labeled by material and color, as follows, Si (blue), SiO_2 (green), InP (red), Al_2O_3 (magenta), and GaAs (black); while the structures are differentiated by line style/markers, as follows, A (solid curve, no marker), B1 (dotted curve & star marker), and B2 (dashed curve & circle marker). (d) σ_{xx} in the III–V and Al_2O_3 layers in different structures *versus* temperature. Some curves of the same material in different structures almost overlap.

Figure 4 (c) shows the lateral ε_{xx} profile in the layers in different structures adjacent to the sidewall at 600 ℃. Thanks to the addition of the Al_2O_3 layer, larger strain is found in the SiO_2 layer in the structures B1 & B2 than in the structure A adjacent to the edge. The InP layer shows similar strain in all structures. The GaAs layer possesses larger strain of 0.18% than InP due to the larger thermal expansion coefficient. The Al_2O_3 layer has the largest strain. The difference of the strain

in Al_2O_3 layer between the structures B1 and B2 is marginal. Figure 4(d) compares the stress only for the III–V and the Al_2O_3 layers in all three structures. As shown in the figure, the GaAs layer possesses larger stress compared with InP. Again, the Al_2O_3 layer shows several times higher stress at all temperatures and the higher temperature the larger deviation.

The strain in the GaAs layer reaches 0.18% and 0.21% at 600 ℃ and 750 ℃, respectively. The critical thickness reduces to about 6 μm and 4 μm, respectively. Therefore, the GaAs layer is potentially risky for growth of many optoelectronic devices when using the GaAsOI as substrate in both MBE and MOCVD.

Lyytinen *et al.* systemically measured the interface strength of ALD deposited Al_2O_3 layers on Si.[20] The critical stress for interfacial fracture is a few tens of MPa for all studied samples under different deposition conditions. The Al_2O_3 layer thickness in our model is thin and the dependence of the critical stress on thickness is not well established. Berdova proposes a $(1/h)^{1/2}$ dependence,[23] where h is the layer thickness. Then the critical interfacial fracture stress in our Al_2O_3 layer is roughly estimated to be around 100 MPa. The simulated stress in the Al_2O_3 layer reaches 1 GPa. Though the accuracy of the critical stress estimation is low, the stress in the Al_2O_3 layer is of high risk to cause fracture at the interfaces with the III–V layer or the SiO_2 layer.

The stress in the Al_2O_3 layer is roughly 1/3 of the critical value of buckling under compressive strain.[24] Therefore, the risk of buckling within the Al_2O_3 layer is low.

A sample of structure B2 was annealed to 600 ℃ in MBE and then characterized by microscope, SEM and TEM. A microscope photo showing the surface with delamination and a detailed observation of the delaminated region by SEM are shown in Fig. 5. It can be seen from Figs. 5(a) and 1(a) that the delaminated regions have rough rectangular shapes indicating crystal orientation dependence. Figure 5(a) shows that there is a region adjacent to the sample edge free of delamination, which may be a result of strain relaxation. It is evident that the delamination happens in the GaAs layer. The factor that the stress in the Al_2O_3 exceeds the critical stress for interfacial fracture could be an explanation for the delamination which originates from the GaAs/Al_2O_3 interface.

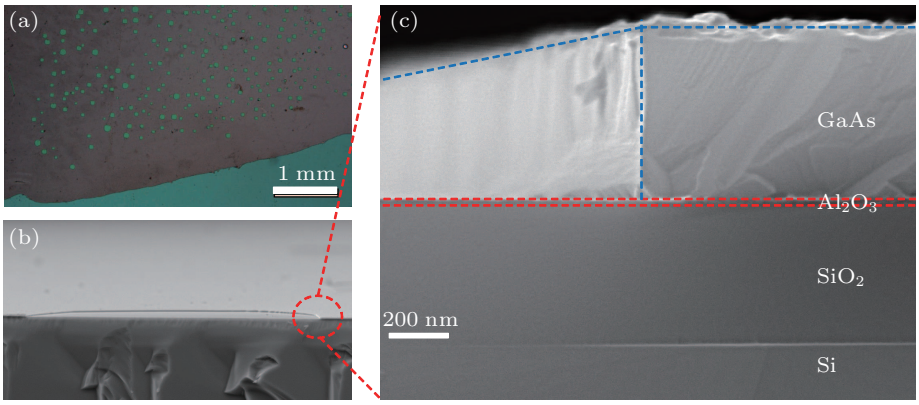


Fig. 5. (a) Optical microscope photo of a structure B2 sample surface close to the sample edge showing delamination after deoxidation at about 600 °C. (b) SEM image of the same sample cleaved through one of the delamination regions and panel (c) is a zoomed-in image at the corner with the layers labeled.

4. Summary

In summary, strain and stress analyses were carried out for three III–VOI structures fabricated experimentally by ion-slicing as the substrate for the growth of optoelectronic devices on Si. The thermal strain/stress in InPOI at normal MBE growth temperature imposes basically little risk for all optoelectronic devices and some risk for thick devices like VCSEL and QCL if grown by MOCVD. GaAsOI is more risky than InPOI with a critical thickness of about 6 μm and 4 μm at 600 ℃ and 750 ℃, respectively. The Al_2O_3 layer was intended to increase the adherence while it brings in the largest risk. The stress in Al_2O_3 is over 1 GPa which is much higher than the critical stress for interfacial fracture. InPOI without Al_2O_3 layer (structure A) is more suitable among the three structures as the substrate for the growth of Si-based laser or the platform for optoelectronic integration on Si.

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