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Experimental evaluation of interface states during time-dependent dielectric breakdown of GaN-based MIS-HEMTs with LPCVD-SiN_x gate dielectric*

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We experimentally evaluated the interface state density of GaN MIS-HEMTs during time-dependent dielectric breakdown (TDDB). Under a high forward gate bias stress, newly increased traps generate both at the SiN_x/AlGaN interface and the SiN_x bulk, resulting in the voltage shift and the increase of the voltage hysteresis. When prolonging the stress duration, the defects density generated in the SiN_x dielectric becomes dominating, which drastically increases the gate leakage current and causes the catastrophic failure. After recovery by UV light illumination, the negative shift in threshold voltage (compared with the fresh one) confirms the accumulation of positive charge at the SiN_x/AlGaN interface and/or in SiN_x bulk, which is possibly ascribed to the broken bonds after long-term stress. These results experimentally confirm the role of defects in the TDDB of GaN-based MIS-HEMTs.

Keywords: GaN-based MIS-HEMTs, gate dielectric, time-dependent dielectric breakdown, interface states

PACS: 72.80.Ey, 72.80.Sk, 73.20.At, 77.22.Jp **DOI:** 10.1088/1674-1056/ab8895

1. Introduction

GaN-based transistors on Si substrate emerged as promising candidates for high voltage, high frequency, and high power applications.[1] Especially, GaN-based metal–insulator–semiconductor (MIS) high electron mobility transistors (MIS-HEMTs) have attracting wide attention owing to the low gate leakage and large gate swing.[2–4] Nevertheless, the reliability issue of MIS-HEMTs caused by the introduction of gate insulator layer is still a major challenge before its commercialization.

One of the most critical gate reliability issues of MIS-HEMTs is the time-dependent dielectric breakdown (TDDB). To concentrate the electric-field in the gate stack, forward constant voltage stress (CVS) TDDB experiments have been conducted to evaluate the gate robustness of MIS-HEMTs.[5–9] Besides, Simon *et al.* investigated the dependence of the dielectric breakdown by forward biased constant current stress (CCS) TDDB measurements.[10] Until now, most of the previous literatures focus on using the catastrophic failure time to evaluate the lifetime of different gate structures, such as the thickness of the dielectric and AlGaN barrier,[6] the area scaling,[7] and the gate electrode.[10] Generally, it is accepted that newly increased traps will occur randomly in the gate stack by prolonging the high-voltage or current gate stress and eventually result in a catastrophic failure. However, there is rarely experimental evaluation to confirm this possible mechanism. In particular, the GaN-based MIS-HEMTs contain multiple layers and several interfaces, which complicates the physical origin of the time-dependent gate degradation.[11–13] Thus, in order to improve the gate reliability of GaN-based MIS-HEMTs effectively, a comprehensive gate degradation analysis of MIS-gate structure is very necessary.

In this paper, forward constant gate bias stress was conducted in low-pressure chemical vapor deposition (LPCVD) SiN_x/AlGaN/GaN MIS-HEMTs to analyze the time-dependent interface state variation. Moreover, the understanding of gate degradation can provide reference for normally-off MISFETs with dielectric and thin AlGaN barrier layer.[14] The first section of this paper analyzed the gate leakage mechanism under forward bias through temperature-dependent gate current characteristics. Then, the gate degradation during the electric-field-accelerated TDDB experiment was discussed to determine the stress voltage and duration. Finally, a series of stress-time-dependent experiments were de-

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veloped to understand the interface state variation, including current–voltage (I–V) and capacitance–voltage (C–V) characterizations.

2. Device structure and fabrication process

The devices were fabricated on 6-inch (1 inch = 2.54 cm) Si substrate by an industry standard complementary metal–oxide–semiconductor (CMOS) process. The cross-sectional schematic diagram of LPCVD-SiN_x/AlGaN/GaN MIS-HEMT is shown in Fig. 1(a). The epitaxial structure was grown by the metal organic chemical vapor deposition on Si (111) substrate, which consists of a 4-μm GaN buffer layer, a 300-nm GaN channel layer, a 0.7-nm AlN space layer, a 25-nm $Al_{0.25}Ga_{0.75}N$ barrier layer, and a 2-nm GaN cap layer. The device fabrication started with the mesa etching, then, a 35-nm-thick SiN_x layer was deposited by LPCVD both as the surface passivation layer and the gate insulator. Afterwards, a 500-nm SiO_2 passivation layer was deposited by plasma-enhanced chemical vapor deposition. Source/drain ohmic contacts were formed with Ti/Al/Ti/TiN metal stack after recessing the SiO_2 passivation layer, the SiN_x gate insulator, and 20-nm AlGaN barrier layer consecutively. Then, the gate window was defined by a combination of SF_6 low-power ICP etching (down to a thickness of 50 nm) and BHF wet etching. The wet etching automatically stopped at the Si_3N_4 surface due to the extremely high selectivity between SiO_2 and SiN_x. TiN/Ti/Al was deposited as gate metal. After the deposition of thick metal and last passivation layer which consists of SiO_2 and SiN_x, the device with multi-finger was formed as shown in Fig. 1(b), featuring a dimension of $L_{GD}/L_{GS}/L_G/W_G$ = 10 μm/5 μm/1.5 μm/25 mm.

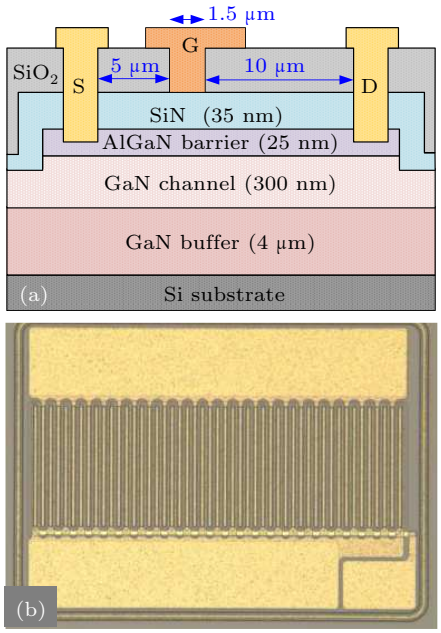


Fig. 1. Schematic structure (a) and optical image (b) of the multi-finger GaN-based MIS-HEMT using LPCVD-SiN_x as gate dielectric.

3. Results and discussion

3.1. The gate leakage mechanism and TDDB measurements

Figure 2 shows the typical transfer and output characteristics of the LPCVD-SiN_x/AlGaN/GaN MIS-HEMTs. The device exhibits a high on/off current ratio of 10^9 and a small subthreshold swing of 87 mV/decade, implying the excellent gate control ability. The threshold voltage (V_{th}) is approximately −10 V at drain current of 10 μA/mm and drain voltage (V_{DS}) of 1 V. The hysteresis of V_{th} is approximately 0.9 V at the maximum sweep gate voltage (V_{GS}) of 10 V. On-resistance was calculated to be 15 Ω·mm and the maximum output current is 375 mA/mm at V_{DS} of 10 V and V_{GS} of 4 V. The relatively higher on-resistance can be further optimized by reducing the L_{GS}. Under a V_{DS} of 0 V, the forward gate breakdown voltage (V_{GS_max}) was measured to be 45 V owing to the high quality of LPCVD-SiN_x layer (not shown). The corresponding breakdown electric-field strength in LPCVD-SiN_x was estimated to be approximately 11.4 MV/cm.

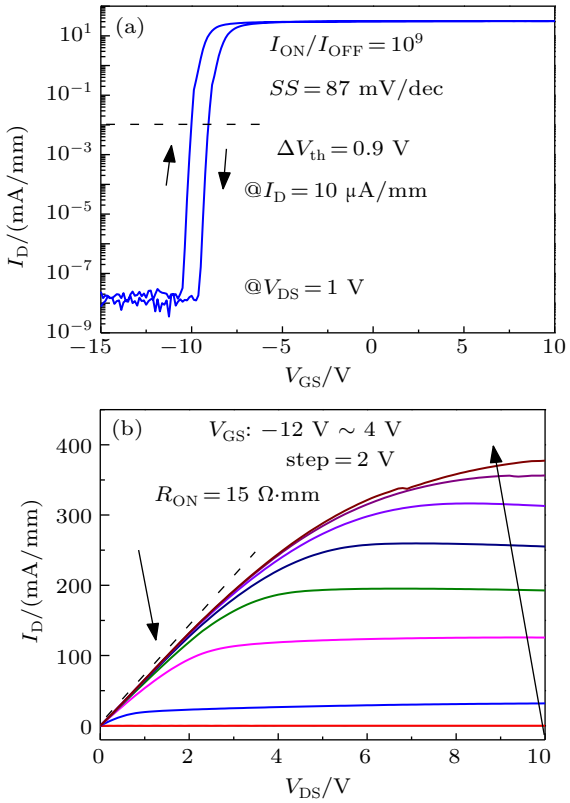


Fig. 2. Transfer (a) and output (b) characteristics of the LPCVD-SiN_x/AlGaN/ GaN MIS-HEMTs.

The temperature-dependent gate leakage current (I_G–V_{GS}) curves measured on the AlGaN/GaN MIS-HEMTs are shown in Fig. 3(a). Under relatively high forward gate bias, the gate leakage current increases obviously with temperature and gate bias. The energy band diagram of LPCVD-SiN_x/AlGaN/GaN MIS-gate structure was simulated under different forward gate biases (Fig. 4). As the gate voltage increases, the potential

drop mainly occurs in the dielectric and decreases the barrier height continuously, resulting in a triangular barrier at the LPCVD-SiN$_x$/AlGaN interface. When V_{GS} is higher than 5 V, the conduction band of AlGaN is pulled down below the Fermi level at the LPCVD-SiN$_x$/AlGaN interface. This means that the two-dimensional electron gas (2DEG) will spill over the 2DEG channel and accumulate at the LPCVD-SiN$_x$/AlGaN interface. Then, with the assistance of relatively high forward electric-field and temperature, the electrons at the LPCVD-SiN$_x$/AlGaN interface can transfer to the gate electrode and increase the leakage current.[15]

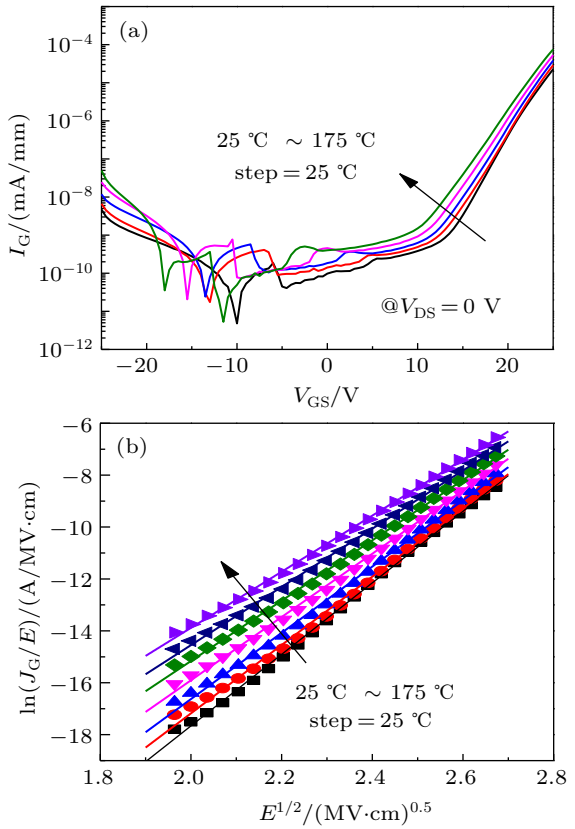


Fig. 3. Temperature-dependent I_G–V_{GS} characteristics (a) and the corresponding Poole–Frenkel plots (b) of the LPCVD-SiN$_x$/AlGaN/GaN MIS-HEMT.

There are several gate leakage mechanisms for GaN-based MIS-gate structure. For example, thermionic emission, Poole–Frenkel (PF) emission, Fowler–Nordheim tunneling, and trap-assisted tunneling. According to our test results, when V_{GS} is higher than 15 V, the gate leakage current depends on both gate bias and temperature, suggesting that the PF emission may be the dominating mechanism under relatively high gate bias. The PF emission can be expressed as the following formula[16]

$$J_{PF} = qn_0\mu E_{ox}\exp\left(-\frac{q(\varphi_t - \sqrt{qE_{ox}}/\pi\varepsilon_s)}{kT}\right), \quad (1)$$

where E_{ox} is the electric-field strength in LPCVD-SiN$_x$ dielectric, φ_t is the barrier height for the electron emission from the trap state, ε_s is the dielectric constant, μ and n_0 are the electron drift mobility and the carrier density, respectively. Equation (1) can be rearranged as

$$\ln\left(\frac{J_{PF}}{E_{ox}}\right) = A\sqrt{E_{ox}} + B, \quad (2)$$

$$A = \frac{q}{kT}\sqrt{\frac{q}{\pi\varepsilon_s}}, \quad (3)$$

$$B = -\frac{q\varphi_t}{kT} + \ln(qn_0\mu). \quad (4)$$

The plots of $\ln(J_{PF}/E_{ox})$ *versus* $\sqrt{E_{ox}}$ yield straight lines as shown in Fig. 3(b). The dielectric constant ε_s and trap energy are calculated to be 6.7 and 0.75 eV according to Eqs. (3) and (4), respectively. Those values are comparable with the previous reports,[16–19] indicating that the PF emission mechanism (a traps-assistant emission process) dominates the dielectric leakage under relatively high forward gate bias.

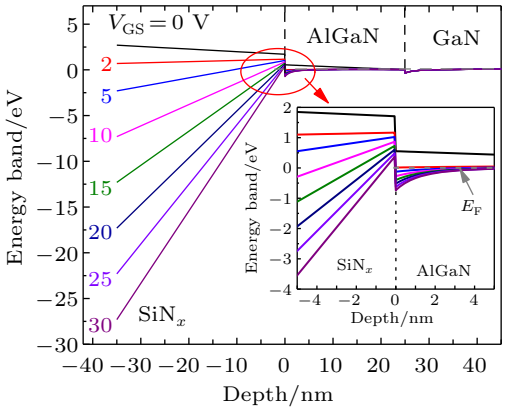


Fig. 4. The simulated energy band diagram of the LPCVD-SiN$_x$/AlGaN/GaN MIS-structure under different forward gate biases.

Finally, an effective method to evaluate the gate reliability is the TDDB test. Herein, the forward gate bias TDDB measurements on LPCVD-SiN$_x$/AlGaN/GaN MIS-HEMTs were conducted at room temperature with three different gate biases of 30 V, 32 V, and 34 V (around 70%–80% of V_{GS_max}, ten devices per group), while source and drain were grounded, respectively. The gate leakage current was monitored during the stress experiment as shown in Fig. 5(a). It was found that the leakage decreases firstly because the accumulated electrons under the gate can suppress the gate leakage current. Then, the leakage current increases and fluctuates before catastrophic failure, which is attributed to the newly increased traps and the gradual formation of the percolation path in the gate stack after a certain stress time.[6] These results indicate that the gate degradation is a time-accumulated process, which is consistent with previous reports.[6,20] After the percolation path formed, the gate leakage current shows a sudden increasing, and the time-to-breakdown (t_{BD}) is defined when gate leakage current is higher than 0.1 mA/mm. Figure 5(b) plots the Weibull distribution of the t_{BD} with a Weibull slope of $\beta = 4$, suggesting an excellent device uniformity.

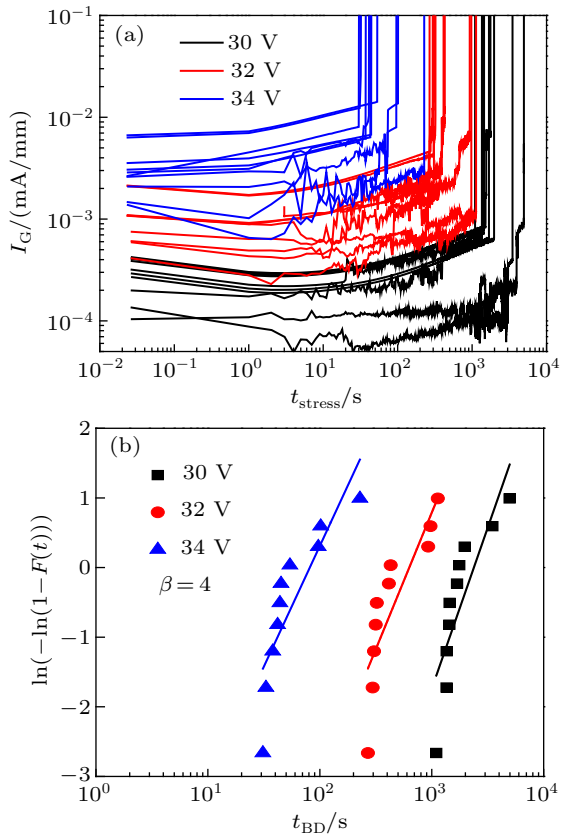


Fig. 5. (a) The gate leakage current monitored with three different gate voltages during TDDB measurements. (b) The Weibull distribution of the t_{BD}.

3.2. Effect of time-dependent gate stress on the device characteristics

In order to deeply understand the effect of forward gate bias stress on the interface state density, a time-dependent stress experiment was used based on the TDDB results. The test process is shown in the inset of Fig. 6, where a constant gate bias of 30 V was applied while the source and drain were grounded. The stress was interrupted after different stress times to monitor the gate degradation, including *I*–*V* and *C*–*V* characteristics. Figure 6 plots the gate leakage variation during the whole stress experiment. The stable output characteristics suggest that the degradation mainly occurs in the LPCVD-SiN_x dielectric, instead of in the AlGaN/GaN heterojunction [Fig. 7(a)]. The V_{th} in transfer curves shows large initial positive shift followed by a small negative shift (from 1 to 2 to 3) as shown in Fig. 7(b). The positive shift has been reported by other authors,[21,22] which is caused by the filling of pre-existing traps both at SiN_x/AlGaN interface and in SiN_x bulk layer.

Frequency conductance method (with frequency from 1 kHz to 100 kHz) was performed to estimate the traps density at LPCVD-SiN_x/AlGaN interface (D_{it}) during the gate stress.[23] The G_p/ω–ω curves for the samples before and after 5000-s forward gate bias stress were recorded at selected bias in the deep accumulation region calculated from the second increase step of *C*–*V* curves (not shown). It can be observed that the G_p/ω peak shifts to the higher frequency side along with an increasing amplitudes, indicating the increase of D_{it} after gate stress. Figure 8(a) plots the variation of D_{it} *versus* $E_C - E_T$ during the time-dependent degradation. It is found that the D_{it} increases obviously with the increasing stress time, especially at the relatively smaller $E_C - E_T$ region. The D_{it} integrated from $E_C - 0.34$ eV to $E_C - 0.4$ eV increased by two times as shown in Fig. 8(b).

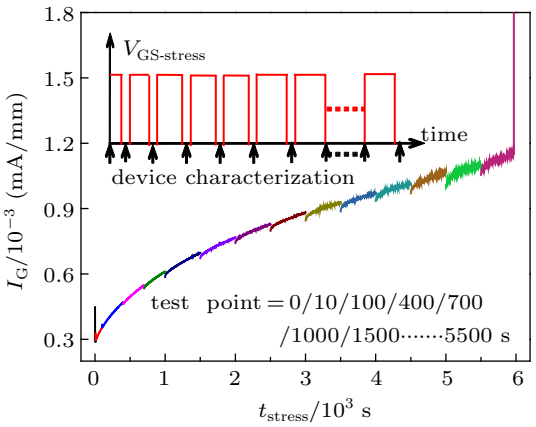


Fig. 6. The gate leakage variation during the whole stress experiment. Inset: the test process of the typical stress experiment, including stress interruption and device characterization.

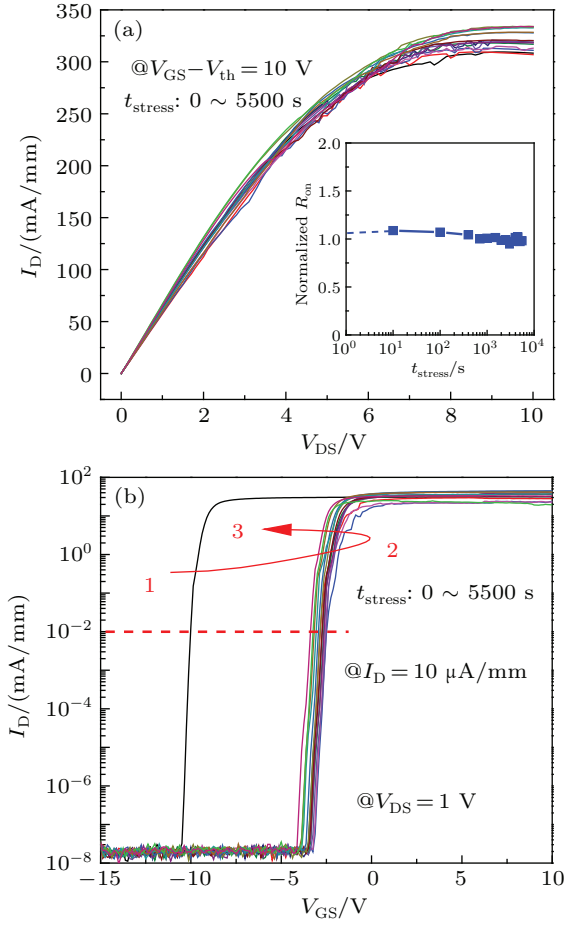


Fig. 7. Monitored output characteristics (a) and transfer characteristics (b) during the gate stress. Inset: on-resistance variation extracted from the output characteristics.

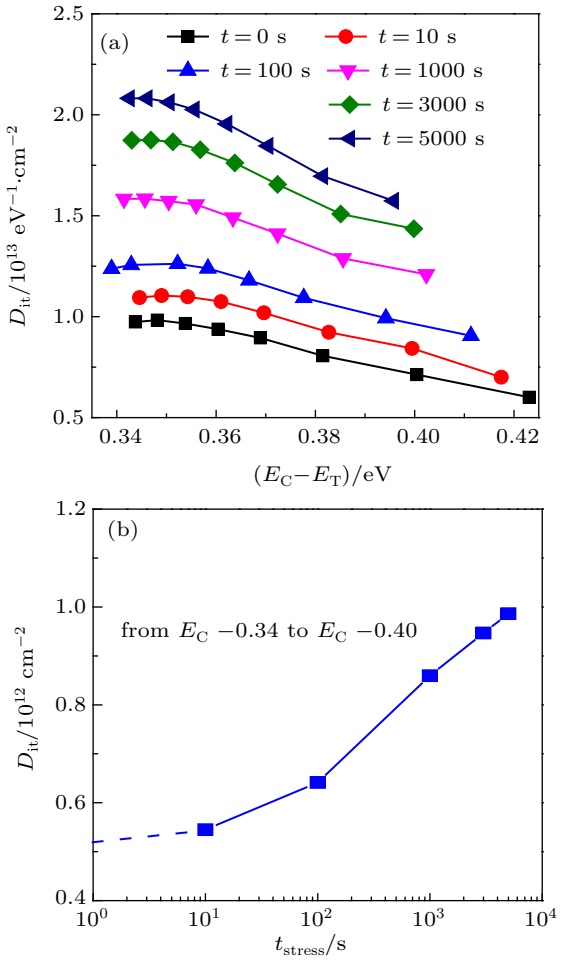


Fig. 8. The evolution of D_{it} *versus* E_C–E_T (a) at different stress time and the corresponding D_{it} integrated from E_C–0.34 eV to E_C–0.4 eV (b) during the gate degradation.

Double sweep *C*–*V* measurements were also conducted at each test point to evaluate the variation of trap density during gate gradation. In order to avoid *C*–*V* curves clutter, only three double sweep *C*–*V* curves at test points of $t = 0$ s, 10 s, 5500 s are shown in Fig. 9(a). The first increase step in *C*–*V* curve represents the formation of 2DEG at AlGaN/GaN interface. With the gate voltage further increases to turn on voltage (V_{on}), the 2DEG will spill over the 2DEG channel and accumulate at the LPCVD-SiN$_x$/AlGaN interface, leading to the second increase step in *C*–*V* curve. This result is consistent with the conduction bands diagram of AlGaN at LPCVD-SiN$_x$/AlGaN interface under forward gate bias as shown in Fig. 4. Considering the initial large positive shift in V_{th}, the gate sweep voltage of *C*–*V* curves ranged from −15 V to 10 V for the fresh sample while changed into −9 V to 16 V during stress.

The hysteresis of V_{on} is attributed to both LPCVD-SiN$_x$/AlGaN interface states and LPCVD-SiN$_x$ dielectric bulk traps (D_{bt}), owing to the large maximum gate voltage in double sweep *C*–*V* measurements.[24] The traps density and increment of traps density can be respectively estimated according to

$$D = \frac{C_{ox} V_{hysteresis}}{q}, \tag{5}$$

$$\Delta D = \frac{C_{ox} \Delta V_{hysteresis}}{q}, \tag{6}$$

where D represents the density of interface states or/and bulk traps in LPCVD-SiN$_x$ layer, C_{ox} is capacitance of LPCVD-SiN$_x$ layer ($C_{ox} = 250$ nF/cm^2), $V_{hysteresis}$ is V_{on} hysteresis, ΔD and $\Delta V_{hyterisis}$ are the increment of traps density and V_{on} hysteresis. Figure 9(b) plots the ΔD *versus* stress time, as estimated by frequency conductance method and the V_{on} hysteresis in double sweep *C*–*V* curves, respectively. At the initial stage of gate degradation, the increment of $D_{it} + D_{bt}$ calculated from V_{on} hysteresis in *C*–*V* curves [Eq. (6)] is smaller than that of D_{it} estimated by frequency conductance method. The possible reason is that the measured V_{on} hysteresis in dc-mode strongly depends on the sweep rate, thus, the density of interface traps and bulk traps could be underestimated. After stress for a long time, the increment of $D_{it} + D_{bt}$ is significantly larger than that of D_{it}, indicating that the dielectric bulk traps generation dominate the gate degradation.

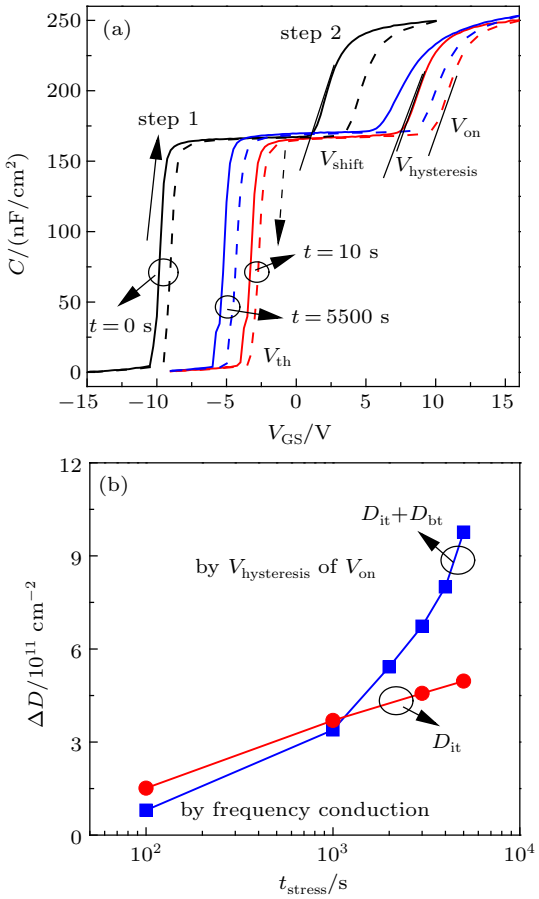


Fig. 9. (a) Double sweep *C*–*V* curves at test point $t = 0$ s, 10 s, 5500 s. Panel (b) is the increment of traps density estimated by frequency conductance method and the voltage hysteresis of double *C*–*V* curves, separately.

Besides, it worth noting that a slowly negative shift of V_{th} and V_{on} in *C*–*V* curves is observed after the firstly positive shift caused by electron trapping, which is consistent with Fig. 7(b). As analyzed above, the newly generated traps are mainly in the gate stack. Therefore, a possible reason for the negative

shift of V_{th} and V_{on} may be ascribed to the broken bonds at the LPCVD-SiN$_x$/AlGaN interface and/or in LPCVD-SiN$_x$ layer, which will cause the accumulation of positive charge.[25]

To further investigate the effect of newly increased traps on the gate leakage current, the I_G–V_{GS} curves were also extracted during the gate degradation as shown in Fig. 10. The gate leakage current does not show significantly increase before eventually breakdown. Especially, for relatively high forward gate bias, the gate leakage increase more obviously than other gate voltage region, which is consistent with gate leakage mechanism.

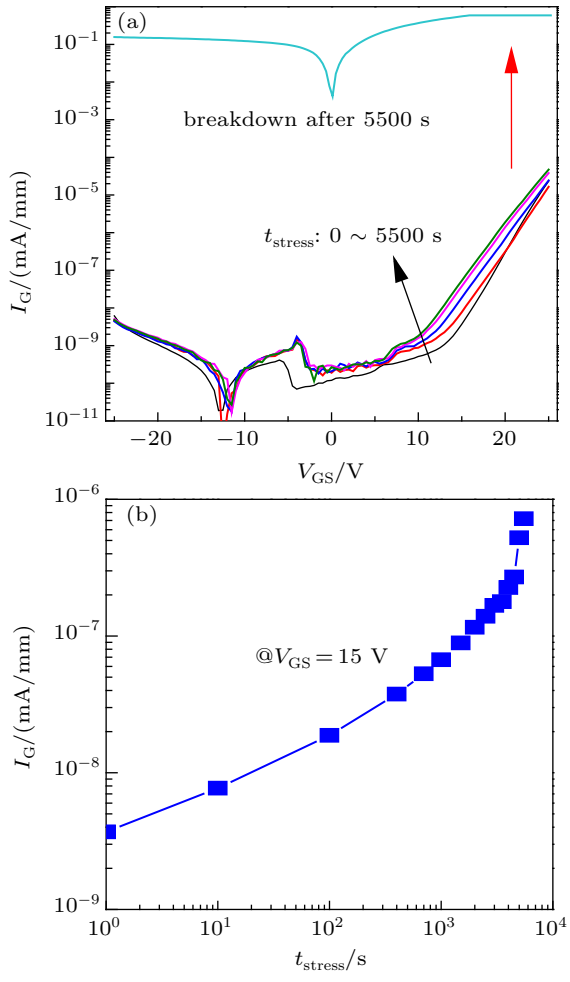


Fig. 10. (a) The gate leakage characteristics measured during gate degradation. (b) The evolution of gate leakage current at V_{GS} = 15 V was extracted from I_G–V_{GS} curves during the degradation.

Finally, by introducing UV light illumination experiments (wavelength = 365 nm), the generation of positive charge at the LPCVD-SiN$_x$/AlGaN interface and/or in LPCVD-SiN$_x$ layer was verified. Before the forward gate bias stress, the device was illuminated with UV light for ten minutes. There is no obvious difference in V_{th} and V_{on} before and after UV light illumination, which is owing to the high interface quality of LPCVD-SiN$_x$/AlGN. Then, the constant gate bias stress with V_{GS} = 30 V was applied to accelerate the gate degradation. The transfer characteristics and *C*–*V* curves were monitored during the stress, and the test process is same with that shown in the inset of Fig. 6. Before catastrophic failure (after 3300-s stress time), the device was grounded and illuminated with UV light for one hour and the recovery phenomenon was characterized. The test results of *C*–*V* curves are shown in Fig. 11. Obviously positive shift in V_{th} and V_{on} followed by a slow negative shift can also be observed (from 1 to 2 to 3). In particular, after one hour UV light illumination, there is an additional negative shift in V_{th} and V_{on} (from 3 to 4), which could be attributed to the accumulation of positive charge in the gate stack.

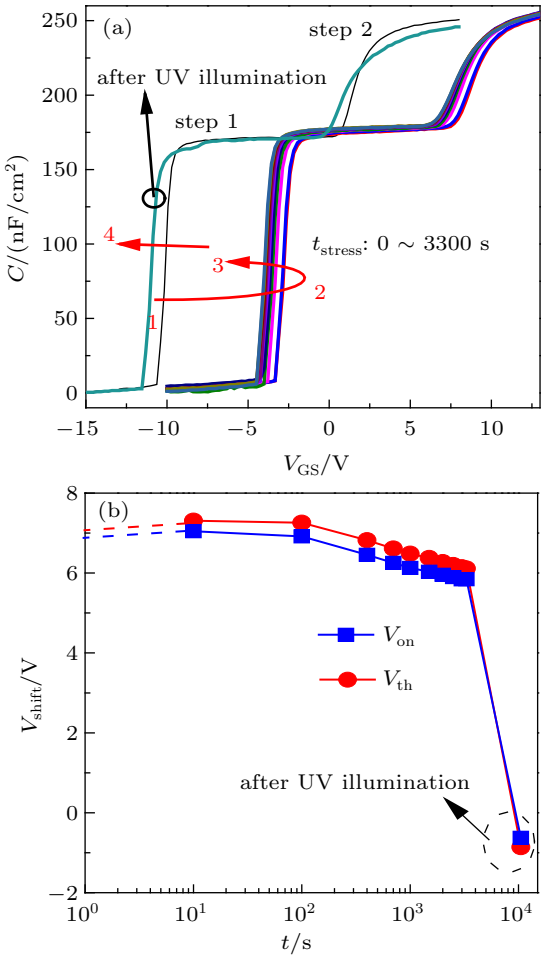


Fig. 11. (a) Monitored *C*–*V* characteristics during the gate degradation and after UV light illumination, (b) the shift of V_{th} and V_{on} *versus* stress time.

4. Conclusions

In summary, we have experimentally investigated the physical origin of the time-dependent gate degradation in LPCVD-SiN$_x$/AlGaN/GaN MIS-HEMTs under forward gate bias stress. Through the temperature-dependent gate current characteristics, the dominant mechanism of gate leakage current was identified to be PF emission which is a traps-assistant emission process under relatively high forward bias. During the forward gate bias stress, the stable output characteristics suggest that the degradation is concentrated in the gate dielectric region, instead of the AlGaN/GaN heterojunction. Combining with the frequency conductance method and double

sweep C–V curves, the newly increased traps were observed not only in the LPCVD-SiN_x layer but also at the LPCVD-SiN_x/AlGaN interface, resulting in the voltage shift and the increase of the voltage hysteresis. Particularly, we found that the traps generated in the LPCVD-SiN_x layer dominated the later stage of time-dependent gate degradation. Finally, the additional negative shift of V_{th} and V_{on} after UV light illumination confirmed the accumulation of positive charge at the LPCVD-SiN_x/AlGaN interface and/or in LPCVD-SiN_x layer, which is consistent with the generation of newly increased traps.

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