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Design of a novel high holding voltage LVTSCR with embedded clamping diode*

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In order to reduce the latch-up risk of the traditional low-voltage-triggered silicon controlled rectifier (LVTSCR), a novel LVTSCR with embedded clamping diode (DC-LVTSCR) is proposed and verified in a 0.18-μm CMOS process. By embedding a p^+ implant region into the drain of NMOS in the traditional LVTSCR, a reversed Zener diode is formed by the p^+ implant region and the n^+ bridge, which helps to improve the holding voltage and decrease the snapback region. The physical mechanisms of the LVTSCR and DC-LVTSCR are investigated in detail by transmission line pulse (TLP) tests and TCAD simulations. The TLP test results show that, compared with the traditional LVTSCR, the DC-LVTSCR exhibits a higher holding voltage of 6.2 V due to the embedded clamping diode. By further optimizing a key parameter of the DC-LVTSCR, the holding voltage can be effectively increased to 8.7 V. Therefore, the DC-LVTSCR is a promising ESD protection device for circuits with the operation voltage of 5.5–7 V.

Keywords: electrostatic discharge, silicon controlled rectifier, clamping diode, holding voltage

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1. Introduction

Although integrated circuits (ICs) become more and more complicated due to the continuous decrease in the minimum feature size and increase in the chip density, they are also becoming more and more vulnerable to electrostatic discharge (ESD) or electrical overstress (EOS) phenomena.[1] Thus the reliable ESD protection of ICs is critical to the reliability of most modern electronic and electrical products. Various researches have been carried out based on the conventional ESD protection structures such as diode, metal-oxide-semiconductor (MOS) and silicon controlled rectifier (SCR).[2–9] The diode[2] and gate-grounded NMOS (GGNMOS)[3] are attractive because of their small snapback margin. However, they have poor ESD robustness[4] and need large chip area to reach the required ESD protection level,[5] resulting in the increasing cost. The SCR is usually regarded as a promising ESD protection device due to its strong ESD robustness per unit area[6] and small parasitic effect,[7] whereas it is restrained from wide applications due to the high trigger voltage (V_{t1})[8] and low holding voltage (V_h),[9] which may result in the breakdown or latch-up of protected circuits.

Recently, various modified SCRs with a small snapback margin have been investigated, aiming at lowering the latch-up risk in high voltage (HV) ICs.[10–13] By integrating a GGNMOS in the SCR, a low-voltage-triggered SCR (LVTSCR) with reduced V_{t1} can be obtained,[10] while its small V_h[11] may lead to the logic disorder or even failure of the internal core circuit, making it still unsuitable for HV ESD protection. To increase the V_h, an self-triggered stacked SCR structure (STSSCR)[12] was proposed by stacking the diode-triggered SCR with the modified-lateral SCR. Unfortunately, the area efficiency of the STSSCR cannot be remarkably improved due to the increasing chip size. A high V_h dual-direction SCR[13] without increasing the chip area was then proposed. However, its leakage characteristics were unstable, having the risk of potential failure. Recently, a snapback-free SCR (SFSCR)[14] with high V_h has been developed by suppressing the snapback of the SCR. However, the added p-type Zener implantation in the device has higher requirements for the fabrication process. Other similar ESD protection solutions also have certain drawbacks and need to be further optimized. Therefore, it remains a demanding task to design an ESD-robust and latchup-immune SCR device.

In this paper, in order to improve the comprehensive ESD performance of LVTSCR without additional chip area consumption, a novel LVTSCR with embedded clamping diode (DC-LVTSCR) is proposed and manufactured in a 0.18-μm CMOS process. The physical mechanisms of both LVTSCR and DC-LVTSCR are investigated by TCAD simulations and transmission line pulse (TLP) tests. Compared with the traditional LVTSCR, the DC-LVTSCR exhibits a higher V_h and can be used in power circuits with the operation voltage of 5 V. By further optimizing a key size parameter, the multi-finger DC-LVTSCR can meet the ESD protection requirements of protected circuits with the operation voltage of 7 V.

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2. Device structure and operation mechanism

The schematic top views and cross sections of the LVTSCR and DC-LVTSCR are shown in Fig. 1. Both devices have the same width ($W = 80$ μm) and length ($L = 18$ μm). Compared to the LVTSCR, the drain of NMOS in the DC-LVTSCR is divided into an n^+ bridge and a topology structure. The topology structure is obtained by inserting the highly doped p^+ region at intervals in the striped highly doped n^+ region, as illustrated using the red dashed lines in Fig. 1(b). The n^+ bridge is directly connected to the n^+ implant region of the topology structure, where the length of n^+ bridge is marked as D_1. Meanwhile, there is a short spacing between the p^+ implant region of the topology structure and the n^+ bridge, forming a reversed Zener diode and helping to increase the V_h.

The schematic internal equivalent circuit of LVTSCR is shown in Fig. 1(a). When the LVTSCR is under an ESD stress, the minority carrier drift current (I_{drift}) is generated in the depletion layer of p–n junction formed by the drain of GGNMOS and the p-well. I_{drift} helps to increase the voltage drop on the p-well bias resistance (R_{pw}) up to 0.7 V, accelerating the turn-on of the parasitic SCR and resulting in a lower V_{t1}.

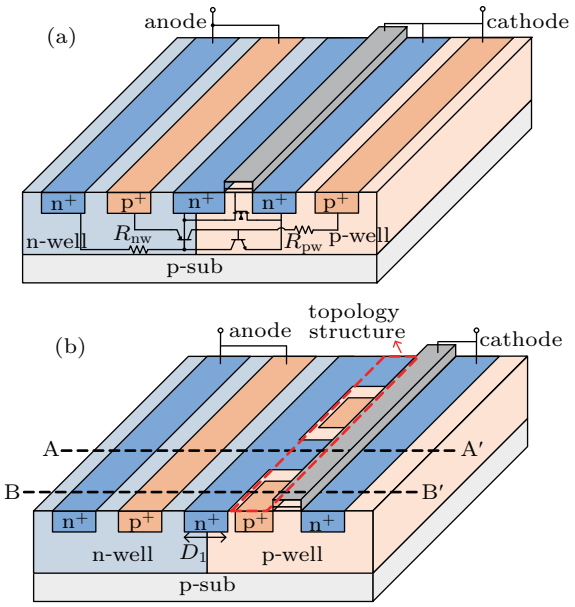


Fig. 1. The top views and cross sections of (a) LVTSCR and (b) DC-LVTSCR.

The schematic cross section cutting along the A–A′ line (marked in Fig. 1(b)) and the corresponding internal equivalent circuit of the DC-LVTSCR under an ESD stress are shown in Fig. 2(a). Although there is an additional R_{pw} in the LVTSCR, the operating mechanism of the DC-LVTSCR along the A–A′ profile is similar to that of the LVTSCR.

The schematic cross section cutting along the B–B′ line (marked in Fig. 1(b)) and the corresponding internal equivalent circuit of the DC-LVTSCR are shown in Fig. 2(b). When the DC-LVTSCR is under an ESD stress, a strong electric field is generated at the reversed p–n junction due to the short spacing between the n^+ bridge and p^+ implant region, resulting in the formation of a reversed Zener diode. With increasing ESD stress, the breakdown of Zener diode occurs first because of the strong electric field at the reversed p–n junction. Large amounts of breakdown current help to turn on the parasitic SCR. After the DC-LVTSCR is fully turned on, there are two parallel current discharging paths, one is the Zener diode path along the device surface, and the other is the SCR path inside the device. The Zener diode can stabilize the voltage, so the voltage drop across the diode is maintained at a high value. As a result, the voltage drop across the SCR can be clamped at a high value due to the parallel Zener diode, resulting in a higher V_h. Meanwhile, the embedded p^+ implant region increases the doped concentration in the base region of n–p–n transistor, resulting in a reduced magnification of n–p–n and a weakened positive feedback of parasitic SCR. Hence, a smaller snapback voltage margin of DC-LVTSCR can be achieved.

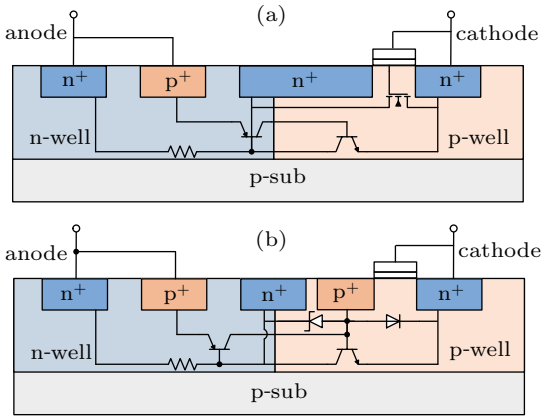


Fig. 2. Cross sections and the corresponding internal equivalent circuits of the DC-LVTSCR cutting along the (a) A–A′ and (b) B–B′ lines marked in Fig. 1(b).

3. TCAD simulations

The above-analyzed working mechanisms of the two devices can also be verified by three-dimensional (3D) Sentaurus TCAD simulations. The physics models of SRH and Auger Recombination, mobility, effective intrinsic density, avalanche breakdown and Fermi energy are used in the simulations. The length of the simulated devices is the same as that of the actual devices, and the width of the simulated devices is 8 μm, one tenth of the actual width. Figure 3 shows the simulated electric field distributions in the LVTSCR and DC-LVTSCR before they are triggered. When the LVTSCR is under an ESD stress, a strong electric field is formed between the drain of NMOS and the p-well. When the electric field is close to the critical breakdown electric field, the breakdown of the reversed p–n junction formed by the drain of NMOS and the p-well occurs first, meaning that the LVTSCR is triggered by GGNMOS first. Compared with the LVTSCR, the DC-LVTSCR

has different electric field distribution. The strong electric field of DC-LVTSCR is not only formed at the interface of p-well and the drain of NMOS, but also at the reverse junction of n^+ bridge and p^+ implant region.

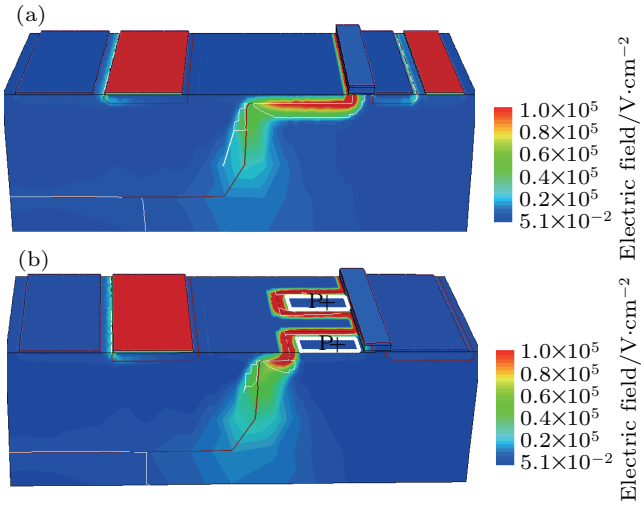


Fig. 3. The simulated 3D electric field distributions of (a) LVTSCR and (b) DC-LVTSCR.

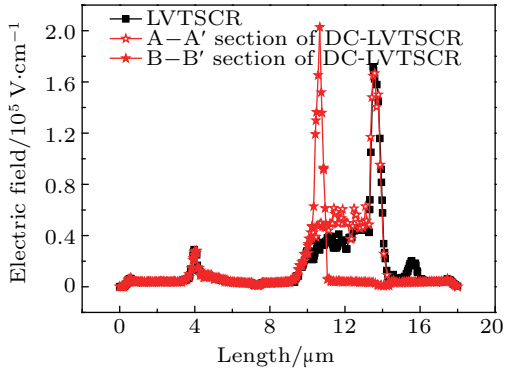


Fig. 4. The electric field variation along the device length of LVTSCR and DC-LVTSCR.

Figure 4 shows the simulated electric field values along the L from the anode to the cathode, extracted from the 3D simulation results of the two devices under the same ESD current stress at the longitudinal depth of 0.1 μm. As shown in Fig. 4, the peak electric field of LVTSCR is located at the reversed p–n junction of the GGNMOS, in agreement with the above analysis. For the DC-LVTSCR, the electric field distribution along the A–A′ section is similar to that of the LVTSCR due to the similar structure. However, owing to the short spacing between the n^+ bridge and p^+ implant region, the peak electric field along the B–B′ section is located at the reversed Zener p–n junction, contributing to a low V_{t1}. In addition, the breakdown voltage of DC-LVTSCR can be further adjusted by changing the spacing between n^+ bridge and p^+ implant region, making the device applicable for multi-power domain.

Figure 5 shows the simulated electrostatic potential distributions in the LVTSCR and DC-LVTSCR when they are post-triggered under the same ESD stress. Obviously, the electrostatic potential of the anode in the DC-LVTSCR is higher than that in the LVTSCR, indicating that the voltage drop on both sides of the reversed Zener diode can be maintained at a high value. Therefore, the V_h of the DC-LVTSCR can be increased, providing a smaller voltage snapback margin.

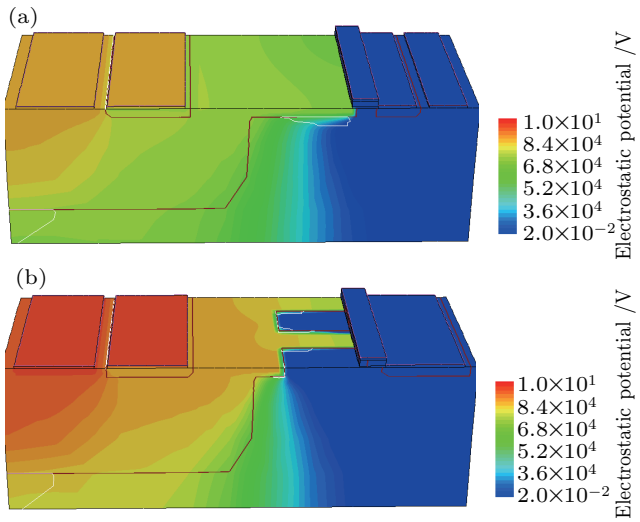


Fig. 5. The simulated 3D electrostatic potential of (a) LVTSCR and (b) DC-LVTSCR.

4. Results and optimization

4.1. TLP test results

A series of experimental devices of both LVTSCR and DC-LVTSCR were fabricated in a 0.18-μm CMOS process, and measured by a Celestron-TLP standard test system with a rise time of 10 ns and a pulse width of 100 ns. The typical current-voltage (I–V) curves are shown in Fig. 6. Compared to the LVTSCR, the V_h of the DC-LVTSCR increases remarkably from 2.6 to 6.2 V, due to the introduced Zener diode. In addition, the V_{t1} of the DC-LVTSCR decreases slightly from 13.8 V to 12.9 V, due to a strengthened electric field of the reversed p–n junction.

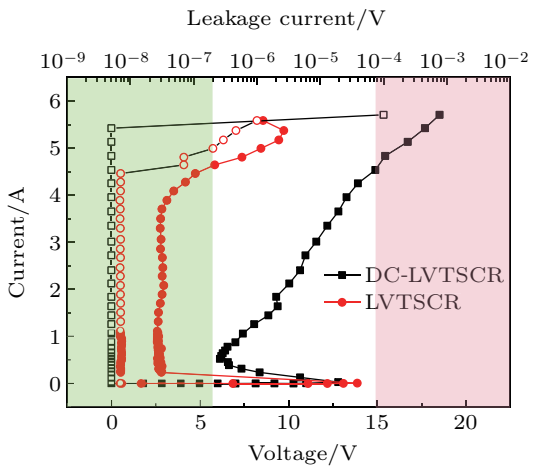


Fig. 6. The TLP I–V curves of LVTSCR and DC-LVTSCR experimental devices.

According the ESD design rules, the voltage range of the ESD window should be determined by 1.1 times of the operation voltage and 0.8 times of the gate oxide breakdown voltage, which is determined by the thickness of gate oxide and appropriately equals to 15 V according to the characteristics of the 0.18-μm CMOS process. The snapback voltage margin of the ESD protection devices should fall within the ESD window. Therefore, the DC-LVTSCR can be used as ESD protection device for ICs with an operation voltage of about 5.5 V.

4.2. Key size optimization

In order to explore the possibility of further increasing the $V_{\rm h}$, two DC-LVTSCR devices with different D_1 values were fabricated and compared, where the key size D_1 is the length of n^+ bridge as marked in Fig. 1(b). Their TLP I–V curves are shown in Fig. 7.

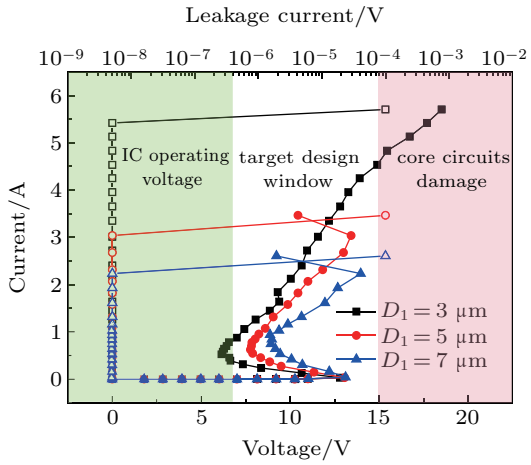


Fig. 7. The TLP I–V curves of DC-LVTSCR with different D_1 values.

When D_1 of the DC-LVTSCR increases from 3 μm to 7 μm, the $V_{\rm h}$ increases from 6.2 V to 8.7 V and the snapback margin decreases from 6.7 V to 4.1 V, whereas $I_{\rm t2}$ decreases from 4.1 A to 2.6 A. Due to the increase of D_1, the base width of the parasitic n–p–n and p–n–p transistors, as shown in Fig. 1(b), is enlarged, which reduces the emission efficiency of the two transistors. Thus the positive feedback effect of the parasitic SCR is weakened, contributing to a higher $V_{\rm h}$ and a lower $I_{\rm t2}$. However, if the length of D_1 is further increased, the $I_{\rm t2}$ of the device will continue to decrease, which requires a large area to achieve the desired ESD robustness. Consequently, the optimized DC-LVTSCR with a D_1 of 5 μm can be applied in protecting circuits with an operation voltage of about 7 V.

The human body model (HBM) ESD robustness measured by the Celestron-TLP test system can be calculated by[15]

$$\mathrm{HBM} = I_{\rm t2} \times R_{\rm human}, \tag{1}$$

where $I_{\rm t2}$ is the failure current and $R_{\rm human}$ is the equivalent resistance of the TLP test system, which is approximately equal to 1.5 kΩ. The calculation results show that all the DC-LVTSCR devices have an ESD robustness of more than 4 kV.

In order to compare the ESD performance and chip area consumption of LVTSCR and DC-LVTSCR comprehensively, the figure of merit (FOM) is introduced to evaluate the efficiency ratio of ESD protection devices, which is defined as[16]

$$\mathrm{FOM} = \frac{I_{\rm t2} \times V_{\rm h}}{V_{\rm t1} \times W}. \tag{2}$$

According to Eq. (2), the higher the $I_{\rm t2}$ and $V_{\rm h}$ are, the more effective the ESD protection device is. The measured ESD characteristics and calculated FOM of LVTSCR and DC-LVTSCR are summarized in Table 1. It can be found that with increasing D_1, the FOM of DC-LVTSCR decreases, but remains about twice the value of LVTSCR. Therefore, the DC-LVTSCR devices with certain D_1 values have a higher ESD protection efficiency per unit area than the LVTSCR, indicating that they are more suitable for HV ESD protection applications.

Table 1. The ESD characteristics of LVTSCR and DC-LVTSCR.

Experimental device	$V_{\rm t1}$/V	$V_{\rm h}$/V	$I_{\rm t2}$/A	FOM/A·μm^{-1}
LVTSCR	13.8	2.6	4.7	0.011
DC-LVTSCR ($D_1 = 3$ μm)	12.9	6.2	4.5	0.027
DC-LVTSCR ($D_1 = 5$ μm)	12.9	7.6	3.0	0.022
DC-LVTSCR ($D_1 = 7$ μm)	12.9	8.7	2.5	0.021

5. Conclusion

A novel DC-LVTSCR has been designed and fabricated in a 0.18-μm CMOS process. By introducing a Zener diode in the conventional LVTSCR, the DC-LVTSCR harvests a high $V_{\rm h}$ and a small snapback voltage margin. The effect of the embedded p^+ implant region on ESD protection performance is analyzed on the basis of 3D simulations and TLP test results. By optimizing the key size parameter D_1, the $V_{\rm h}$ of DC-LVTSCR can be further increased to 8.7 V. Consequently, the DC-LVTSCR with a $V_{\rm t1}$ of 12.9 V and a $V_{\rm h}$ of 8.7 V is particularly suitable for ESD protection applications in the 5.5–7 V power domains.

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