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Variable-K double trenches SOI LDMOS with high-concentration P-pillar*

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A variable-K trenches silicon-on-insulator (SOI) lateral diffused metal–oxide–semiconductor field-effect transistor (MOSFET) with a double conductive channel is proposed based on the enhancement of low dielectric constant media to electric fields. The device features variable-K dielectric double trenches and a P-pillar between the trenches (VK DT-P LDMOS). The low-K dielectric layer on the surface increases electric field of it. Adding a variable-K material introduces a new electric field peak to the drift region, so as to optimize electric field inside the device. Introduction of the high-concentration vertical P-pillar between the two trenches effectively increases doping concentration of the drift region and maintains charge balance inside it. Thereby, breakdown voltage (BV) of the device is increased. The double conductive channels provide two current paths that significantly reduce specific on-resistance ($R_{on,sp}$). Simulation results demonstrate that a 17-μm-length device can achieve a BV of 554 V and a low on-resistance of 13.12 mΩ·cm^2. The $R_{on,sp}$ of VK DT-P LDMOS is reduced by 78.9% compared with the conventional structure.

Keywords: variable-K (VK), trench technology, specific on-resistance ($R_{on,sp}$), breakdown voltage (BV)

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1. Introduction

Silicon-on-insulator (SOI) lateral diffused metal–oxide–semiconductor (LDMOS) devices with dielectric buried layers have broad applications in power IC market due to their excellent isolation capacity and strong immunity to latching effect.[1–4] In order to achieve better breakdown characteristics for planar LDMOS devices, charge balance principle has been widely used.[5–7] Although it has a good effect on improving power figure of merit (FOM), there is no effect on reducing device area.

However, the trench technology has excellent effects on reducing device area, which can reduce $R_{on,sp}$ while reducing the cell pitch without sacrificing device BV.[8–11]

By changing dielectric constant and combining with trench structure, limitations of dielectric trenches on device performances are reduced.[12–14] What should be noted is that abilities of dielectric materials to withstand the BV are inversely proportional to dielectric constant, and their abilities to assist in depleting the drift region are proportional to dielectric constant.[15] This paper presents a high-voltage and low-on-resistance VK DT-P LDMOS with double conductive channels. Design of the structure includes double variable-K trenches and conductive channels. The double variable-K trenches are to increase voltage of the device, but it is indicated by simulation that the deeper a dielectric trench is, the more difficult it will be to apply to the deeper half of a drift region, which means that deeper trenches cannot completely deplete drift regions. Therefore, a vertical P-pillar is designed between the two trenches in this paper. The P-pillar can optimize electric fields in drift regions and maintain charge balance within the entire region, ensuring BV of the VK DT-P LDMOS while greatly reducing its $R_{on,sp}$.

2. Structure and mechanism

Figure 1 shows the diagram of VK DT-P LDMOS and the withstand voltage schematics. As shown in Fig. 1(a), the VK DT-P LDMOS has three significant structural features: (i) There are two dielectric trenches with depth D_t and width W_t. Upper half of the deep trench is filled with a low dielectric constant with thickness D_1, whose K value is 1.8. The rest of the deep trench is filled with silica dielectric, whose K value is 3.9; (ii) A P-pillar with depth D_P and width W_P is designed between the double trenches to assist in depleting the drift region; (iii) Two vertical gates are designed inside both of the double trenches to introduce double conductive channels.

Using the ENDIF effect, BV can be written as

$$V_B = V_{bs} + E_I t_I, \tag{1}$$

where V_{bs} is the potential difference of the silicon region. The Gauss theorem in the interface of dielectric layer is

$$\varepsilon_I E_I = E_S \varepsilon_S + q\sigma_{in}, \tag{2}$$

where E_S, E_I, and ε_s, ε_I are respectively electric fields and dielectric constants of the top and buried layer in the interface.

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The t_s is the thickness of drift region, t_I is the thickness of oxide layer, and σ_{in} is the interface charge density.

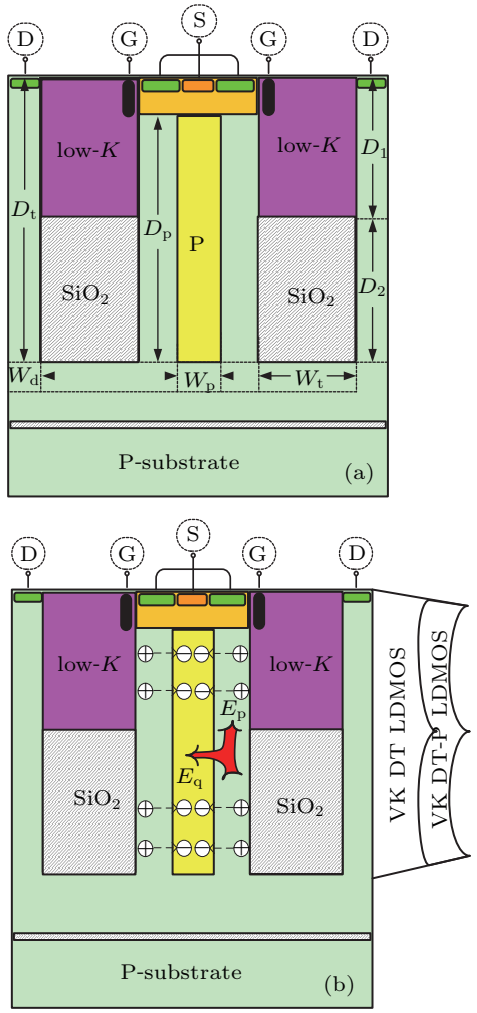


Fig. 1. The structure and mechanism of VK DT-P LDMOS: (a) the structure of VK DT-P LDMOS, (b) the mechanism of VK DT-P LDMOS.

Table 1. Structural parameters.

Parameters	VK DT-P LDMOS
D_1, D_2, D_t/μm	8, 7.5, 15.5
W_d, W_P/μm	2, 2
K_1, K_2	1.8, 3.9
N_d/cm^{-3}	5×10^{15}
N_P/cm^{-3}	1.1×10^{16}
W_t/μm	4

Since electric flux between the interfaces is continuous, a low dielectric constant is introduced to improve vertical *BV* under the condition of the Gauss theorem, and there is no charge in the buried layer interface of the drift region. The electric field flux in the vertical body is 0.

When $\sigma_{in}=0$, formula (2) can be simplified as

$$\varepsilon_I E_I = E_S k_S, \quad E_S = \frac{\varepsilon_I E_I}{k_S}. \tag{3}$$

Compared with DT-P LDMOS, VK DT-P LDMOS adds low-*K* dielectric to the oxidation trench. Breakdown electric field of the dielectric buried layer is much higher than that of silicon. It is obtained from Eq. (3) that k_S is reduced, and vertical *BV* of VK DT-P LDMOS is increased by enhancing electric field of the dielectric buried layer.

A high-concentration P-pillar is designed between the two trenches to optimize equipotential distribution and to form a new charge balance with ionized charges in the drift region. Therefore, the doping concentration of the drift region can be effectively increased to reduce $R_{on,sp}$. As shown in Fig. 1(b), the acceptor ion remaining in the depleted P-pillar will attract electric field lines from the drift region to produce a lateral electric field E_q, which is a superposition component of the vertical electric field E_p in the double trenches of the drift region that greatly slows down superposition progress of the vertical electric field E_p and largely optimizes *in-vivo* electric field of the device. On the right side of Fig. 1(b), the VK DT-P LDMOS with a P-pillar increases about a half of area compared to VK DT LDMOS, which greatly increases *BV* and also assists in depleting an n-type drift region with P-pillar to reduce $R_{on,sp}$ of VK DT-P LDMOS. A vertical gate is designed on inner sides of the double trenches. When the device is in the ON state, the double gates will provide two conduction channels for current, which help it to selectively flow through the drift region and optimize $R_{on,sp}$.

3. Simulation result and discussion

The four structures, conventional DT LDMOS (Con. DT LDMOS), VK DT LDMOS, DT-P LDMOS, and VK DT-P LDMOS are simulated and compared through TCAD simulation software. Comparing surface electric field distributions ($y=0.001$ μm) of the four structures in Fig. 2, due to the addition of high-concentration P-pillar and low-*K* trenches, electric field of VK DT-P LDMOS is increased from 67 V/μm to 151 V/μm, compared to the conventional structure.

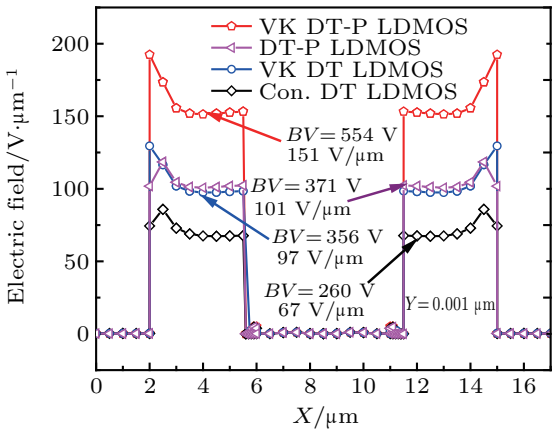


Fig. 2. The surface electric field distribution.

Figure 3 shows the vertical electric field in variable-*K* trench ($X=4.399$ μm) and the illustration shows a partial electric field in it on the left ($X=2$ μm). The trench is filled

with different dielectrics in upper and lower parts. The low-K dielectric layer used on the surface can increase surface electric field of the dielectric layer and thereby reducing surface area since electric flux between the dielectric interfaces is continuous. Electric field on the left side of the trench further illustrates that the variable-K dielectric trench causes a new electric field peak (as is shown at point B) to increase the overall BV that is shown in the illustration. The addition of P-pillar makes electric field concentration between the two dielectric trenches downward, thereby optimizing electric field distribution.

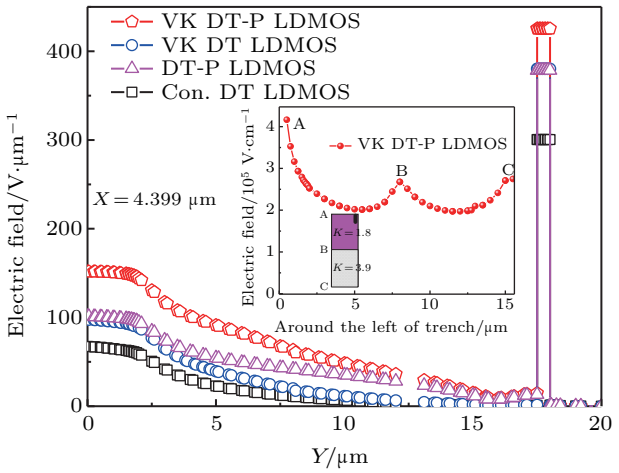


Fig. 3. Vertical electric field of the four structures and electric field around left trench of the new structure.

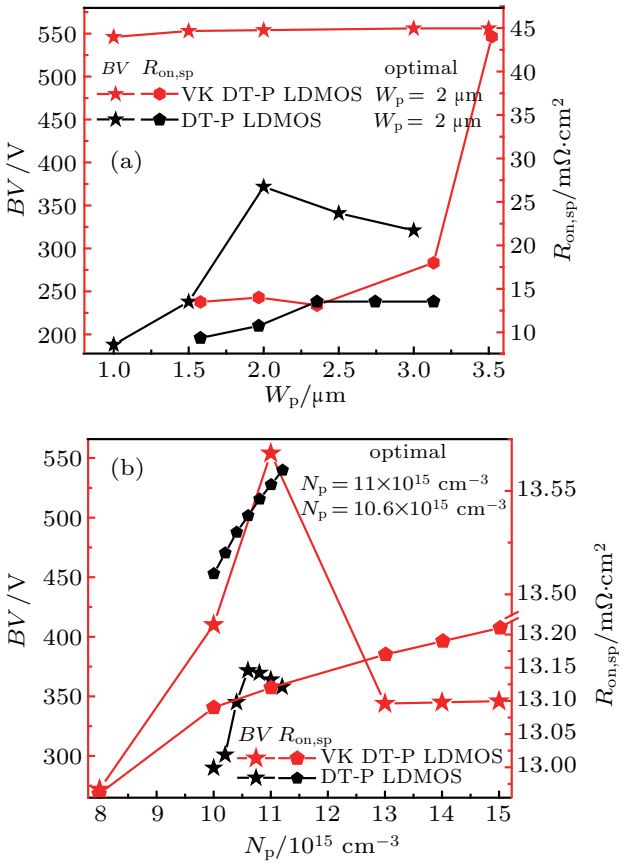


Fig. 4. Effects of W_P and N_d of P-pillar on BV and $R_{on,sp}$.

Figure 4 discusses influences of width W_P and concentration N_d to BV and $R_{on,sp}$. It is known that in Fig. 4(a), the optimal value of P-pillar width (W_P) is 2 μm. When $W_P > 2$ μm, BV of DT-P LDMOS remains basically unchanged and that of VK DT-P LDMOS shows a downward trend. As shown in Fig. 4(b), when widths of both pillars are equal, the concentration difference is 3.8% and the BV difference is 48.9%, which fully reflects influences of introduction of the low-K dielectric trench to improving BV of device. the P-pillar optimizes the bulk electric of and causes a new charge balance between the ionized donors and accepters in the drift region. Thus, the doping concentration of the drift region can be increased efficiently to reduce $R_{on,sp}$.

Effects of depth of low-K trench (D_1) and value of K on $R_{on,sp}$, BV and FOM are shown in Fig. 5. Figure 5(a) illustrates the effects of D_1 on $R_{on,sp}$, BV, and FOM. With increases of depth, $R_{on,sp}$ of the new structure slowly decreases and then gradually increases, and BV increases first and then decreases. The optimal value of FOM reaches 23.4 MW/cm^2. Figure 5(b) shows effects of K value on BV and $R_{on,sp}$. The pie chart represents proportion of FOM in case that K = 1–2.6. When K = 1.8, the highest proportion is 17.91%.

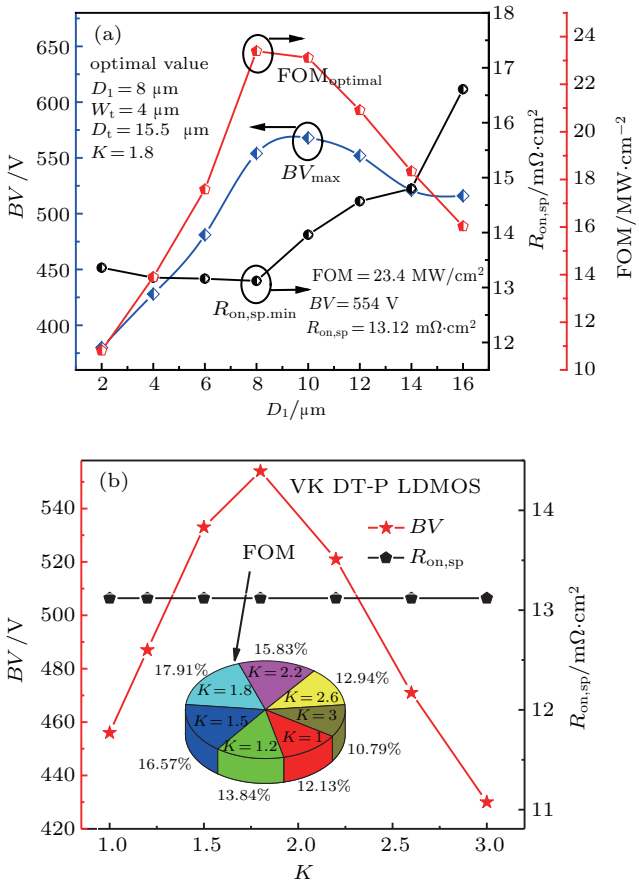


Fig. 5. Effects of depth of low-K trench (D_1) and value of K on $R_{on,sp}$, BV, and FOM.

Figure 6 shows the relationship between leakage voltage and leakage current of the four structures in OFF state. Due

to introduction of variable-K trenches and a p-type doped pillar, the overall electric field is increased, and the drift region is depleted, so that electric field of the new structure reaches 151 V/μm. It can be seen from equipotential distribution diagrams of the four structures in the illustration that Con. DT LDMOS has few equipotential lines and an uneven distribution in the drift region. Equipotential lines in VK DT LDMOS are not only more than those in Con. DT LDMOS, but are also distributed more deeply in the drift region. Compared with Con. DT LDMOS, the vertical P-pillar introduced in DT-P LDMOS not only adds extra equipotential lines but also extends them to the bottom of drift region of DT-P LDMOS, making them distributing evenly in the drift region. Compared with the other three structures, VK DT-P LDMOS introduces a larger number of equipotential lines and makes them more uniformly distributing in the drift region. Its drift region utilization is also higher, and its BV is also the highest.

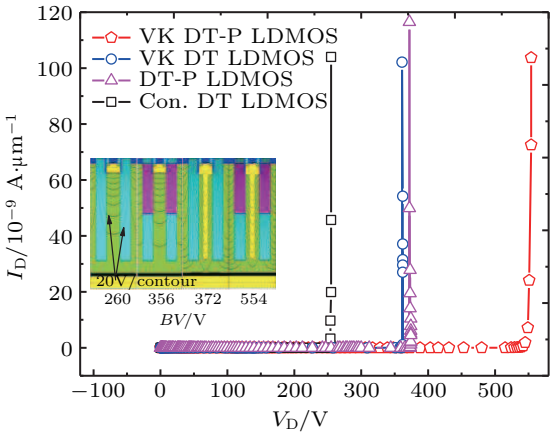


Fig. 6. Relationship of leakage voltage and leakage current of the four structures in breakdown state.

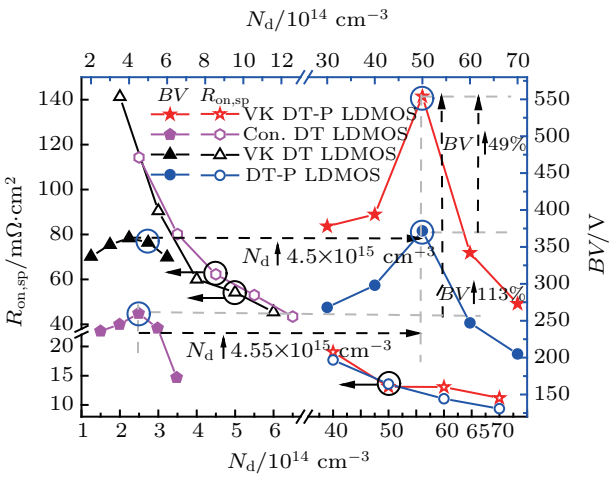


Fig. 7. The relationship between N_d and BV, $R_{on,sp}$.

Figure 7 illustrates that BV and $R_{on,sp}$ are affected by changes of N_d. It is easily seen from the figure that BV of the four devices first rises with the increase of drift region concentration, and then decreases. So, the device can gain the optimal value of BV. When N_d is 5×10^{15} cm^{-3}, the proposed VK DT-P LDMOS will gain a maximum BV of 554 V. Compared with Con. DT LDMOS ($N_d = 4.5\times10^{14}$ cm^{-3}) and VK DT LDMOS ($N_d = 5\times10^{14}$ cm^{-3}), the new structure's abilities to assist in depleting the drift region are significantly increased. When $N_d > 5\times10^{15}$ cm^{-3}, the device cannot be completely depleted to reduce BV of the device.

VK DT-P LDMOS introduces high-concentration of P-pillar based on VK DT LDMOS to assist in depleting the entire drift region. It provides a low-impedance path for current in the ON state, thereby reducing $R_{on,sp}$ of the device.

Table 2 shows comparisons in electrical characteristics of the four device structures. It can be seen from the table that the maximum FOM ($BV^2/R_{on,sp}$) obtained in VK DT-P LDMOS at $D_1 = 8$ μm and $N_d = 5\times10^{15}$ cm^{-3} is 23.39 MW/cm^2.

Table 2. Performance comparison chart of the four devices.

Devices	BV/V	$R_{on,sp}$/mΩ·cm^2	FOM/(MW/cm^2)
VK DT-P LDMOS	554	13.12	23.39
DT-P LDMOS	372	13.54	10.203
VK DT LDMOS	356	54.27	2.335
Con. DT LDMOS	260	62.25	1.085

Figure 8 shows the relationship between BV and $R_{on,sp}$ in different devices. As can be seen from the figure, a good compromise between BV and $R_{on,sp}$ is achieved in VK DT-P LDMOS.

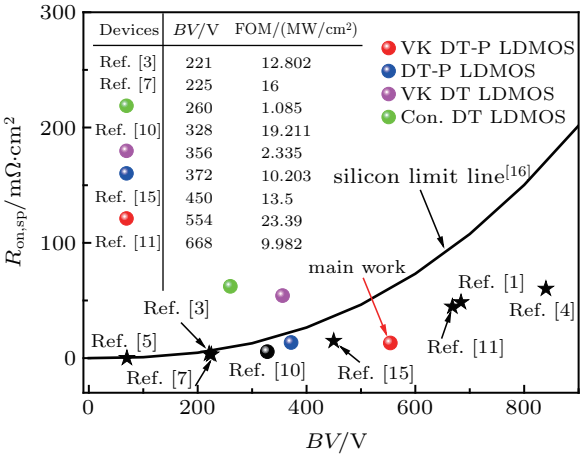


Fig. 8. *BV versus* $R_{on,sp}$ tradeoff relationship for different devices.

Figure 9 shows the process flow of VK DT-P LDMOS.

i) As shown in Fig. 9(a), two silicon substrates are bonded together after oxidation.

ii) Etch in the drift region of silicon materials to form a double rectangular region.

iii) Fill the rectangular region with low pressure chemical vapor deposition (LPCVD) with silica ($K = 3.9$). At this time, a silica dielectric step will appear. Therefore, chemical

mechanical polishing (CMP) planarization and etching are required to form a semi-silica dielectric trench, which is shown in Fig. 9(d).

iv) Fill a low-K ($K = 1.8$) with LPCVD and CMP.

v) Etch the P-pillar and fill the rectangular trench. In Fig. 9(f), to prevent impurities from contaminating the drift region and dielectric materials, a mask is needed.

vi) Deposit a P-pillar and implant impurities through ion implantations to form a p-well. N+, P+, and N+ under the drain are generated through the same process, all of which are shown in Fig. 9(i).

vii) Fabricate electrodes and vertical gates. As shown in Fig. 9(j), etch the vertical gate rectangular trench at a distance of 0.05 μm from the inner side, deposit the poly-silicon material and etch away excess portions.

viii) Sources and drain metals are deposited and the excess are etched away. After the above process is completed, surface of the device needs to be isolated, and a layer of silicon dioxide is deposited to protect the electrodes. Finally, etch the trough-hole with dry etch to avoid metal ion contaminations inside of containers and lead out a conducting wire to form a VK DT-P LDMOS, as is shown in Fig. 9(k).



Fig. 9. The process of VK DT-P LDMOS.

4. Conclusion

In this paper, a VK DT-P LDMOS with double conductive channels is proposed. Double conductive channels provide two current paths, significantly reducing $R_{on,sp}$. The variable-K trenches not only reduce surface area of the device but also introduce a new electric field peak in the drift region, which greatly improves BV. A high-concentration P-pillar modulates electric field, increases drift region concentration, and forms a new charge balance within the drift region. Comparing the four structures with simulation, the BV of the new structure

VK DT-P LDMOS was increased by 113%, 56%, and 49%, respectively. The $R_{on,sp}$ was reduced by 78.9%, 70.3%, and 3.1%, respectively.

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