ISSN 1674-1056
http://cpb.iphy.ac.cn
http://iopscience.iop.org/cpb
中国物理 B
Chinese Physics
中国物理 Chinese Physics B

Quantum legitimacy of reversible gate and a new design of multiplier based on R gate

Tingyu Ge(葛庭宇), Tinggui Zhang(张廷桂), Xiaofen Huang(黄晓芬)
Citation: Chin. Phys. B . 2020, 29(5): 050305 . **doi:** 10.1088/1674-1056/ab7d9d
Journal homepage: http://cpb.iphy.ac.cn; http://iopscience.iop.org/cpb

What follows is a list of articles you may be interested in

Generating Kerr nonlinearity with an engineered non-Markovian environment

Fei-Lei Xiong(熊飞雷), Wan-Li Yang(杨万里), Mang Feng(冯芒)
Chin. Phys. B . 2020, 29(4): 040302 . **doi:** 10.1088/1674-1056/ab7741

Reconciliation for CV-QKD using globally-coupled LDPC codes

Jin-Jing Shi(石金晶), Bo-Peng Li(李伯鹏), Duan Huang(黄端)
Chin. Phys. B . 2020, 29(4): 040301 . **doi:** 10.1088/1674-1056/ab6d4f

Quantum speed limit time of a non-Hermitian two-level system

Yan-Yi Wang(王彦懿), Mao-Fa Fang(方卯发)
Chin. Phys. B . 2020, 29(3): 030304 . **doi:** 10.1088/1674-1056/ab6c45

Heralded entanglement purification protocol using high-fidelity parity-check gate based on nitrogen-vacancy center in optical cavity

Lu-Cong Lu(陆路聪), Guan-Yu Wang(王冠玉), Bao-Cang Ren(任宝藏), Mei Zhang(章梅), Fu-Guo Deng(邓富国)
Chin. Phys. B . 2020, 29(1): 010305 . **doi:** 10.1088/1674-1056/ab5939

Fault tolerant controlled quantum dialogue against collective noise

Li-Wei Chang(常利伟), Yu-Qing Zhang(张宇青), Xiao-Xiong Tian(田晓雄), Yu-Hua Qian(钱宇华), Shi-Hui Zheng(郑世慧)
Chin. Phys. B . 2020, 29(1): 010304 . **doi:** 10.1088/1674-1056/ab5786

Quantum legitimacy of reversible gate and a new design of multiplier based on R gate*

Tingyu Ge(葛庭宇), Tinggui Zhang(张廷桂)†, and Xiaofen Huang (黄晓芬)

School of Mathematics and Statistics, Hainan Normal University, Haikou 571158, *China*

(Received 10 January 2020; revised manuscript received 21 February 2020; accepted manuscript online 9 March 2020)

Quantum full adders play a key role in the design of quantum computers. The efficiency of a quantum adder directly determines the speed of the quantum computer, and its complexity is closely related to the difficulty and the cost of building a quantum computer. The existed full adder based on R gate is a great design but it is not suitable to construct a quantum multiplier. We show the quantum legitimacy of some common reversible gates, then use R gate to propose a new design of a quantum full adder. We utilize the new designed quantum full adder to optimize the quantum multiplier which is based on R gate. It is shown that the new designed one can be optimized by a local optimization rule so that it will have lower quantum cost than before.

Keywords: reversible gate, quantum full adder, quantum multiplier

PACS: 03.67.–a, 02.20.Hj, 03.65.–w **DOI:** 10.1088/1674-1056/ab7d9d

1. Introduction

Quantum computers have far more computing power than classical computers. This is because of the properties called quantum parallel operation. Plenty of questions cannot be solved with a classical computer because it will cost ridiculous resources. Quantum computer can solve some of these problems because of quantum parallel operation. Based on this properties, a lot of quantum algorithms have been designed. Grover's search algorithm[1] and Shor's factorization algorithm are included.[2] Since quantum computers are based on quantum gates and all quantum gates are reversible, the research of reversible gates plays an important role in quantum computers.

The research of reversible gates is an important branch of basis mathematics. The reason why reversible gates were the first choice is that it does not consume any energy in theory. Based on Landauer's principles,[3] if a computation could be done reversibly, then the energy consumed can be zero. Since a reversible gate maps each input vector to an output vector uniquely and vice versa,[4] that means a reversible computation does not erase any information, it does not cost any energy. Besides the application in quantum computer, reversible gates are also widely used in other fields, such as low power CMOS systems,[5] optical computing,[6] DNA computing,[7] and nanotechnology.[8] It is very clear that the research of reversible gates will provide a solid theoretical basis for fundamentals and applications.

Arithmetic adders and multipliers are the fundamental component in computational units. It is clear that adders and multipliers are the fundamental of a classical computer. As a result, quantum adders and multipliers should be designed to build perfect quantum computers. However, it lies a question: classical adders and multipliers are irreversible (most classical logic gates are irreversible such as AND and OR), hence they cannot be used directly in quantum computers. Thus, quantum arithmetic operations must be built from reversible gates.[9] Based on this idea, lots of reversible adders and multipliers using different reversible gates have been proposed. A design of reversible full adders using two RG gates is introduced in Ref. [10]. Thersesal *et al.*[11] have proposed a new reversible gate called NR gate, then used this gate to construct a full adder and a subtractor. Thapilyal *et al.*[12] used TR gate to build a full adder, and it has been optimized. Islam *et al.*[13] have proposed a full adder with two P gates, and the quantum cost has been optimized by Banerjee *et al.*[14] A new reversible gate was introduced in Ref. [15], then it has been used to made a full adder and a subtractor.[16]

In this paper, we focus on the quantum legitimacy of main reversible gates and a new design of multiplier using R gate. We are going to show the quantum legitimacy of N, C, T, P and R gates. Then we propose a new design of a full adder using R gate. We show that when we use the new full adder to build a multiplier, our new designed multiplier has absolute advantage than using the existed full adder based on R gate, and our design has the lowest garbage bit and quantum cost, then we explain the advantages of using R gate to build quantum Arithmetic operations. The chapters are distributed as follows: In Section 2, we introduce some definitions and facts which will be referred in this paper. Section 3 lists some reversible gates, and shows the quantum legitimacy of these reversible gates. In Section 4, we propose a new design of a full adder, then build a multiplier with it. In Section 5, we give conclusions

*Project supported by the National Natural Science Foundation of China (Grant No. 11861031).

†Corresponding author. E-mail: tinggui333@163.com

© 2020 Chinese Physical Society and IOP Publishing Ltd

and compare our designs with relevant designs proposed by others.

2. Definitions and fact

First, we recall some basic concepts and facts.

Definition 1 An m-input, m-output, totally specified Boolean function will be reversible if it maps each input assignment to a unique output assignment.

Definition 2 An n-input, n-output gate will be reversible if it realizes a reversible function.[17]

Definition 3 Reversible gate G corresponds to a reversible function f, and it is bijective.[18][19]

As we can seen from the above three definitions, a reversible gate is equal to a bijective function, and it is a boolean function. It means that many properties about bijective function and boolean function are applicable for reversible gates.

Definition 4 The cost of the circuit is the total cost of all the n gates used to synthesize the circuit.[19]

This definition give us a way to compute the whole quantum cost of a circuit.

Definition 5 The constant bit is an input to the circuit used to compute some given logical operations.[16]

Simply, a constant bit is an input bit which value is given.

Definition 6 Garbage bit is an additional output to the reversible logical gate, and it is added to make the number of inputs equal to the number of outputs whenever necessary, in order to achieve reversibility.[20]

Garbage bit is something that people love and hate. The existed garbage bit makes irreversible gate to reversible gate. The existence of it is essential. However, garbage bit will destroy the interference properties crucial to quantum computation. As a result, we should keep its quantity as low as possible, even it will generate additional consumption, especially in quantum computer and quantum computation.

Definition 7 The quantum cost of any reversible circuit is the number of 2-qubit gates used to build the circuit. Generally speaking, we consider the quantum cost of any 1-qubit gate as zero, the quantum cost of any 2-qubit reversible gate as one, and the quantum cost of the other reversible gates is calculated by counting the number of 2-qubit gates used to build them.[18,19]

Definition 8 A quantum bit can be defined by a vector, and denoted by qubit. There are two based qubits, 0 and 1.[21] Their corresponding vectors are $|\mathbf{0}\rangle = (1\ \ 0)$ and $|\mathbf{1}\rangle = (0\ \ 1)$.

Definition 9 A reversible gate will be quantum legitimacy if it can be represented by a unitary matrix M.[21]

3. Common reversible gates and quantum legitimacy

There are many reversible gates, and these gates can used to construct lots of circuits. In this section we introduce some common reversible gates and show the matrix of them, so that these reversible gates can be used as quantum gates, which means that circuits based on these gates are also suitable for quantum computers.

The NOT gate (N) is a one-bit gate, it flips the input bits unconditionally. The quantum cost of NOT gate is zero. it is trivial that for a 1×1 reversible circuit, there is only one NOT gate. In quantum computation, it is called the Pauli matrix, and it can be represented by matrix $X = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}$.

The controlled-NOT gate or CNOT gate is a reversible gate, and also a two-qubit quantum gate. The quantum cost of CNOT gate is one. It is easy to see that there are two possible CNOT gates for a 2×2 circuit. The action of the CNOT gate is given by $|c\rangle|t\rangle \rightarrow |c\rangle|c\oplus t\rangle$, that is, if the control qubit is set to $|\mathbf{1}\rangle$, then the target qubit will be flipped, otherwise the target qubit will be let alone. Thus, the matrix representation of CNOT are

$$C(1,2) = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix},\ C(2,1) = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \end{pmatrix}.$$

The Toffoli gate (T) is a 3×3 reversible gate, and also a three-qubit quantum gate. The quantum cost of Toffoli gate is five. There are three possible Toffoli gates for a 3×3 circuit. The circuit representation is shown in Fig. 1. The action of the Toffoli gate is given by $|a\rangle|b\rangle|c\rangle \rightarrow |ab\rangle \oplus c\rangle$, that is, if the control qubit $|x\rangle$ and $|y\rangle$ are set to $|\mathbf{1}\rangle$ at the same time, then the target qubit will be flipped, otherwise the target qubit will be let alone. Thus, the matrix representation of Toffoli gates are

$$T(1,2,3) = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \end{pmatrix},$$

$$T(1,3,2) = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \end{pmatrix},$$

$$T(2,3,1) = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \end{pmatrix}.$$

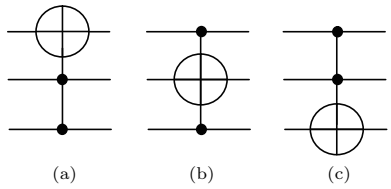


Fig. 1. The Toffoli gate: (a) T(2,3,1), (b) T(1,3,2), and (c) T(1,2,3).

The Fredkin gate (F) is a 3×3 reversible gate, and also a three-qubit quantum gate. The quantum cost of Fredkin gate is five, which was optimized in Ref. [22]. There are three possible Fredkin gates for a 3×3 circuit. The circuit representation is shown in Fig. 2. The action of the Fredkin gate is that, if the control qubit $|x\rangle$ is set to $|1\rangle$, then swap the values of the other two qubits, otherwise the gate will do nothing. Thus, the matrix representations of Fredkin gates are

$$F(1,2,3)=\begin{pmatrix}1&0&0&0&0&0&0&0\\0&1&0&0&0&0&0&0\\0&0&1&0&0&0&0&0\\0&0&0&1&0&0&0&0\\0&0&0&0&1&0&0&0\\0&0&0&0&0&0&1&0\\0&0&0&0&0&1&0&0\\0&0&0&0&0&0&0&1\end{pmatrix},$$

$$F(2,1,3)=\begin{pmatrix}1&0&0&0&0&0&0&0\\0&1&0&0&0&0&0&0\\0&0&1&0&0&0&0&0\\0&0&0&0&0&0&1&0\\0&0&0&0&1&0&0&0\\0&0&0&0&0&1&0&0\\0&0&0&1&0&0&0&0\\0&0&0&0&0&0&0&1\end{pmatrix},$$

$$F(3,1,2)=\begin{pmatrix}1&0&0&0&0&0&0&0\\0&1&0&0&0&0&0&0\\0&0&1&0&0&0&0&0\\0&0&0&0&0&1&0&0\\0&0&0&0&1&0&0&0\\0&0&0&1&0&0&0&0\\0&0&0&0&0&0&1&0\\0&0&0&0&0&0&0&1\end{pmatrix}.$$

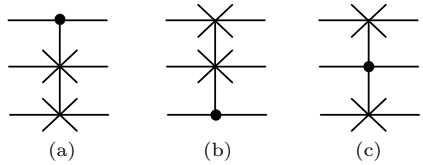


Fig. 2. The Fredkin gate: (a) F(1,2,3), (b) F(3,1,2), and (c) F(2,1,3).

The R^n gate is an n-qubit universal reversible gate, we can make a universal gate library only used R^n gate. It was first introduced in Ref. [15] and used to construct a full adder/substractor in Ref. [16]. It combines the functionality of the NOT gate, the CNOT gate and the Toffoli gate. We will make a multiplier using R^3 gate, so we introduce R^1, R^2 and R^3 only.

The R^1 gate is just like NOT gate, it is a 1×1 gate, and flips the input qubit unconditionally. The quantum cost of R^1 gate is zero.

The R^2 gate is a combine of NOT gate and CNOT gate. If the control qubit is set to $|1\rangle$ then the target qubit is flipped, otherwise the target qubit is let alone, then flips the control qubit unconditionally. The quantum cost of R^2 gate is one. There are two possible R^2 gate for a 2×2 circuit. Figure 3 shows the circuit representation. It can be represented by

$$R^2(1,2)=\begin{pmatrix}0&0&1&0\\0&0&0&1\\0&1&0&0\\1&0&0&0\end{pmatrix},\ R^2(2,1)=\begin{pmatrix}0&1&0&0\\0&0&1&0\\0&0&0&1\\1&0&0&0\end{pmatrix}.$$

Thus R^2 gate is a quantum gate.

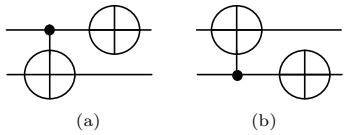


Fig. 3. The R^2 gate: (a) R(1,2) and (b) R(2,1).

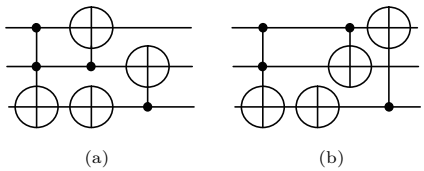


Fig. 4. The R^3 gate: (a) R(3,1,2), (b) R(1,3,2). We do not list all representations of R^3 gate, the others are similar to these two examples.

The R^3 gate is a three-qubit gate, the function of this gate can be described as follows: firstly use $|x\rangle$ and $|y\rangle$ as control bits to flip $|z\rangle$. Secondly $|x\rangle$ is used as a control bit to flip $|y\rangle$, then flips $|z\rangle$ unconditionally. Finally use $|z\rangle$ as control bit to flip $|x\rangle$. The quantum cost of R^3 gate can be optimized to four with moving rules.[23][24] There are six possible R^3 gates for a 3×3 circuit. Figure 4 shows the circuit representation and figure 5 shows the optimization process. It is easy to calculate the matrix corresponding to each R^3 gate, we list the calculation results in the following:

$$R^3(1,2,3)=\begin{pmatrix}0&0&1&0&0&0&0&0\\0&0&0&1&0&0&0&0\\0&0&0&0&0&0&0&1\\0&0&0&0&1&0&0&0\\0&0&0&0&0&1&0&0\\0&0&0&0&0&0&1&0\\1&0&0&0&0&0&0&0\\0&1&0&0&0&0&0&0\end{pmatrix},$$

$$R^3(1,3,2)=\begin{pmatrix}0&1&0&0&0&0&0&0\\0&0&0&0&0&0&0&1\\0&0&0&1&0&0&0&0\\0&0&0&0&1&0&0&0\\0&0&0&0&0&0&1&0\\1&0&0&0&0&0&0&0\\0&0&0&0&0&1&0&0\\0&0&1&0&0&0&0&0\end{pmatrix},$$

$$R^3(2,1,3)=\begin{pmatrix}0&0&0&0&1&0&0&0\\0&0&0&1&0&0&0&0\\0&0&0&0&0&0&1&0\\y0&0&0&0&0&1&0&0\\0&0&0&0&0&0&0&1\\y1&0&0&0&0&0&0&0\\0&1&0&0&0&0&0&0\\y0&0&1&0&0&0&0&0\end{pmatrix},$$

$$R^3(2,3,1)=\begin{pmatrix}0&0&0&0&1&0&0&0\\y0&0&0&0&0&1&0&0\\0&0&0&1&0&0&0&0\\0&0&0&0&0&0&1&0\\0&0&0&0&0&0&0&1\\0&0&1&0&0&0&0&0\\1&0&0&0&0&0&0&0\\0&1&0&0&0&0&0&0\end{pmatrix},$$

$$R^3(3,1,2)=\begin{pmatrix}0&1&0&0&0&0&0&0\\0&0&0&0&0&0&0&1\\0&0&0&0&0&0&1&0\\1&0&0&0&0&0&0&0\\0&0&0&0&0&1&0&0\\0&0&1&0&0&0&0&0\\y0&0&0&1&0&0&0&0\\0&0&0&0&1&0&0&0\end{pmatrix},$$

$$R^3(3,2,1)=\begin{pmatrix}0&0&1&0&0&0&0&0\\0&0&0&0&0&1&0&0\\0&0&0&0&0&0&0&1\\1&0&0&0&0&0&0&0\\0&0&0&0&0&0&1&0\\0&0&0&1&0&0&0&0\\0&1&0&0&0&0&0&0\\0&0&0&0&1&0&0&0\end{pmatrix}.$$

As a result, R^3 gate is a quantum gate.

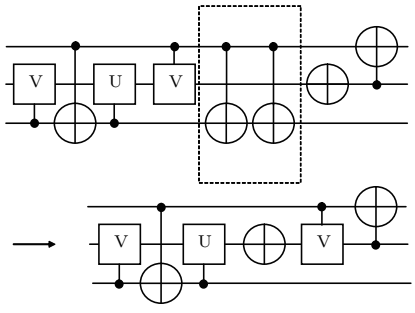


Fig. 5. The optimization process.

4. Proposed multiplier

In this section, we propose three new designs, which are a half adder, a full adder and a multiplier, designed using R gate.

The half adder can be used to calculate the operation $S=X+Y$ and to carry out bit C. The combination of $R^3(3,1,2)$ and $R^2(2,1)$ can do this. We use three input qubits, i.e., $|x\rangle$, $|y\rangle$, which is the target value, and a constant qubit $|0\rangle$. We can obtain three output qubits, the first one is the summation bit S_i, the second one is a garbage bit, and the third one is the carry out bit C_i. The quantum cost of our half adder is four. Figure 6 shows the proposed half adder.

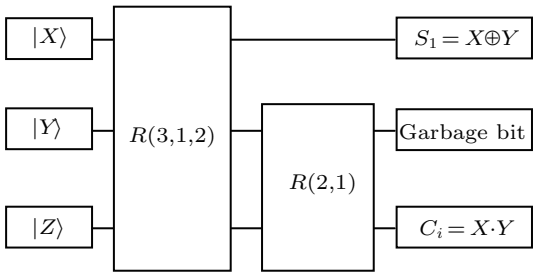


Fig. 6. The half adder using R gate.

Using this half adder, we can make a full adder. Figure 7 shows the full adder. This design uses two half adders and one constant bit to produce two garbage bit, the quantum cost of this full adder is six. Figure 8 shows the optimized process.

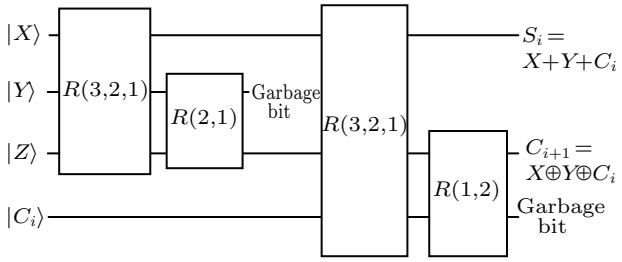


Fig. 7. The full adder using R gate.

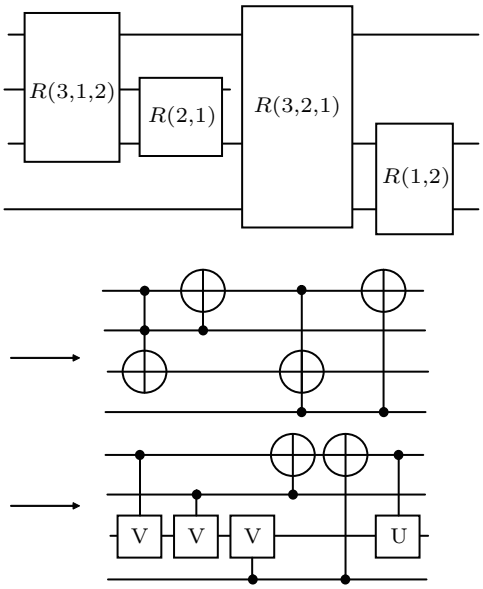


Fig. 8. The optimization process.

Now we can apply our half adder and full adder to build a multiplier. A multiplier consists of a partial product generator circuit (PPCG) and a reversible parallel adder (RPA), we

use the partial product generator circuit proposed in Ref. [14], then give the structure of an array multiplier in Fig. 9.

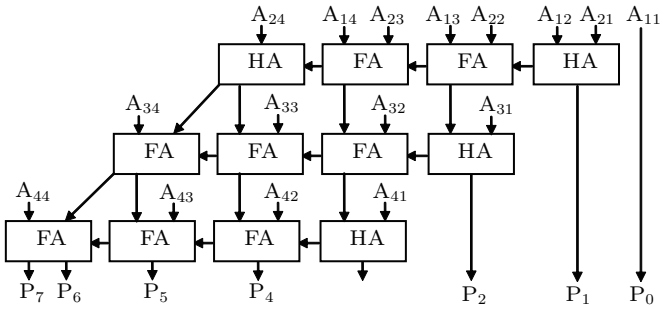


Fig. 9. RPA circuit.

It should be noted that the PPCG proposed in Ref. [14] uses only Toffoli gate, whereas we choose R gate library instead of NCT gate. This means that we need more R gate to synthesize a Toffoli gate in order to use this PPCG. However, it is worth. On the one hand, this circuit produces the lowest garbage bit, which is of great importance in a quantum computer. On the other hand, based on the view of Ref. [14] more quantum gates do not means more quantum cost. After simplification, we use the same numbers of N, V and U gates, which mean that in actual use, they do not make any difference, as a result, the gate number is out of consideration in this paper.

Finally, we compare our designs with the previous work in Tables 1 and 2. Table 1 shows the comparison of different full adders, and Table 2 shows the comparison of different multipliers. It is easy to see from Table 1 that our design has lower quantum cost than the existing design using R gate,[16] and have the same garbage bit and quantum cost as the existing design,[14] which means that it is the best design. From Table 2, we can see that our design is better than using the full adder proposed in Ref. [16] and has the lowest total cost.

Table 1. Comparison of the full adder.

	Garbage bit	Quantum cost	Total cost
Our proposed full adder	2	6	8
Full adder/substractor[16]	1	8	9
Existing full adder[13]	2	8	10
Existing full adder[14]	2	6	8

Table 2. Comparison of full adder.

	Garbage bit	Quantum cost	Total cost
Our proposed multiplier	28	144	172
Existing multiplier[16]	28	160	188
Existing multiplier[14]	28	144	172
Existing multiplier[13]	52	140	192

5. Conclusions and discussion

We have shown the quantum legitimacy of some common reversible gate and given a new design of multiplier. It is very meaningful to show the quantum legitimacy of reversible gates. The difference between a reversible gate and a quantum gate is that a reversible use takes zero or one as the input while a quantum gate takes vector $|\mathbf{0}\rangle$ and $|\mathbf{1}\rangle$ as the input. However, giving a matrix representation to a reversible gate means that it can deal with a vector input, which means that many results based on reversible gates can be applied to quantum computer directly, and promote the research and development of related interdisciplinary subjects.

Our designs use local optimization rule in order to achieve the limit optimization of quantum cost and garbage bit, in this point it is similar to the existing design. However, compared with existed designs, our designs have lots of differences and advantages. The most obvious thing is that we use a new library. Our new designs are based on R gate library. R gate library is better than other gate libraries in many ways such as the size of minimal universal sub libraries, utilization of gate, the minimal length and so on. As a result, under the same condition, R gate library is a better choice than NCT gate libraries. However, as shown in Table 2, the multiplier using the previous adders is not optimal. Our designs make up for its defects in the multiplier part, and make the R gate library more advantageous in theoretical research and practical use. Moreover, our design pays more attention to the optimization of garbage bit, although it uses a little more gates, but it is worth. Regarding the comparison between our designs and the previous results, we have carried out a detailed analysis in Tables 1 and 2.

References

[1] Grover L K 1997 *Phys. Rev. Lett.* **79** 325
[2] Shor P W 1999 *Siam Rev.* **41** 303
[3] Landauer R 1961 *IBM J. Res. Dev.* **5** 183
[4] Das K and De D 2010 *Int. J. Nanosci.* **09** 201
[5] Chee Y H, Niknejad A M and Rabaey J 2006 *IEEE J. Solid-State Circuits* **41** 1740
[6] Shamir J, Caulfield H J, Micelli W J and Seymour R J 1986 *Appl. Opt.* **25** 1604
[7] Cervantes-Salido V M, Jaime O, Brizuela C A, Israel M and Pérez M 2013 *Appl. Soft Comput.* **13** 4594
[8] Zhang J, Albelda M T, Liu Y and Canary J W 2005 *Chirality* **17** 404
[9] Ritter S, NLleke C, Hahn C, Reiserer A, Neuzner A, Uphoff M, Mücke M, Figueroa E, Bochmann J and Rempe G 2012 *Nature* **484** 195
[10] Ni L, Guan Z and Zhu W 2010 *Third International Symposium on Intelligent Information Technology and Security Informatics*, April 2–4, 2010, Jinggangshan, China, pp. 109–113
[11] Thersesal T, Sathish K and Aswinkumor R 2015 *Int. J. Sci. Res. Publ.* **5** 1
[12] Rangaraju H G, Venugopal U, Muralidhara K N and Raja K B 2010 *International Conference on Advances in Communication, Network, and Computing* (Berlin: Springer)
[13] Islam M S and Islam M R 2005 *Asian J. Inf. Technol.* **4** 1146
[14] Banerjee A and Pathak A 2009 arXiv:0907.3357.1
[15] Montaser R, Younes A and Abdelaty M 2017 *Quantum Matter* **2017** 1403
[16] Montaser R, Younes A and Abdel-Aty M 2019 *Int. J. Theor. Phys.* **58** 167
[17] Morrison M, Lewandowski M, Meana R and Ranganathan N 2011 *11th IEEE International Conference on Nanotechnology*, August 15–18, 2011, Portland, OR, USA, pp. 417-420

[18] Miller D M and Sasanian Z 2010 *53rd IEEE International Midwest Symposium on Circuits and Systems*, August 1–4, 2010, Seattle, WA, USA, pp. 260–263

[19] Bhuvana B P and Bhaaskaran V S K 2018 *Quantum Cost Optimization of Reversible Adder/Subtractor Using a Novel Reversible Gate* in *Innovations in Electronics and Communication Engineering. Lecture Notes in Networks and Systems* ed Saini H, Singh R and Reddy K Vol. 7 (Singapore: Springer)

[20] Rahman M M, Banerjee A, Dueck G W and Pathak A 2011 *41st IEEE International Symposium on Multiple-Valued Logic*, May 23–25, 2011, Tuusula, Finland, pp. 86–92

[21] Nielsen M A and Chuang I L 2011 *Quantum Computation and Quantum Information* 10th Anniversary Edition (Cambridge: Cambridge University Press)

[22] Patel R B, Ho J, Ferreyrol F, Ralph T C and Pryde G J 2016 *Sci. Adv.* **2** 1501531

[23] Iwama K and Yamashita S 2003 *New Generation Comput.* **21** 297

[24] Miller D M, Maslov D and Dueck G W 2003 *Transformation Based Algorithm for Reversible Logic Synthesis* (New York: Association for Computing Machinery) p. 318