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Characteristic enhancement in tunnel field-effect transistors via introduction of vertical graded source*

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A novel vertical graded source tunnel field-effect transistor (VGS-TFET) is proposed to improve device performance. By introducing a source with linearly graded component, the on-state current increases by more than two decades higher than that of the conventional GaAs TFETs without sacrificing the subthreshold swing (SS) due to the improved band-to-band tunneling efficiency. Compared with the conventional TFETs, much larger drive current range can be achieved by the proposed VGS-TFET with SS below the thermionic limitation of 60 mV/dec. Furthermore, the minimum SS about 20 mV/dec indicates its promising potential for further ultralow power applications.

Keywords: vertical graded source, band-to-band tunneling (BTBT), tunnel field-effect transistor (TFET)

PACS: 85.30.Mn, 81.05.Ea, 85.30.Tv **DOI:** 10.1088/1674-1056/ab7d99

1. Introduction

The continuous success in the fourth industrial revolution including artificial intelligence and Internet of Things demands for the rapid advances in low-power semiconductor logic devices. Unfortunately, with the dimensional scaling near material and impurity distribution limits,[1,2] conventional CMOS logic is approaching fundamental limitations and the fabrication processing becomes increasingly challenging. A more problematic issue is power constraint, especially the dynamic power consumption that is proportional to the square of supply voltage (V_{DD}), which restricts the activity and functionality possible for kinds of applications. Hence, it is an effective method to reduce the supply voltage for the Gordian knot of power consumption decrease. However, the subthreshold swing (SS) of MOSFETs cannot be reduced below 60 mV/dec at room temperature due to the Fermi tails in carrier distribution and the working mechanism of thermal electron emission, which would hinder the supply voltage scaling when a sufficiently high ratio of on-state current/off-state current (I_{ON}/I_{OFF}) is required for noise margins and immunity.

Recently, this challenge has attracted plenty of interests in steep slope device researches.[3–8] As one of the most promising candidates in meeting the demands for low power applications, tunnel field-effect transistors (TFETs) can achieve lower SS than the thermal limitation of 60 mV/dec relying on the temperature-independent quantum band-to-band tunneling (BTBT).[9–12] However, the commercialization of TFETs is blocked by several shortcomings, such as low I_{ON}, SS degradation and ambipolar switching effect.[13] For the Si-based TFETs,[14,15] the on-state current has been restricted due to inefficient interband tunneling in indirect semiconductors. Some studies are reported to improve on-state current by modifying structures or using narrow and direct bandgap semiconductor materials,[16–22] in which the subthreshold characteristics would be degraded simultaneously due to the increased off-state current and ambipolar tunneling, thereby leading to higher power consumption and the additional process complexity. In Ref. [23], a lateral graded source has been introduced in TFETs to further increase I_{ON} by the valence band modulation. However, the broken bandgap at the uniform hetero-junction would also enhance the I_{OFF} and degenerate the SS,[24] which suggests that such devices still need to be improved for the subthreshold and off characteristics.

In this paper, a novel vertical graded source tunnel field-effect transistor (VGS-TFET) is proposed for further improving device performance, which is studied by using the 2-D Technology Computer-Aided Design (TCAD) simulator. By employing a vertical linearly graded source to form the graded tunnel junction with the uniform channel, the proposed device is expected to achieve high I_{ON} and low I_{OFF} simultaneously. Furthermore, small SS over a wide range of drain current is obtained as well. The optimization on a significant factor to determine the device characteristics is also discussed.

2. Device structure and operation principle

Figure 1(a) shows the proposed VGS-TFET structure, in which the source is formed with graded $In_mGa_{1-m}As$ material and the Indium mole fraction m is supposed to increase lin-

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early from 0 to 1 along the vertical direction compared with the uniform source of conventional TFET in Fig. 1(b). This suggests that the top of the source in VGS-TFET is GaAs ($E_g^{GaAs} = 1.42$ eV) with a relatively wider bandgap, the center is narrower-bandgap InGaAs (E_g^{InGaAs} between 0.36 eV and 1.42 eV) and the bottom is InAs ($E_g^{InAs} = 0.36$ eV). In order to restrain the leakage current, GaAs as the wider bandgap material is still adopted in the channel and the drain region.

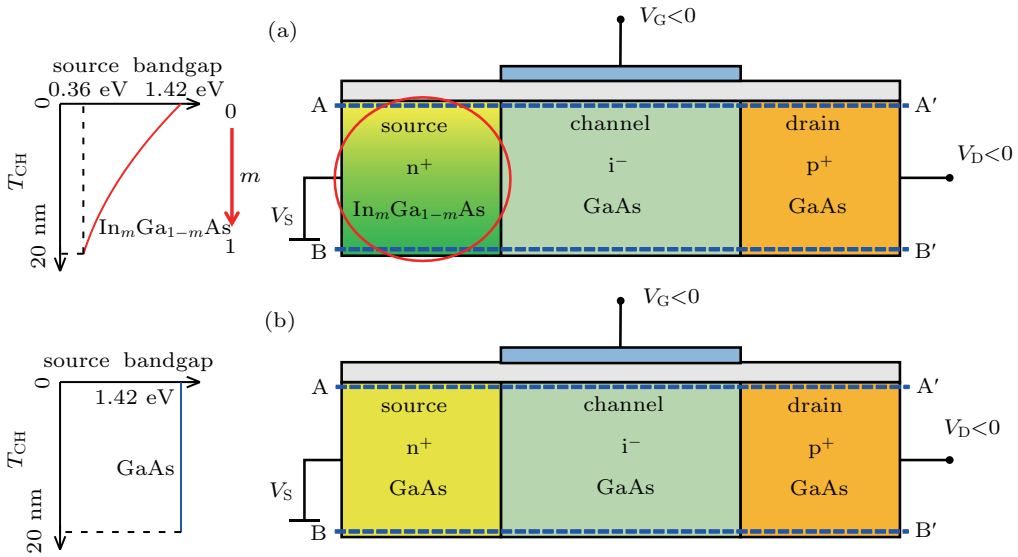


Fig. 1. Source bandgap variations and cross-sectional schematics of (a) the studied VGS-TFET and (b) the GaAs conventional TFET.

Device simulations are carried out using the 2-D TCAD simulation tools and the dynamic nonlocal path BTBT model is applied to account for the arbitrary tunneling barrier with nonuniform electrical field. The graded $In_mGa_{1-m}As$ source epitaxial growth would introduce the lattice strain, which would affect the band structure accordingly. For TFET devices, the influences of the band structure change including band gap width on device characteristics are contained in two key parameters of the dynamic nonlocal path BTBT model, A and B, which include the information of the energy band structure, such as the effective mass of the tunneling carrier and the material band gap width, and both of them can be obtained through the experimental data in Refs. [25,26]. Shockley–Read–Hall (SRH) recombination, drift-diffusion, doping-dependence and high-field dependence of mobility models are also included. The quantum modifications (eQuantumPotential and hQuantumPotential) with respect to the density of states of electrons and holes are used as well. The involved parameters are calibrated with Refs. [25,26]. Figure 2 shows the calibration results with the data from experimental work,[27] in which the simulation results match well with the band-to-band tunneling current of the experimental data in the on state. The channel thickness T_{CH} is 20 nm and the gate dielectric is HfO_2 with thickness T_{OX} of 2 nm. In order to suppress short-channel effects, the gate length L_G is set as 100 nm.[28] The source is n-type doped with a donor concentration N_S of 5×10^{19} cm^{-3}, while the drain is p-type doped with an acceptor concentration N_D of 5×10^{19} cm^{-3}.[26,29] The channel is very lightly doped with the doping concentration of 5×10^{15} cm^{-3}. The gate work function is set to make I_D equal to -1×10^{-16} A/μm at zero gate biasing.

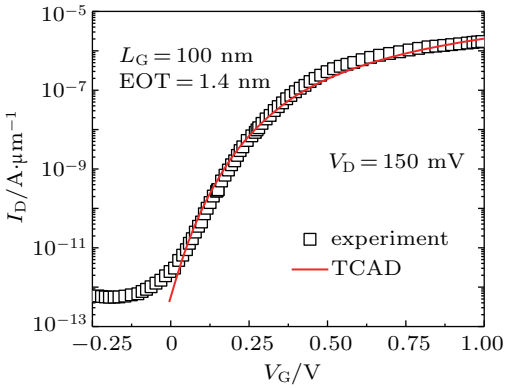


Fig. 2. Calibrations of the nonlocal tunneling model for the InGaAs TFET. L_G is set as 100 nm in the simulation because the gate length scaling has a very weak impact on device characteristics.[30]

Thanks to the introduction of the graded source, the tunnel junction becomes a graded $In_mGa_{1-m}As$/GaAs heterojunction in the VGS-TFET, which is the key to the performance boost. The simulated band diagrams of VGS-TFET, GaAs-TFET and InAs-TFET are depicted in Fig. 3. As can be seen in Fig. 3(a), the band diagrams of VGS-TFET in the top region are quite like the band diagrams of the GaAs homo-junction TFET with wider bandgap along the cutline A–A′ in Fig. 1, which is crucial for restraining leakage current. When the gate voltage V_G is very small, the maximal electric field dominating the tunnel junction is near the surface and the electric field decreasing along the vertical direction just has mild influence on band-to-band tunneling in the center and the bottom region. Therefore, the off-state current of VGS-TFET

is very small since the wider bandgap is not conducive to band-to-band tunneling. In addition, the GaAs channel/drain homo-junction with wider bandgap is adopted for achieving low leakage current and effectively restraining the ambipolar effect that severely affects the performance of narrow-gap devices (such as InAs-TFET), which contributes a desirable off-state characteristic to the VGS-TFET.

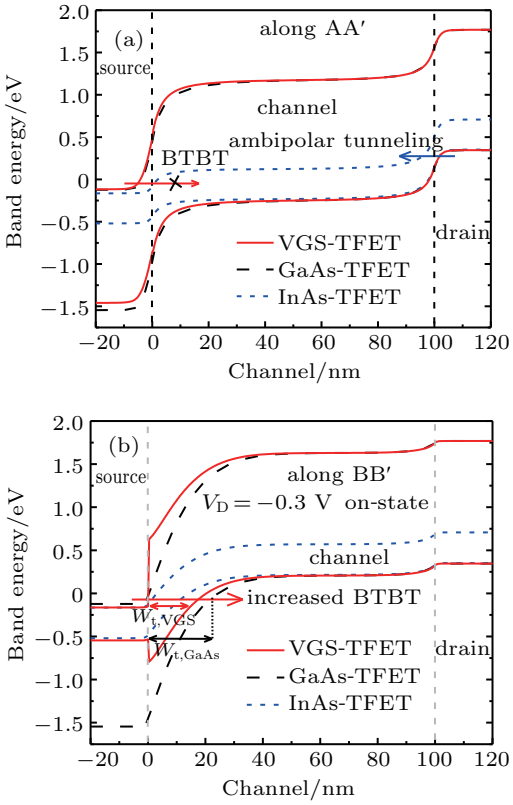


Fig. 3. Band diagrams of the tunnel junction for VGS-TFET, GaAs-TFET and InAs-TFET, respectively, (a) at the off state along the cutline A–A′ (at the distance of 1 nm below the channel surface) and (b) at the on state along the cutline B–B′ (at the distance of 1 nm above the channel bottom).

On the other hand, with V_G increasing and the device turning on, the gate control capability over the center and bottom of the tunnel junction is also enhanced. Owing to the graded source bandgap narrowing, the tunnel distances of the VGS-TFET ($W_{t,graded}$) in the bottom region are much shorter than that of the GaAs homo-junction TFET as shown in Fig. 3(b). Regarding Kane's theory,[31] the BTBT generation rate G_{BTBT} would rise exponentially with comshortened tunnel distance $G_{BTBT} \propto \exp(-W_t)$ obviously, which means that the tunnel current would be greatly improved ($I_D = \int G_{BTBT} d\Omega$) and the VGS-TFET is expected to perform better with higher tunnel current than the conventional GaAs homo-junction TFETs in the on state.

3. Device characteristics and discussion

The transfer characteristics of the proposed $In_mGa_{1-m}As$/GaAs VGS-TFET are compared to GaAs TFET, InAs TFET and InAs/GaAs hetero-junction TFET in Fig. 4(a). Obviously, the VGS-TFET can achieve improved on-state current and subthreshold characteristic compared with GaAs conventional TFETs. The on-state current of the VGS-TFET is more than one hundred times larger than that of the GaAs conventional TFET, which indicates the great contribution of the graded $In_mGa_{1-m}As$ source with high BTBT generation to tunnel current enhancement. From another aspect, compared with the InAs TFET, VGS-TFET can obtain much lower off-state current that remains the same level as GaAs TFET attributed to the wider bandgap of the top source material, and the ambipolar effect is effectively restrained as well owing to the wider-bandgap GaAs channel/drain homo-junction against ambipolar tunneling.

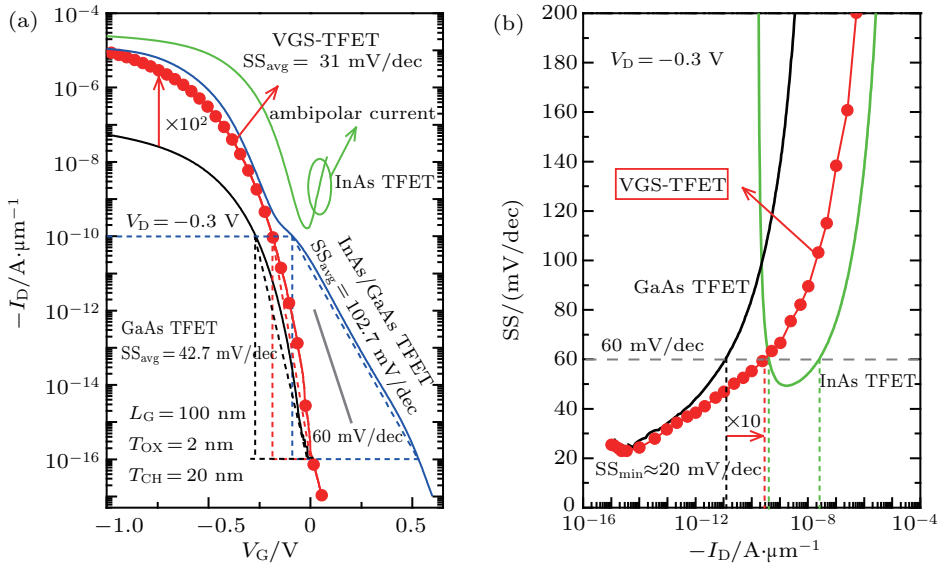


Fig. 4. (a) Transfer characteristics of the $In_mGa_{1-m}As$/GaAs VGS-TFET in comparison with the GaAs conventional TFET, InAs homo-junction TFET and InAs/GaAs hetero-junction TFET for $V_D = -0.3$ V. (b) SS of the VGS-TFET as a function of drain current compared with the conventional TFET.

Meanwhile, the wider bandgap material in the top source region effectively limiting the leakage current is also the key to guarantee the excellent subthreshold characteristic. As a result, a very high ratio of on-state current/off-state current (such as 10^6) of VGS-TFET can be obtained with the gate voltage just varying no more than 0.2 V in Fig. 4(a). This also means that a very small average subthreshold swing would be achieved. Here V_T is extracted by the constant current method using the threshold current I_T set as -10^{-10} A/μm. The average subthreshold swing is defined as $SS_{avg} = |V_T - V_0|/\log(I_T/I_0)$, where the I_0 defined as the turn-off current is set as -10^{-16} A/μm corresponding to the turn-off voltage V_0, in which the TFET is just in off. For the VGS-TFET, the value of SS_{avg} is reduced to 31 mV/dec for the six decade variations of drain current, which is very conducive to further supplied voltage reduction.

In Fig. 4(b), the extracted SS of VGS-TFET as a function of drain current I_D is compared with the conventional InAs TFET and GaAs TFET. As can be seen in the figure, VGS-TFET can obtain a larger current range in which the corresponding SS is less than 60 mV/dec, when compared with conventional GaAs TFETs. And the current corresponding to SS = 60 mV/dec of VGS-TFET is over one order of magnitude higher than the current corresponding to SS = 60 mV/dec of the conventional GaAs TFET. In addition, the SS reaches the minimum about 20 mV/dec when the device is just turned into subthreshold region and the drain current is very small.

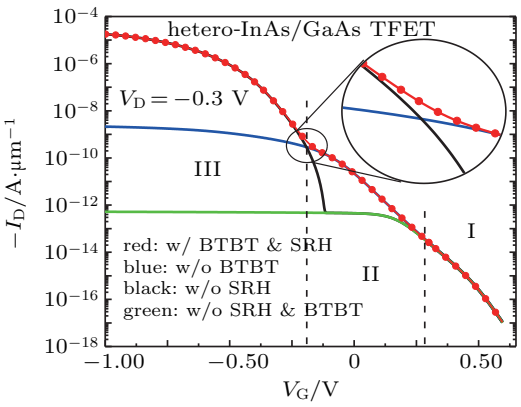


Fig. 5. The simulated transfer characteristics of the InAs/GaAs hetero-junction TFET for $V_D = -0.3$ V (red line) and the components of total drain current. In region I, the currents of band-to-band tunneling and SRH recombination are very small and the p–n junction inverse drifting current plays a dominant role in I_D. In region Ⅱ, the drain current mainly consists of the SRH recombination current. In region Ⅲ, the band-to-band tunneling current increases sharply to become the main part of I_D.

As is expected, the proposed $In_mGa_{1-m}As$/GaAs VGS-TFET exhibits the much steeper subthreshold characteristic simultaneously and high on-state current just slightly smaller than that of the InAs/GaAs hetero-junction TFET, via the adoption of the vertical graded $In_mGa_{1-m}As$ source modulating the band structures rather than the uniform narrow-gap InAs source. For the InAs/GaAs hetero-junction TFET, the tunnel current is very high due to the InAs/GaAs hetero-junction with thinner barrier for very high band-to-band tunneling generation rate. However, the hetero-junction also induces large leakage current to make the off-state worse and increase the static power consumption, which is undesirable for low-power applications. As shown in Fig. 5, the InAs/GaAs hetero-junction TFET has very high SRH recombination current and the p–n junction inverse drifting current that seriously hurts the subthreshold characteristics.

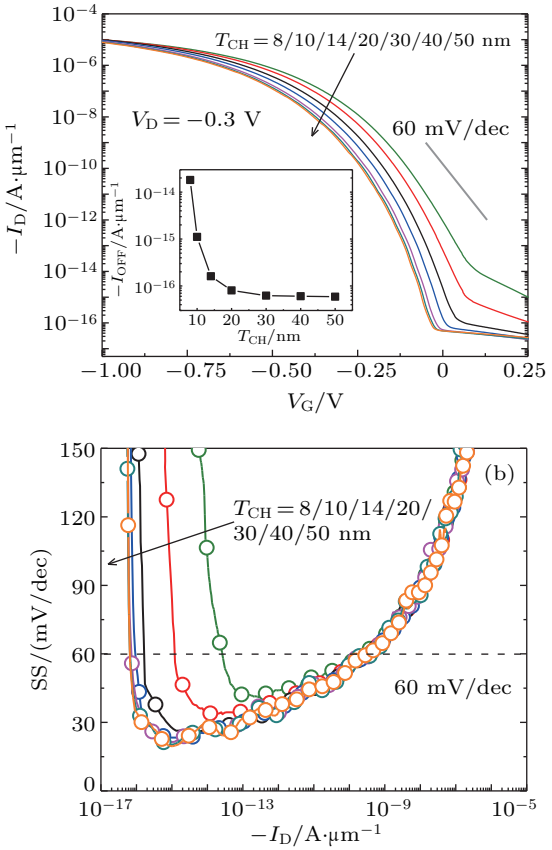


Fig. 6. (a) Transfer characteristics of the $In_mGa_{1-m}As$/GaAs VGS-TFET with different channel thickness T_{CH} at $V_D = -0.3$ V and (inset) leakage current I_{OFF} of the VGS-TFET versus T_{CH}. (b) SS of the VGS-TFET versus drain current with different T_{CH}.

In the proposed $In_mGa_{1-m}As$/GaAs VGS-TFET, the channel thickness is a significant parameter influencing the bandgap variation of graded source and the device characteristics. As shown in Figs. 6(a) and 6(b), thinner channel will make larger leakage current and degrade the subthreshold characteristics, because the gate control of the bottom channel is enhanced and the bottom hetero-junction would be opened for carrier tunneling before the device is turned on consequently. Meanwhile, higher on-state current is also achieved since the tunnel barrier causes more carriers tunneling and the BTBT generation is exponentially proportional to the enhanced electric filed in junction. However, the gate control of the channel would be screened and the differences of tunneling current are not obvious for different T_{CH} under this condition, because of a large number of carriers aggregating at the chan-

nel surface when the gate voltage is very large.[32] In addition, the leakage current and the subthreshold degradation could be restrained with the channel thickness increasing appropriately owing to the widened tunnel barrier and the weakened tunnel electric filed in junction. From Fig. 6, nevertheless, the device characteristics will not be sensitive to T_{CH} if the channel thickness over 30 nm, which suggests that the gate control of the bottom channel is very weak when the channel is too thick (such as $T_{CH} > 30$ nm). Furthermore, the thicker channel would cut down the drive current as well. Hence, there is a choice tradeoff for channel thickness between powerful drive current and good subthreshold characteristic. As depicted in Fig. 6, the VGS-TFET with T_{CH} of 20 nm can make high on-state current and admirable subthreshold characteristic, synchronously.

The decrease of the variation range of In component in the vertical graded $In_mGa_{1-m}As$ source means that the source would change from graded $In_mGa_{1-m}As$ to pure GaAs. The bottom tunnel junction would also change from low-tunnel-barrier narrow-gap/wide-gap hetero-junction to high-tunnel-barrier GaAs homo-junction accordingly. Therefore, the turn-on voltage of whole tunnel junction would be raised as shown in Fig. 7, meanwhile the on-state tunneling current would be reduced as well.

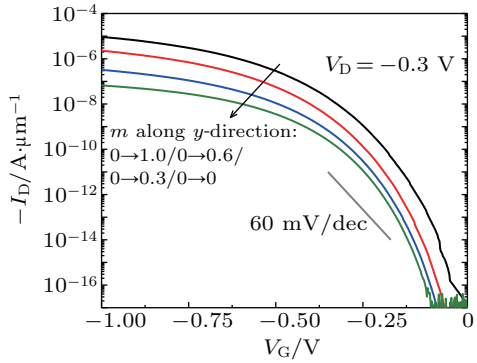


Fig. 7. The transfer characteristics of VGS-TFET with different variation ranges of In component in the vertical graded $In_mGa_{1-m}As$ source.

As discussed above, the proposed VGS-TFET has outstanding characteristics because of the vertical graded source, but the high quality graded hetero-epitaxy needs to be completed after a highly selective and anisotropic etching process for the vertical graded tunnel junction formation. The graded $In_mGa_{1-m}As$ source epitaxial growth would introduce the dangling bonds and interface defects due to lattice mismatch between source and channel, which may bring the defect energy levels in the band gap of tunnel junction to assist carriers tunneling early. Consequently, the leakage power dissipation and the threshold voltage may be affected. However, the aim of this work is mainly to present a new idea for the performance enhancement of TFETs. Thus, more details about the reliability of VGS-TFET need further discussion in the future work yet. In addition, the material system for the VGS-TFET is not just limited to GaAs/InGaAs. The lattice-matched material systems, such as InGaAs/GaAsSb, Ge/Si and the quaternary compound InGaAsP, are also perfect for the proposed VGS-TFET structure. Thus, the study of VGS-TFET is also meaningful for the long-term development the ultro-low power logical ICs.

4. Conclusion

In summary, a novel vertical graded source TFET is studied using the TCAD simulator, which demonstrates the outstanding performance, in which the VGS-TFET can effectively enhance the on-state current to improve driving capability and to suppress the SS degradation behavior to obtain much steeper switching slope simultaneously by applying the graded source structure. Compared with conventional homo-junction TFETs, the proposed VGS-TFET can also have much larger drive current range, in which the SS is below the thermionic limit 60 mV/dec, without leakage current degradation. Therefore, the results indicate the promising potential of VGS-TFET for further ultralow power logic and other innovative applications.

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