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TOPICAL REVIEW — Physics in neuromorphic devices

High-performance synaptic transistors for neuromorphic computing*

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The further development of traditional von Neumann-architecture computers is limited by the breaking of Moore's law and the von Neumann bottleneck, which make them unsuitable for future high-performance artificial intelligence (AI) systems. Therefore, new computing paradigms are desperately needed. Inspired by the human brain, neuromorphic computing is proposed to realize AI while reducing power consumption. As one of the basic hardware units for neuromorphic computing, artificial synapses have recently aroused worldwide research interests. Among various electronic devices that mimic biological synapses, synaptic transistors show promising properties, such as the ability to perform signal transmission and learning simultaneously, allowing dynamic spatiotemporal information processing applications. In this article, we provide a review of recent advances in electrolyte- and ferroelectric-gated synaptic transistors. Their structures, materials, working mechanisms, advantages, and disadvantages will be presented. In addition, the challenges of developing advanced synaptic transistors are discussed.

Keywords: synaptic transistor, artificial synapse, synaptic plasticity, electrolyte gating, ferroelectric gating

PACS: 07.05.Mh, 73.40.Mr, 85.30.Tv, 85.50.Gk **DOI:** 10.1088/1674-1056/ab7806

1. Introduction

Traditional digital computers based on the von Neumann architecture have been fully developed over the past few decades, and largely promoted the development of industry, science, and technology. They are ideal for solving structured problems, e.g., explicit mathematical problems, or processing precisely defined data sets.[1,2] Nevertheless, there are two main obstacles that hinder their further improvement: 1) Moore's law-based device scaling and the accompanying technology development have been significantly slowing down; 2) the physical separation of memory and data processing units increases the cost for "big data" movements, known as the von Neumann bottleneck.[3] These issues make von Neumann computers uncomparable with the human brain when dealing with uncertainty, ambiguity, and contradiction in the natural world.

Compared to von Neumann computers, the human brain works in a completely different fashion: 1) it is massively parallel and extremely compact, 2) it is power efficient, 3) it is fault-tolerant and robust, 4) it combines storage and computation, 5) it is self-learning and adaptive to changing environments.[1] The human brain consists of $\sim 10^{11}$ neurons connected by $\sim 10^{15}$ synapses, which control motion, thinking, learning, and memory.[4] As basic units of the human nervous system, synapses regulate the strengths of neuron connections, and simultaneously store and process information. When neuron spikes arrive at the synapses, the connection strength, i.e., the synaptic weight, is changed in a specific way.[5,6] This adaptability, also called synaptic plasticity, is considered to be the main principle underlying learning and memory functions in the brain.[7–9] Although the operating speed of a neuron or synapse is much slower than that of a complementary metal-oxide-semiconductor (CMOS) transistor, the parallel processing mechanism makes the biological brain outperform von Neumann computers and demonstrate superior performance when solving tasks like video or voice recognition, image analysis, etc., and with an ultralow energy consumption ($\sim$ 20 W) and a small volume occupation ($\sim$ 1200 cm^3).[10–13] Given the impressive computational performance of the human brain, a stream of research on "brain-inspired computing" (neuromorphic computing) has recently been presented.[14–21]

Currently, great efforts have being devoted to implement neuromorphic computing. One method is emulation at soft-

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ware level using CMOS integrated circuits. A more recent example is Intel's Loihi chip, announced in 2017, which has 128 neuromorphic cores, each containing 1024 primitive spiking neural units grouped into tree-like structures. The Loihi chip can implement not only inference but also self-learning using spike neural networks (SNNs).[22] However, such CMOS-based approaches often require tens of transistors to emulate a single neuron or synapse; the Loihi chip has 2.07 billion transistors to mimic around 131 thousand simulated neurons and 130 million synapses. They are energy intensive and limited in terms of further scalability due to the slowdown in CMOS scaling. Another method is the hardware implementation based on artificial neuromorphic devices. In the past decades, tremendous efforts have been devoted to implement artificial neurons and artificial synapses using a variety of emerging materials and devices.[1,23,24] Herein we mainly focus on the latter — artificial synapses. Initially, two-terminal memristors, such as resistive random access memory (RRAM),[25–28] phase-change memory (PCM),[29] ferroelectric random access memory (FRAM),[30] and magnetic random access memory (MRAM),[31,32] were investigated extensively as artificial synapses. These devices enabled several important advances in image recognition and data classification.[33,34] Recently, three-terminal synaptic transistors were presented as a more advantageous solution than two-terminal memristors due to their good stability, relatively controllable testing parameters, clear operation mechanism, and the capability to be constructed from a variety of materials.[35,36] A typical synaptic transistor has a structure shown in Fig. 1(b). The gate electrode is usually regarded as a pre-synaptic terminal for applying action potentials, i.e., pre-synaptic spikes. The channel layer with its source–drain electrodes is considered to be the post-synaptic membrane, whereas the channel conductivity is deemed the synaptic weight. The dielectric layer emulates the synaptic cleft and its material can be ionic electrolyte or ferroelectric. Taking ionic electrolytes for example, when voltage pulses are applied to the gate electrode, the active ions are gathered to the electrolyte/channel interface and even injected into the semiconductor channel, thereby further changing the source–drain conductance.[37] Therefore, signal transmission and self-learning can be performed simultaneously in such types of artificial synapses.[38,39] Moreover, a multi-gate configuration facilitates dynamic spatiotemporal information processing.[40–42] These features make synaptic transistors more suitable than two-terminal memristors for simulating synaptic functions. Although several review articles have been published in this field,[2,16,17,35–37,41–44] it is still necessary to investigate high-performance synaptic transistors from the viewpoint of dielectric materials.

In this topical review, the recent advances in high-performance synaptic transistors are discussed. The article is structured as follows. In Section 2, we introduce the key concept of synaptic plasticity and learning rules, including short-term plasticity, long-term plasticity, spike-timing-dependent plasticity, etc. In Section 3, we review electrolyte gated synaptic transistors (EGTs). These are classified into H^+-EGTs, metal ion EGTs, and O^{2-}-EGTs depending on the active ions. In Section 4, we review the ferroelectric gated synaptic transistors (FGTs), which consist of inorganic or organic ferroelectric dielectric layers. In Section 5, a few application instances of synaptic transistors are introduced. Finally, in Section 6 we provide the conclusion and perspectives of the entire review.

2. Synaptic plasticity and synaptic learning rules

In biological nervous systems, there are two types of fundamental synapses: electrical and chemical. Electrical synapses pass ionic current directly and mainly exist in invertebrates such as crustaceans and fishes, while chemical synapses constitute the majority of synapses in the human brain.[35] Thus, we will mainly focus on the latter. Figure 1(a) presents the schematic diagram of a chemical synapse, which mainly consists of the pre-synapse, the synaptic cleft, and the post-synapse. When the neuron's signal arrives at the pre-synaptic terminal, it causes the pre-synapse to release a neurotransmitter to the synaptic cleft. Then, some of the neurotransmitter binds the receptors on the post-synaptic terminal. Many of these receptors contain an ion channel capable of passing positively charged ions either into or out of the cell. At excitatory synapses, the ion channel typically allows sodium into the cell, generating an excitatory postsynaptic current/potential (EPSC/EPSP).[47] This makes the post-synaptic neuron more likely to generate an action potential. Conversely, inhibitory post-synaptic current/potential (IPSC/IPSP) is generated at inhibitory synapses and tends to drive the post-synaptic neuron away from the threshold for generating an action potential. In this way, the connection between two neurons is modulated, i.e., the weight of the synapse is changed via synaptic plasticity. Different forms of synaptic plasticity shape different synaptic outputs and form the foundation of learning and memory.[5,48] Classified by the retention time, the synaptic plasticity types can be generally grouped into short-term plasticity and long-term plasticity.

Short-term plasticity occurs at a timescale from milliseconds to seconds and can be categorized as short-term potentiation (STP) and short-term depression (STD).[5,48] STP/STD refers to the increase/decrease of synaptic transmission in a short-term mode, including paired-pulse facilitation/depression (PPF/PPD), post-tetanic potentiation (PTP), etc. PPF is a typical phenomenon in which the EPSC evoked by a pulse is increased when a second pulse follows closely.[48,49] The PPF ratio can be defined as PPF =

$(A_2/A_1) \times 100\%$, where A_1 and A_2 are the EPSC peaks of the first and second pulses, respectively. This ratio decreases with the increase of the time interval between the pair of pulses and can be approximated using a double decay function:[5] PPF $= C_1 \exp(-t/\tau_1) + C_2 \exp(-t/\tau_2) + 1$, where t is the interval between the two pulses. C_1 and C_2 are the initial facilitation magnitudes and τ_1 and τ_2 are the characteristic relaxation time of the rapid and slow phases, respectively. Conversely, PPD depicts a phenomenon in which the EPSC evoked by the second pulse is smaller than that of the first pulse, and its ratio increases with the increase of the time interval between the two pulses.[50–52] PTP is a transient enhancement of synaptic weight caused by intense consecutive synaptic activities in a short period of time;[48,53] in a way, it is like an extension of PPF. Figure 1(e) illustrates a PTP behavior triggered by ten repeated presynaptic spikes (0.8 V, 10 ms) at 50 Hz simulated using a synaptic transistor.[54]

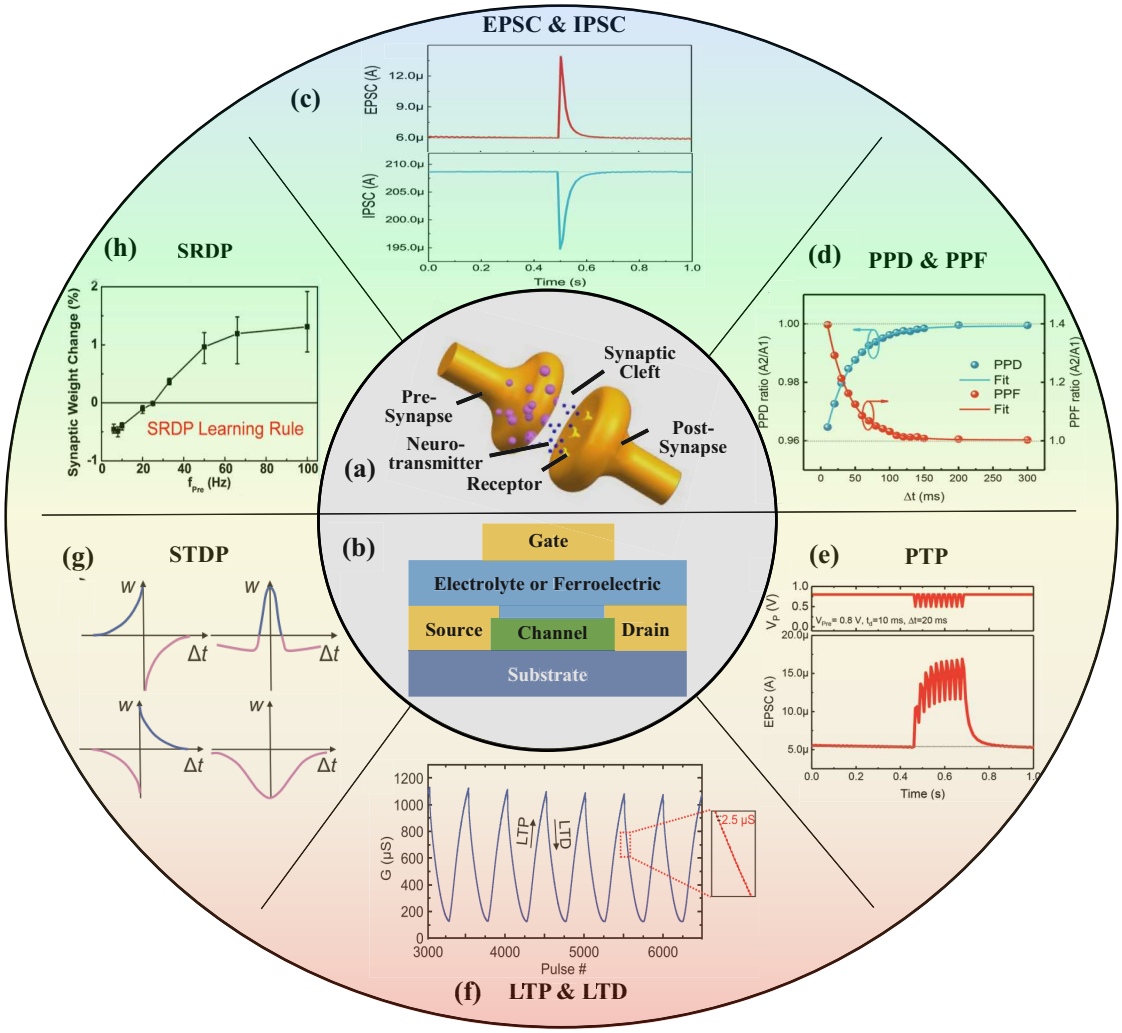


Fig. 1. (a) Schematic illustration of biological synapse. (b) Typical structure of synaptic transistor. (c)–(e) Typical postsynaptic current behaviors: (c) EPSC & IPSC; (d) PPD & PPF; (e) PTP. Reprinted with permission from Ref. [54]. Copyright 2019, John Wiley & Sons. (f) Demonstration of LTP & LTD. (g) Typical STDP behaviors. Reprinted with permission from Ref. [72]. Copyright 2018, John Wiley & Sons. (h) SRDP learning rule. Reprinted with permission from Ref. [68]. Copyright 2016, American Chemical Society.

Long-term plasticity can last for several hours or longer and can be categorized into long-term potentiation (LTP) and long-term depression (LTD), in which the synaptic strength can be permanently improved and diminished through repeated stimulation, respectively.[55,56] It is believed that the LTP is the key to our brain's memory formation.[57,58] In synaptic transistors, LTP/LTD can be implemented using electrochemical doping/de-doping of the channel layer or electric field control via ferroelectric switching.

Learning is the most important function of the biological brain, thus revealing the rules and theories of learning would be of great significant in achieving neuromorphic computing. As early as the 1940s, Hebb proposed a postulate of synaptic modification through correlated activities, which can be concisely described as "neurons that fire together wire together".[59] Developed for several decades, the Hebbian learning rule is mainly reflected in two kinds of plasticity: spike-timing-dependent plasticity (STDP) and spike rate-

dependent plasticity (SRDP).[2,3] STDP states that the change of synaptic weight is a function of the time difference between post-synaptic and pre-synaptic spikes.[7,60,61] It can be symmetric or asymmetric, as shown in Fig. 1(g). For asymmetric STDP function, when the pre-synaptic spike precedes the post-synaptic spike, the synaptic weight increases, while it decreases when the pre-synaptic spike occurs after the post-synaptic one. In both cases, the weight change is increased as the time difference decreases. SRDP is also one of the basic learning rules in human brains,[62,63] which states that the synaptic weight change is a function of the frequency of the pre-synaptic spikes.[23] According to SRDP learning rules, pre-synaptic pulses with high frequency result in potentiation, while those with low frequency result in depression.[64]

It can be said with certainty that synaptic plasticity is the biological basis for our brain's learning and memory functions. In fact, the knowledge of our brain's mechanisms is still quite limited. Even so, we can still try to realize the neuromorphic computing by simulating the structure and function of biological neural networks and synapses. In the following parts, different high-performance synaptic transistor-based mechanisms and materials will be reviewed.

3. Electrolyte gated synaptic transistors

In general, electrolytes are insulators of electrons and holes, but good conductors of ions. EGTs can use the ions in the electrolyte dielectric layer effectively to regulate the conductance of the channel. They mainly work in two ways. One is that the functional ions in the electrolyte move under the action of the applied gate electric field and gather on the interface between the semiconductor and the dielectric, thus forming a double electric layer with high capacitance. In the second, an electric double layer is also formed but as the gate field intensifies, functional ions in the electrolyte are inserted into the channel material to further regulate the channel conductance in a non-volatile manner. Since it can simulate both short-term and long-term synaptic plasticities, the latter regulation mechanism has become an important research topic. The functional ions in electrolytes are varied, and they can be cations or anions, such as H^+,[54,65–70] Li^+,[19,71–73] O^{2-},[74–77] etc. In this section, we will present EGTs utilizing different functional ions.

3.1. H^+-EGTs

Protons, the smallest-sized cations, exist in a wide range of electrolytes, inorganic, organic, solid, or liquid. Due to their small volume and light weight, protons in electrolytes can be easily driven using an external electric field and inserted into the lattice spacing of the channel layer. In 2014, Wan *et al.* proposed an indium-zinc-oxide-based synaptic transistor gated using phosphorus-doped SiO_2 nanogranular proton-conducting electrolyte films.[40] Synaptic plasticity functions, such as STDP (Fig. 2(b)) and PPF (Fig. 2(c)), were mimicked successfully. Moreover, the dynamic logic established through spatiotemporal spike measurements with two in-plane gates was investigated. Similar to this work, Yang *et al.* designed a synaptic transistor using WO_3 and ionic liquid (IL) (Fig. 2(d)).[78] The high-quality epitaxial WO_3, which can be regarded as a pseudo-perovskite oxide with absent A-site cations, was prepared on a $LaAlO_3$ substrate using laser molecular beam epitaxy (LMBE) technique.[79,80] The A-site absence provides sufficient interstitial space for ion intercalation and extraction, which makes WO_3 an excellent model material for artificial synaptic devices. In this work, short-term plasticity functions, such as PPF and PTP (Fig. 2(e)), as well as long-term plasticity (Fig. 2(f)) were investigated. To understand the working mechanism, figures 2(g)–2(j) give a visualized schematic of ion migration and relaxation of the gating dynamics. When a low positive bias is applied to the gate, protons in the IL will migrate and accumulate at the WO_3/IL interface. After removing the bias, the accumulated protons will diffuse back to their equilibrium positions due to the concentration gradient. Consequently, short-term synaptic plasticity was simulated. When a high positive (negative) bias is applied, protons can penetrate into (out of) the WO_3 channel, which will result in a permanent increment (decrement) of the channel conductance due to electrochemical doping. Thus, LTP and LTD were also simulated.

Compared to inorganic materials, organic materials have many unique advantages, such as cheap processing, easily changeable chemical structures, and large free volumes. In 2017, Salleo's group demonstrated a redox synaptic transistor, which used PEDOT: PSS as the channel layer and nafion as the electrolyte.[81] Moreover, the device was fabricated on a flexible PET substrate. This all-plastic device proved the potential of low-cost fabrication of transistor arrays, which might enable the integration of neuromorphic functionality in flexible large-area electronic systems. In 2019, Elliot *et al.* further combined the redox transistor with a conductive-bridge memory (CBM), and named it the ionic floating-gate memory (IFG).[14] Figures 3(a) and 3(b) give a schematic of the "write" and "read" states of the IFG. As with flash memory, the CBM allows current injection only above a threshold, i.e., when $|V^{\mathrm{w}}| > V_{\mathrm{th}} = \pm 400$ mV, and not during the OFF state. During programming, electron injection (extraction) through the CBM into the top PEDOT: PSS gate results in the reversible electrochemical oxidation (reduction) of the bottom PEDOT: PSS channel, thereby increasing (decreasing) the channel conductance. Excellent linear modulation of conductance was achieved (Fig. 3(c)). The authors further pioneered a crossbar array, as schematically illustrated in Fig. 3(d), and demonstrated selective addressing by subjecting one of the crossbar

elements to 50 weight updates without disturbing another element, as shown in Fig. 3(e). The IFG also has excellent endurance, as no degradation was observed after 10^8 write–read operations sampling the entire device range, as shown in Fig. 3(f). Regarding the speed aspect, though > 1-MHz write–read frequencies have been supported in current devices, the authors projected that further downscaled devices will enable < 100 ns switching (Fig. 3(g)). The proposed IFG concept can be generalized to a wide variety of electrochemical systems that can provide even greater performance with improved CMOS compatibility and that are yet unexplored for neuromorphic computing applications.

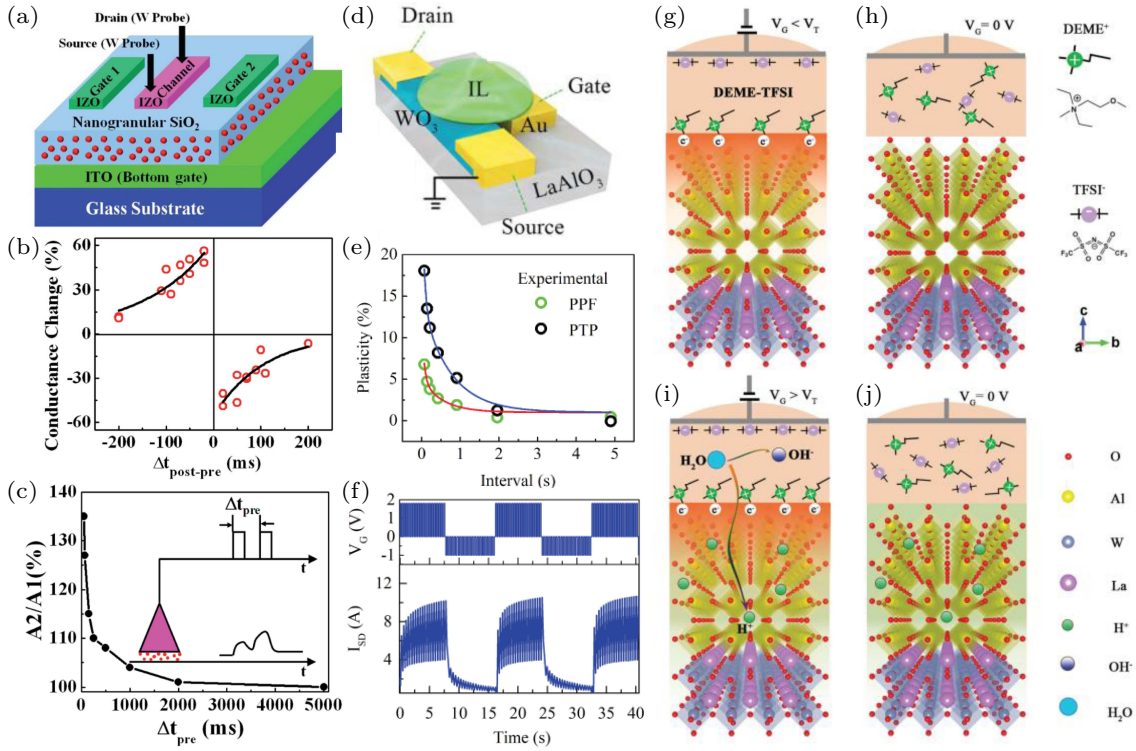


Fig. 2. (a) Schematic diagram of the oxide-based transistor. (b) STDP result of the oxide-based transistor. (c) PPF index plotted as a function of interval between two spikes. Reprinted with permission from Ref. [40]. Copyright 2014, RSC Pub. (d) Schematic diagram of WO_3–ionic liquid synaptic transistor. (e) PPF and PTP curves fitted with an exponential function. (f) Synaptic potentiation and depression. (g), (i) Schematic of ion migration and (h), (j) relaxation of gating dynamics. Reprinted with permission from Ref. [78]. Copyright 2018, John Wiley & Sons.

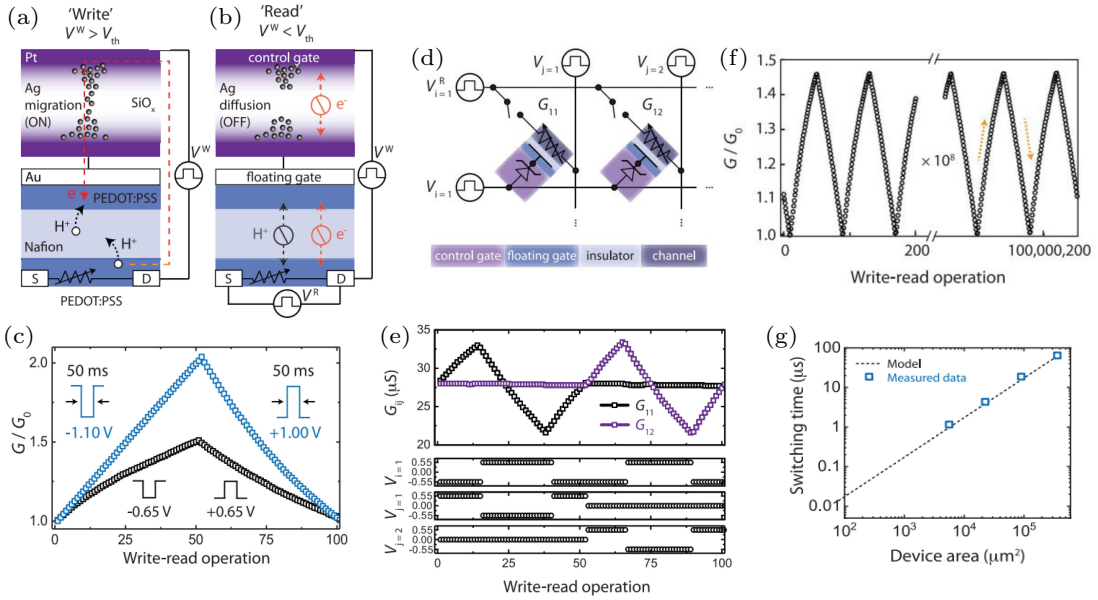


Fig. 3. (a) The "write" and (b) "read" states of an IFG cell consisting of a CBM and a redox transistor. (c) Programming of an IFG cell at two different write voltages. (d) Schematic of a 1-by-2 IFG resistive memory array. (e) Selective addressing by subjecting G_{11} or G_{12} to 50 weight updates without disturbing the adjacent element. (f) Demonstration of $> 10^8$ write–read operations without deterioration of device properties. (g) Estimated (dashed line) and measured (open squares) redox-transistor switching speed scaling with channel area. Reprinted with permission from Ref. [14]. Copyright 2019, American Association for the Advancement of Science.

Actually, many natural polymer materials are also good H^+-conducting electrolytes and can be used for synaptic transistor design. Wan's group in Nanjing University reported several achievements in this field. It is interesting to note that Wu *et al.* used natural chicken egg albumen with high proton conductivity to prepare the synaptic devices.[82] The device structure is shown in Fig. 4(b). Semiconductor indium zinc oxide (IZO) was selected to be the channel material, whose conductance was modulated via protons in the albumen. The ionic conductivity of albumen was mainly due to the presence of water, which facilitated proton transport. In the experiment, the spin-coated albumen films were only dried in ambient air without any thermal reaction treatment. Figure 4(c) shows the atomic force microscope (AFM) image of the indium tin oxide (ITO) glass after albumen coating, indicating that the spin-coated albumen film has a very smooth surface, which is favorable for device fabrication. Figure 4(d) shows the transfer curves measured at $V_{DS} = 2.5$ V with different bottom gate voltage sweeping ranges. The on/off ratio of this transistor can be as large as 10^6, which indicates an excellent modulation effect. Besides egg albumen, cellulose nanofibers[42] and chitosan membrane[83] have also been used as electrolyte materials to fabricate synaptic transistors. As shown in Figs. 4(e) and 4(f), both of them have a similar device structure — the IZO channel layer and multi-gate design. In these multi-gate synaptic transistors, the spiking logic operation and logic modulation were realized successfully.

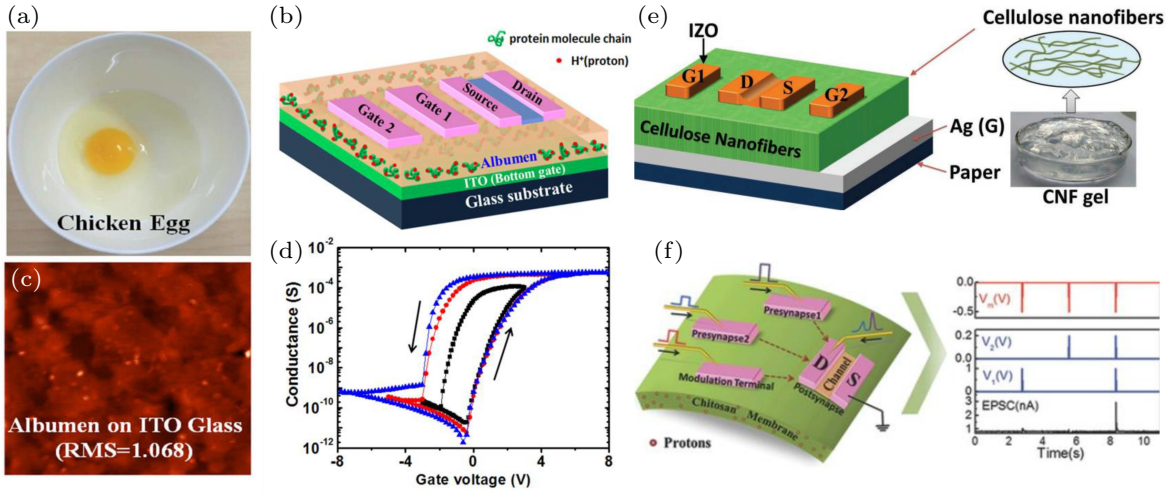


Fig. 4. (a) Broken chicken egg in a bowl. (b) Schematic diagram of albumen-gated IZO-based synaptic transistor with two in-plane gates. (c) Albumen film spin-coated on the ITO glass substrate (d) Ttransfer curves of the device. Reprinted with permission from Ref. [82]. Copyright 2016, Nature Publishing Group. (e) Schematic illustration of in-plane double-gate EDLT with CNF film used as the gate dielectric. A picture of the CNF hydrogel is given on the right. Reprinted with permission from Ref. [42]. Copyright 2017, John Wiley & Sons. (f) Freestanding synaptic transistors fabricated on solution-processed chitosan membranes. Reprinted with permission from Ref. [83]. Copyright 2015, John Wiley & Sons.

3.2. Ag^+- & Li^+-EGTs

Some heavier ions, such as Li^+, Ag^+, etc., have also been used as functional ions to modulate the channel layer's conductance. An early study was reported by Chen *et al.* in 2010,[84] where the synaptic transistor had the Si n–p–n source–channel–drain structure of a conventional MOS transistor, as shown in Fig. 5(a). Poly [2-methoxy-5-(20-ethylhexyloxy)-p-phenylene vinylene] (MEH-PPV)/$RbAg_4I_5$ layers were sandwiched between the p-Si channel and an Al/Ti electrode. Under the action of an external electric field, Ag^+ and I^- in $RbAg_4I_5$ can diffuse into the MEH-PPV polymer layer and further adjust the channel carrier concentration through the electrostatic coupling effect. Based on this principle, EPSC and STDP were realized with a very low energy consumption. After that, inspired by the lithium ion battery technology, Fuller *et al.* designed a battery-like synaptic transistor, which had the structure shown in Fig. 5(b).[73] A 400 nm-thick lithium phosphorous oxynitride electrolyte (LiPON) layer (green) was used to separate the $Li_{1-x}CoO_2$ channel (red) from a Si gate electrode (purple). This all-solid-state device is nonvolatile with a resistance switching mechanism based on the intercalation of Li-ion dopants into the $Li_{1-x}CoO_2$ channel. From the transfer curve of Fig. 5(c), we see that for the charging branch (negative I_G), the source–drain conductance G_{SD} increased, and after charging, a subsequent positive I_G discharged the device to near 0 V and returned it to the low-conductance state. In a selective conductance range, fairly linear potentiation and depression were obtained for neuromorphic computation, as shown in Fig. 5(d). What is more, for all 40 cycles, $G_{SD}(t)$ exhibited predictable, saw-tooth-like conductance ramps without degradation in the overall conductivity, indicating high write endurance for neuromorphic applications. In 2018, Zhu *et al.* also designed and fabricated a synaptic transistor with a Li^+-conducting electrolyte ($LiClO_4$ dissolved in polyethylene oxide (PEO), forming an ion gel) and a structure shown in Fig. 5(e).[71] In particular, the material used for the channel was a thin flake of transition metal dichalcogenide (TMDC) or phosphorus trichalcogenide, including WSe_2, $NiPS_3$, and $FePSe_3$. The working mechanism of such a device bears strong resemblance to bio-

logical synapses, as depicted in Fig. 5(f), where the migration and dynamic balance of Li^+ and Ca^{2+} concentrations play decisive roles in their respective systems. Two-stage ionic gating effects, namely, surface adsorption and internal intercalation in the channel layer, caused different post-stimulation diffusive dynamics and thus accounted for the short- and long-term plasticities. When a 5 V voltage pulse was applied to the gate, the EPSC characteristic was observed, while when a successive train of such pulses was applied, a transition from short-term plasticity to long-term plasticity could be clearly observed (Figs. 5(g) and 5(h)). The authors also found that the long-term weight change ($\Delta\omega/\omega_0$) of the WSe_2 channel had a dependence on the layer number of WSe_2. A relatively thin WSe_2 channel layer led to a low $\Delta\omega/\omega_0$ in devices due to the reduced interlayer position for ion intercalations. However, when the thickness of WSe_2 exceeded $\sim$ 35 layers, a significant increase in $\Delta\omega/\omega_0$ was observed due to the largely increased intercalation sites and possibly deeper intercalation (Fig. 5(i)). In addition, the complex functionalities, including PPF, LTP/LTD, SRDP, dynamic filtering, etc., with remarkable linearity, symmetry, and ultralow energy consumption have been realized using these devices.

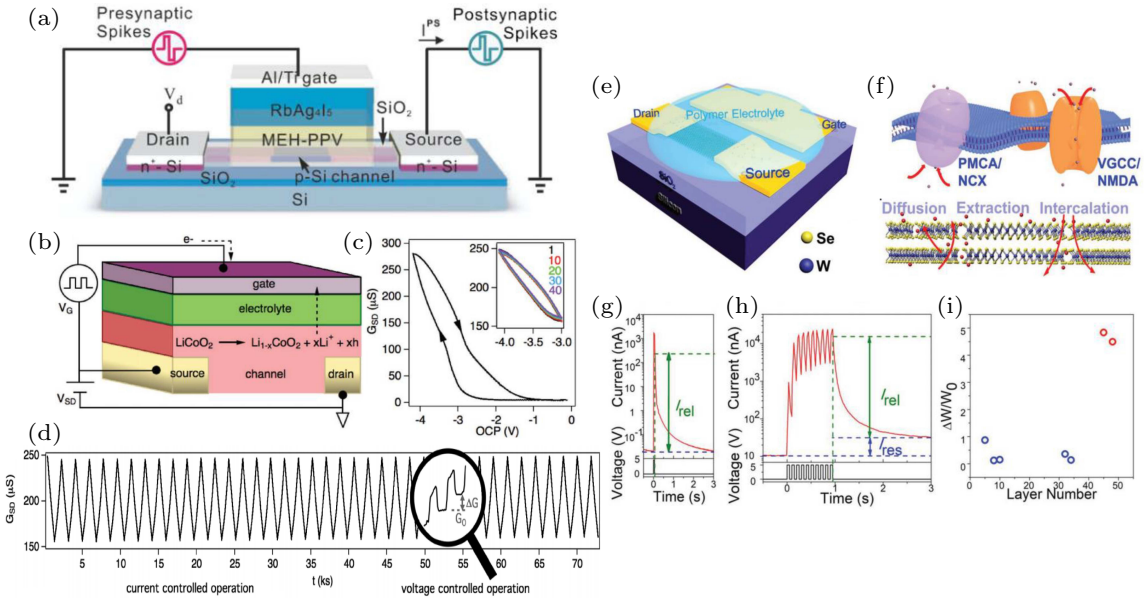


Fig. 5. (a) Schematic of a synaptic transistor with $RbAg_4I_5$ electrolyte. Reprinted with permission from Ref. [84]. Copyright 2010, John Wiley & Sons. (b) Schematic of device with $Li_{1-x}CoO_2$ channel material. (c) G_{SD} as a function of gate voltage. (d) Conductance response $G_{SD}(t)$ during current-controlled cycling. Reprinted with permission from Ref. [73]. Copyright 2017, John Wiley & Sons. (e) Schematic of the ion gated synaptic transistor, with 2D materials as the channel. (f) Similarity of the migration and dynamic balance of ion concentrations between biological systems and present synaptic transistors. (g) EPSC characteristic. (h) Transition from STP to LTP. (i) Dependence of long-term weight changes on the layer number of WSe_2. Reprinted with permission from Ref. [71]. Copyright 2018, John Wiley & Sons.

3.3. O^{2-}-EGTs

Oxygen ions can also be the functional ions in electrolytes of high-performance synaptic transistors. The conductance of some oxides, such as $SmNiO_3$, is very sensitive to the respective oxides' stoichiometric ratio.[74] Stoichiometry can be modulated *in situ* through an ionic liquid electrolyte gate electrode. The transmission and reception of oxygen ions in channel materials are the basis for the implementation of synaptic functions. Recently, $SrFeO_x$ (SFO) and $SrCoO_x$ (SCO) have been shown to be excellent channel materials for oxygen ion synaptic transistors.[75,76,85] They have similar characteristics, so we only discuss SFO, the crystal structure of which exhibits a variety of distinct oxygen-deficient perovskite (PV) structures, with x ranging from 2.5 to 3, depending on its oxygen stoichiometry. The brownmillerite (BM)-$SrFeO_{2.5}$ structure with alternating stacks of FeO_4 tetrahedral and FeO_6 octahedron layers is an insulator, while PV-structure with corner-sharing FeO_6 octahedra exhibits metallic conduction. Furthermore, they can be electrically transformed to each other through electrolyte-gating, as shown in Fig. 6(a). Based on this principle, Ge *et al.* and Huang *et al.* designed and fabricated EGTs based on SFO and SCO channel layers, respectively. The transistor structure and measurement setup are illustrated in Fig. 6(b), while figure 6(c) shows an optical image of a typical device with a droplet of ionic liquid. High-quality epitaxial BM-SFO (SCO) were first grown on (001) $SrTiO_3$ (LSAT) substrates. After standard photolithography and etching, the ionic liquid N, N-diethyl-N-(2-methoxyethyl)-N-methylammoniumbis-(trifluoromethylsulphonyl)-imide (DEME-TFSI), a good conductor of oxygen ions, was deposited on the channel and the gate electrodes as the electrolyte gating medium. When a negative voltage is applied on the gate electrode, the oxygen ions are driven by the electric field and inserted into the BM-SFO channel, evoking phase transformation from the low-conducting BM-SFO to the high-conducting PV-SFO. In contrast, positive gate voltages induce the extraction of oxygen ions from the channel, thus changing the high-conductance

state to a low-conductance state. In such a way, various important synaptic functions such as long-term plasticity, STDP, and non-volatile logic operations were simulated by the devices. Beyond the oxide channel materials, Go *et al.* found that various metals can also be used for the channel layer.[86] They used the device design shown in Fig. 6(d) to evaluate titanium, molybdenum, and tungsten as the channel metals. The results (Fig. 6(e)) showed that the W channel, which formed a relatively less stable oxide, exhibited a much higher on/off ratio (> 10) and linear conductance change.

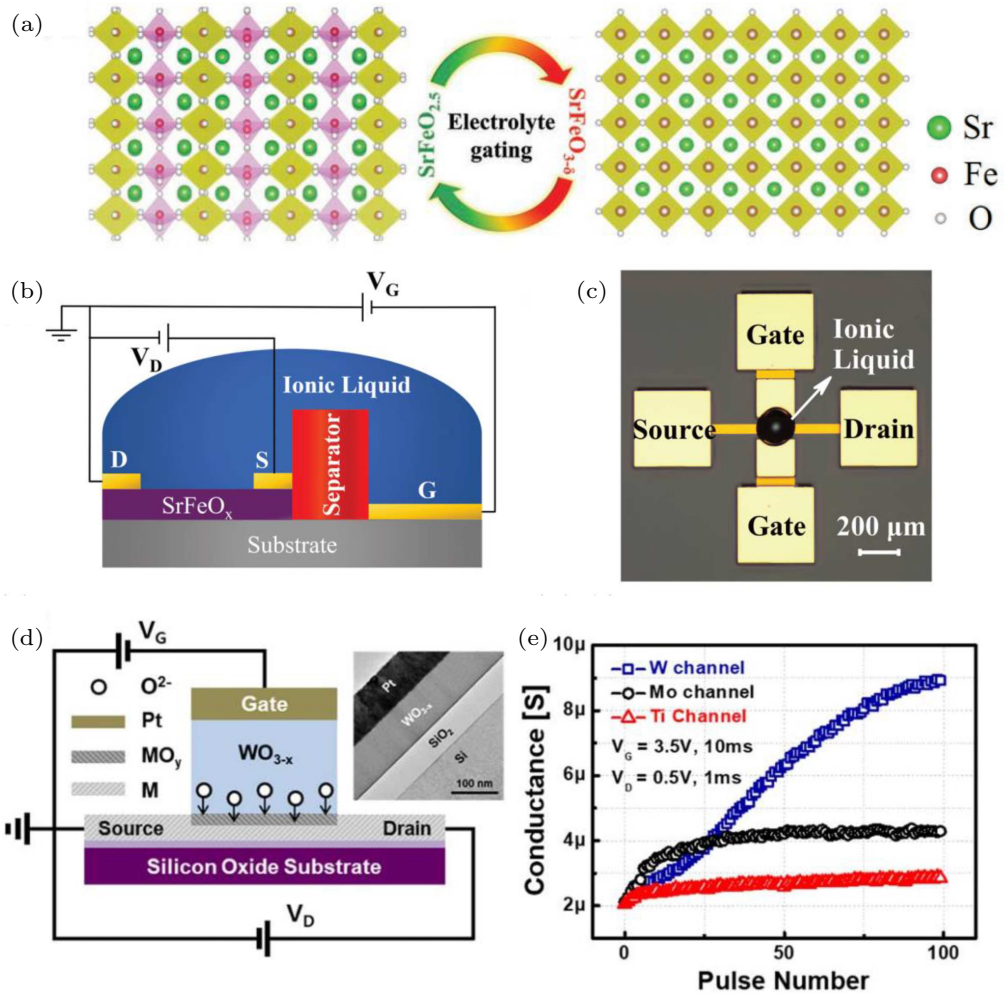


Fig. 6. (a) Crystal structures of BM-$SrFeO_{2.5}$ and PV-$SrFeO_{3-\delta}$ thin films along the {100} direction on the $SrTiO_3$ substrate. (b) Illustration of the transistor structure and measurement setup. (c) An optical image of a typical ferrite transistor device. Reprinted with permission from Ref. [75]. Copyright 2019, John Wiley & Sons. (d) Schematic diagram of the three-terminal synapse device structure, which includes the operating mechanism and measurement setup. Inset shows cross-sectional TEM image of Pt/WO_{3-x}/W/SiO_2/Si stack. (e) Channel conductance change (potentiation) for different channel metals as a function of positive gate pulses (3.5 V, 10 ms). Reprinted with permission from Ref. [86]. Copyright 2019, the Japan Society of Applied Physics.

Although the above mentioned EGTs can mimic various important synaptic functions, such as short-term synaptic plasticity, LTP, LTD, STDP, SRDP, etc., a reliable synaptic device for neuromorphic computing is still missing, as are fundamental analyses on device scalability, endurance, operating speed, and stability of electrolytes. Moreover, a network level demonstration with several such devices is urgently needed. Besides that, the effect of mobile ion type on synaptic transistors' performance is an issue of common interest. H^+, the smallest ion, has the highest mobility and is easy to insert into the interstitial void of materials. Thus, the H^+-EGTs are expected to have fast write speed and low programming energy. Li^+-EGTs are similar to H^+-EGTs, but with larger programming energy and more robust retention. O^{2-}-EGTs with excellent retention property are relatively different from the aforementioned two. The O^{2-}-EGTs are usually slower because the O^{2-} ion is much heavier than H^+ and Li^+.

4. Ferroelectric gated synaptic transistors

Ferroelectric materials have a spontaneous electric polarization that can be reversed by the application of an external electric field. Tremendous efforts have been devoted to ferroelectric devices.[87–90] In a ferroelectric gated field effect transistor (FeFET), the carrier density can be modulated by changing the polarization state of ferroelectric materials using the gate voltage due to the Coulomb interaction between the ferroelectric polarization and the carriers in the channel.[91]

Traditional FeFETs use the two remnant polarization states of ferroelectric materials to realize two digital states of the memory and have been intensively investigated.[89–94] Due to the multi-domain polarization switching capability of ferroelectric materials, FeFETs can also have multi-conductance levels, and can be used to record the synaptic weights of artificial synapses.[44,90,95–99]

4.1. Inorganic FGTs

In 2012, Nishitani *et al.* fabricated an FGT which used $Pb(Zr,Ti)O_3$ (PZT) as the gate insulator and semiconductor ZnO for the channel layer.[38] As shown in Fig. 7(a), a 30 nm-thick ZnO/675 nm-thick PZT/30 nm-thick $SrRuO_3$ (SRO) stacked structure was deposited on a single-crystal $SrTiO_3$ (001) substrate using pulsed laser deposition (PLD). The conductive SRO film acted as the gate electrode and two Pt/Ti pads on ZnO acted as the source & drain electrodes. As can been seen from Fig. 7(b), applying a pulse gate voltage enabled the multi-valued modulation of the non-volatile channel conductance; the variation depended on the height and the duration of the gate pulse voltage. Furthermore, the asymmetric and symmetric STDP functions were also successfully simulated using this device. However, since Pb is hazardous to the environment, PZT cannot be easily adopted, and a lead-free ferroelectric material is urgently needed. In 2011, the ferroelectric properties of HfO_2-based films were fist revealed.[100] When doped with Zr,[101] Y,[102] Al,[103] etc., various HfO_2-based films demonstrate ferroelectric properties. Moreover, HfO_2-based ferroelectric materials have various advantages, such as CMOS compatibility, low process temperature, and process scalability.[104,105] Thus, great efforts have been devoted to FGTs with HfO_2-based materials as gate insulators.[99,106] Most recently, Kim *et al.* reported an artificial synaptic device with an $HfZrO_x$ ferroelectric film and an indium gallium zinc oxide (IGZO) channel layer.[90] As shown in Fig. 7(c), when applying a positive voltage on the gate, the polarization state of the HZO layer begins to switch to the upward direction. As the positive bias pulse amplitude is increased, the polarization of the ferroelectric layer changes from downward to upward. At the same time, the conductance of the IGZO channel gradually increases because of the electrons that accumulate at the interface region with the upward polarization. Conversely, when a negative voltage is applied to the gate, the channel conductance gradually decreases. In this way, the conductance of the device can be modulated by the external electronic field. More to the point, the FGT in this work exhibits good potentiation and depression properties, such as 64 conductance state levels and good linearity (A_p: -0.8028; A_d: -0.6979), and G_{max}/G_{min} ratio > 10 (Fig. 7(d)). By applying the potentiation and depression data of this device to electronic neural networks, the handwritten digit recognition accuracy can reach 91.1%.

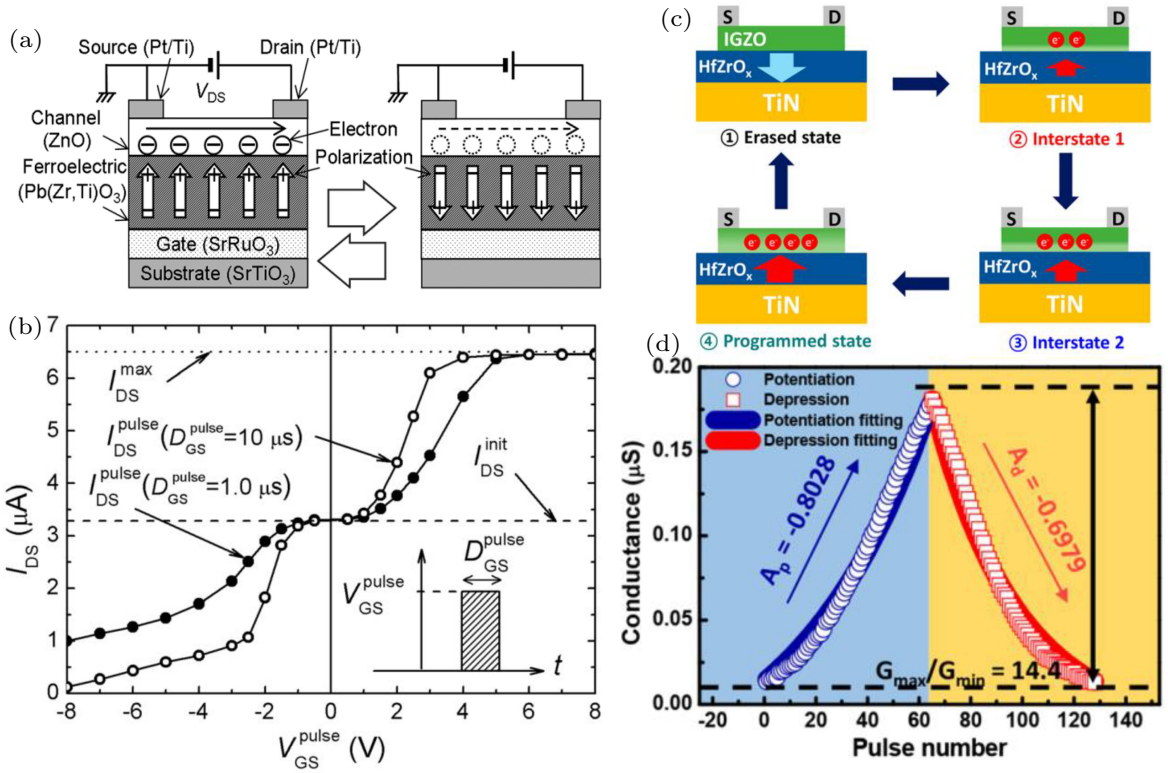


Fig. 7. (a) Schematic of fabricated FGT with upward polarization and downward. (b) Change of the drain current before and after applying the pulsed gate voltage with various heights and widths. Reprinted with permission from Ref. [38]. Copyright 2012, AIP Publishing. (c) Illustration of suggested mechanism of multi-level data storage. (d) Potentiation and depression properties of ferroelectric thin-film transistor with incremental pulse scheme. Reprinted with permission from Ref. [90]. Copyright 2019, American Chemical Society.

4.2. Organic FGTs

Due to the high preparation temperature condition, the fabrication of the above oxide ferroelectric materials is limited to only some substrates. Given this situation, FGTs with organic ferroelectric gated materials, mainly PVDF-TrFE, attracted more attention.[44,95–98] Recently, Jang *et al.* fabricated an ultrathin artificial synapse that featured freestanding ferroelectric organic neuromorphic transistors (FONTs), which does not require a substrate or an encapsulation layer.[44] The device structure is shown in Fig. 8(a). A 20 nm-thick Au layer (gate electrode) was first formed on the substrate using an electron beam evaporator. Then, a PVDF-TrFE ferroelectric film (415 nm thick) was prepared by spin-coating the prepared PVDF-TrFE solution on the Au electrode and annealing at 140 ℃ for 2 h in a nitrogen-filled glovebox. After that, pentacene (30 nm thick) and Au (35 nm thick) were evaporated to create the organic semiconductor channel and source/drain electrodes, respectively, using a shadow mask. Finally, the FONTs were obtained by mechanically peeling them off from the fabricated SiO_2 substrate using a PDMS stamp and subsequently supporting them on a polyethylene terephthalate (PET) film with the central region removed using a punch. In this device, the PSC was studied as a function of the number of pulses with different amplitudes and a fixed width. A larger change in the PSC was observed for both the LTP and LTD when stronger input pulses were applied (Fig. 8(c)) and when the pulse duration was increased (Fig. 8(d)). Moreover, both symmetric and asymmetric forms of STDP were successfully simulated using this device (Fig. 8(e)). In particular, to verify that the FONTs maintain their stable synaptic characteristics even under extreme bending, the researchers transferred the freestanding FONTs onto a brain-shaped PDMS mold and completely folded the freestanding FONTs into a bending radius of 50 μm (Fig. 8(e)). Under both conditions, the FONTs maintained their abilities well and showed LTP and LTD features. Such extraordinary properties make the device suitable for wearable and ultra-flexible materials like bionic skin, brain molds, and collapsible electronic materials. In addition, two-dimensional (2D) semiconductor materials can be used as a channel layer in the FGTs. In 2019, Tian *et al.* successfully designed a synaptic transistor by utilizing PVDF-TrFE and 2D MoS_2, as shown in Fig. 8(g).[95] The conductance of the MoS_2 channel layer can be manipulated precisely, with a highest on/off ratio of $\sim 10^4$. It is worth mentioning that this device showed excellent endurance after 10^7 cycles of stimulation (Fig. 8(h)) with an ultralow energy consumption for each synaptic operation (less than 1 fJ), which highlights its immense potential for neuromorphic computing systems.

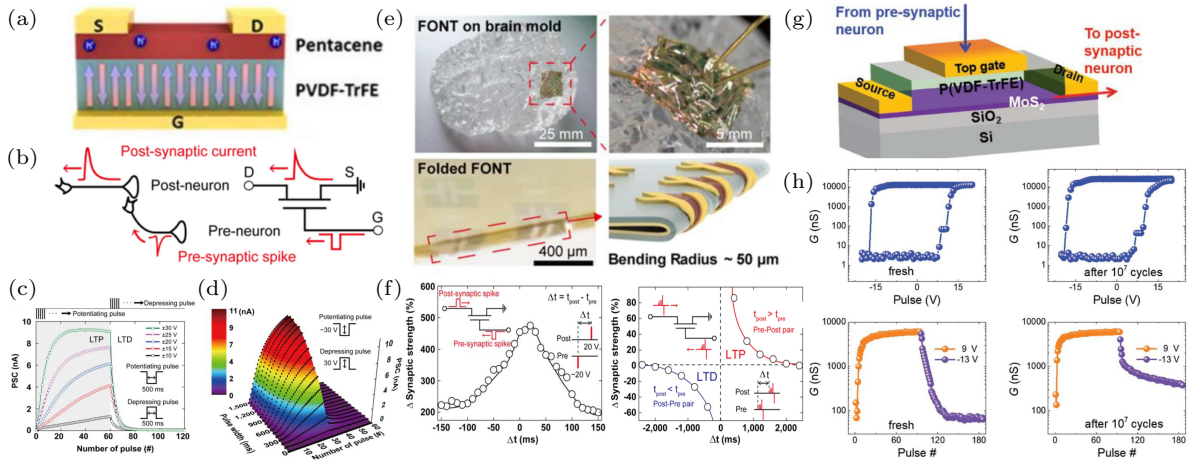


Fig. 8. (a) Structure of a PVDF-TrFE ferroelectric synaptic transistor. (b) Schematic biological synapse (left) and corresponding equivalent circuit of the FONT synapse (right). (c) PSC as a function of the number of pulses with different amplitudes and fixed width. (d) PSC as a function of the pulse width and number of pulses. (e) Images of conformable FONTs on brain-shaped PDMS mold and completely folded FONTs. (f) Implementation of symmetric and asymmetric STDP of the FONT synapse. Reprinted with permission from Ref. [44]. Copyright 2019, American Chemical Society. (g) 3D sketch of the design of an organic ferroelectric transistor synapse with a 2D MoS_2 channel. (h) Channel conductance as a function of gate voltage pulse amplitude. Reprinted with permission from Ref. [95]. Copyright 2019, John Wiley & Sons.

Although FGTs demonstrate some promising features, such as high stability, large on/off ratio, fast programming operations, as well as fewer variations in the weight update curve,[107] they also suffer from the similar scaling problems as DRAM and floating gate memories because in essence they all are charge-based memories.[16] Moreover, it is difficult to simulate short-term synaptic plasticity in these FGTs. Therefore, much effort needs to be put into solving these problems.

5. Advanced functions of synaptic transistors

Recent experiments have made great progress not only on the transistor device level, but also in simulating functionalities of the human nervous system. First, synaptic transistors have been used to construct a tactile perception system.[108,109]

In 2018, Kim *et al.* built a tactile sensing system using flexible organic electronic devices.[110] As shown in Fig. 9(a), the device consists of resistive pressure sensors, organic ring oscillators, and an EGT. Each pressure sensor corresponds to a feeling point. The ring oscillator can be thought of as an artificial nerve fiber, which acts to convert external tactile stimuli into voltage pulses. Multiple electrical signals are then integrated and converted into post-synaptic currents by a synaptic transistor. The synaptic transistor can be subsequently used to interface with biological efferent nerves to form a complete monosynaptic reflex arc. The actuation of the tibial extensor muscle in a detached cockroach leg was demonstrated by connecting this artificial afferent nerve to the leg's biological efferent nerves (Fig. 9(b)). This design can also be used to detect object shape and motion, as well as to distinguish braille characters.

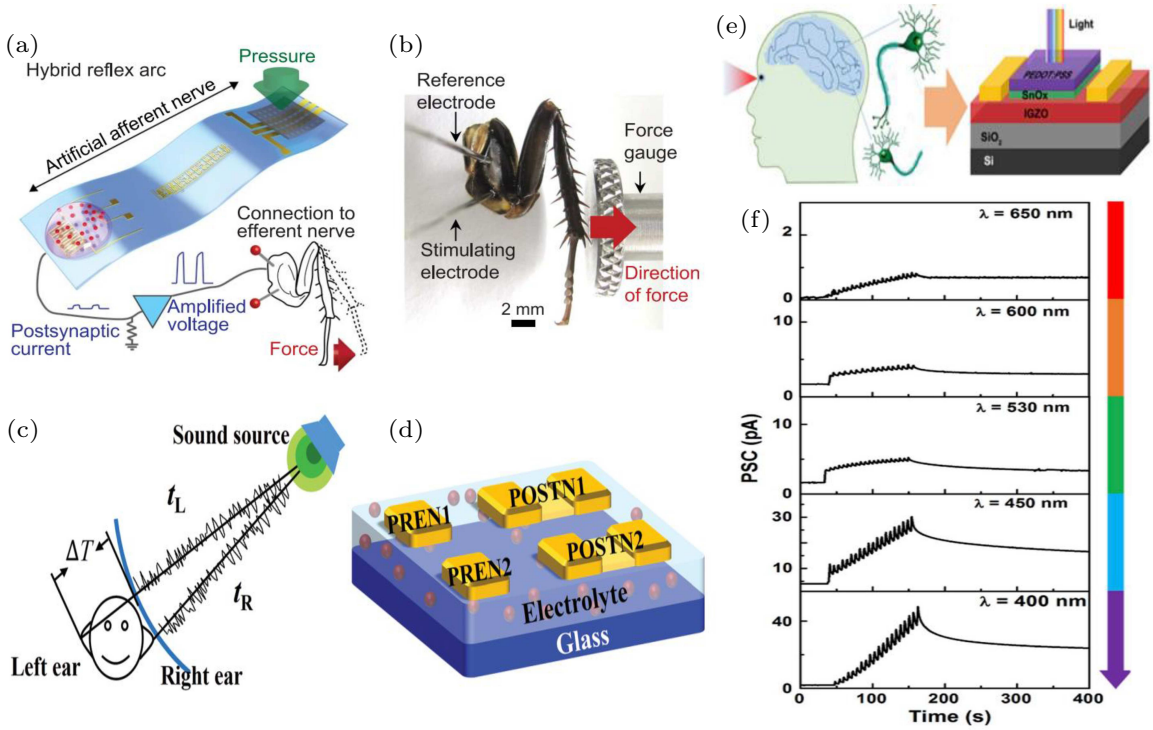


Fig. 9. (a) Hybrid reflex arc made of an artificial afferent nerve and a biological efferent nerve. (b) Photograph of reference and stimulating electrodes, detached cockroach leg, and a force gauge. Reprinted with permission from Ref. [110]. Copyright 2019, American Association for the Advancement of Science. (c) Schematic image of sound location by binaural effect in the human brain. (d) Schematic illustration of sound location in an artificial neural network based on the neuro-transistor. Reprinted with permission from Ref. [111]. Copyright 2019, John Wiley & Sons. (e) Artificial neuromorphic system for eyesight simulation. (f) PSCs triggered by a constant pulse condition at different wavelengths ranging from UV to visible light with a power density of 120 μW/cm^2 (λ = 400–650 nm). Reprinted with permission from Ref. [115]. Copyright 2019, Elsevier.

In addition to simulating tactile senses, synaptic transistors have also been applied successfully in simulating human hearing. Based on capacitively coupled multi-terminal oxide synaptic transistors, He *et al.* constructed a simple artificial neural network to simulate the sound orientation detection of the human brain.[108] The system consists of two gate electrodes and two sets of source/drain terminals, considered as pre-synapses (PREN1 and PREN2) and post-synapses (POSTN1 and POSTN2), respectively (Fig. 9(d)). The two pre-synapses represent the two human ears. In order to simulate the sound location function, an electrical pulse was applied on PREN2 and another pulse with the same amplitude and duration was applied on PREN1 to simulate sound coming from one or the other direction. The interval between the two stimuli represents the interaural time difference due to the different distances between the two ears and the sound source. After that, the ratio of the amplitude of the two post-synaptic currents can be associated in a one-to-one manner with the azimuth angle. In this way, the sound location functionality of our brain can be simulated using such multi-terminal synaptic transistors.

For real-world applications, it is highly desirable to study neuromorphic devices enabled by non-electrical signals (such as photon, pressure, chemical signals) to avoid the problems caused by transduction.[112–114] Recently, Yu *et al.* designed a novel optoelectronic neuromorphic device based on a PN-junction-decorated oxide synaptic transistor and demonstrated ocular simulation.[115] The system consists of four parts: a CMOS photon sensor, a signal processing unit, an electronic memristive synapse (Fig. 9(e)), and an output neuron. As shown in Fig. 9(f), the device can respond to light from red to purple. A monotonic increase was demonstrated as the wave-

length decreased, but non-volatile current remained always present after light stimulation. In addition, typical synaptic behaviors such as short- and long-term plasticities were also successfully simulated using this photo-transistor. Its main modulation mechanism is based on the defects related to the formation and recovery process of metastable oxygen vacancies. This synaptic transistor uses the optical signal directly as a stimulus, simplifying the processing of the image information compared to electrical signals, thus greatly improving the operating speed of the device and reducing the power consumption. This provides an opportunity for photoelectron neural morphology calculation and simulation.

Apart from the above technologies mentioned, many significant achievements have been achieved in artificial sensory systems and neuromorphic computations based on synaptic transistors, such as PH detection,[116] spiking humidity detection,[117] and neuronal arithmetic.[118] These studies laid the foundations for the application of synaptic transistors in neural computing and artificial intelligence.

6. Conclusion and perspectives

In light of the great advantages of high efficiency, low power consumption, and self-learning ability, neuromorphic computing can be the footstone of future artificial intelligence. As the basic unit of a neuromorphic computing hardware, synaptic devices have been studied extensively. For an overview of this field, we summarized synaptic plasticity, learning rules, and recent advances in high-performance synaptic transistors, which are capable of simulating biological synapses. Depending on the different working mechanisms of the dielectric layer, the synaptic transistors are divided into electrolyte-gated and ferroelectric-gated. In the former, electrostatic and electrochemical effects occur at the electric-double-layer, which is formed at the interface of the semiconducting channel layer/electrolyte. Then, the synaptic weight can be modulated via the doping or de-doping of active ions, which can be cations (such as H^+, Li^+, etc.) or anions (such as O^{2-}, S^{2-}, etc.). In FGTs, the channel conductance can be altered depending on the density of electrons induced by the polarization of the ferroelectric film, which can be controlled by applying the gate voltage in a non-volatile manner. Both inorganic and organic ferroelectric layer-based synaptic transistors are reviewed in this article. We hope this article inspires researchers to explore new materials and structure designs to implement better synaptic transistors.

Despite the great advances of synaptic transistors, there are still many challenges to be overcome before further general applications in neuromorphic computing. First, the performance of current synaptic transistors is not good enough. An ideal synaptic transistor should have: 1) small size for integration ($< 1\ \mu m^2$); 2) a large number of states (~ 100); 3) linear and symmetric conductance tuning; 4) low switching noise ($< 0.5\%$ of the weight range); 5) low switching energy consumption (< 1 pJ per switching event); 6) fast write/read speed ($< 1\ \mu s$); 7) long state retention time (10^3–10^8 s) and 7) excellent write endurance ($\sim 10^9$).[15] Yet, none of the reported works satisfy all these requirements. Second, the processing technology of most of the previous works is not compatible with standard micro-electronic technology. Moreover, it is hard to realize the 3D integration of synaptic transistors and their interconnection is also a great challenge. Therefore, the use of synaptic transistors for neuromorphic computing still has a long way to go.

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