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# A method of generating random bits by using electronic bipolar memristor*

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The intrinsic stochasticity of resistance switching process is one of the holdblocks for using memristor as a fundamental element in the next-generation nonvolatile memory. However, such a weakness can be used as an asset for generating the random bits, which is valuable in a hardware security system. In this work, a forming-free electronic bipolar Pt/Ti/$Ta_2O_5$/Pt memristor is successfully fabricated to investigate the merits of generating random bits in such a device. The resistance switching mechanism of the fabricated device is ascribed to the electric field conducted electrons trapping/de-trapping in the deep-energy-level traps produced by the "oxygen grabbing" process. The stochasticity of the electrons trapping/de-trapping governs the random distribution of the set/reset switching voltages of the device, making a single memristor act as a random bit in which the resistance of the device represents information and the applied voltage pulse serves as the triggering signal. The physical implementation of such a random process provides a method of generating the random bits based on memristors in hardware security applications.

**Keywords:** memristor, resistance switching, electrons trapping/de-trapping, random bits

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## 1. Introduction

Memristors,[1,2] or resistive switching devices greatly promise to be vehicles for the next-generation information technologies such as neuromorphic computing,[3–6] novel non-volatile memory,[7–9] and logic-in-memory,[10–14] because of their outstanding performances such as low power consumption,[15] fast switching speed,[16] high endurance,[17] excellent scalability,[18] and CMOS-compatibility.[19] However, the large fluctuations of the switching parameters themselves are always being the major obstacle for these applications.[20] Although the uniformity of the switching parameters of the memristor is constantly improved,[21–24] the intrinsic stochasticity originating from the physical switching process is always the pain spot for the above non-volatile memory-related applications, which somewhat lowers the researcher's expectations for the prospects of this kind of novel electrical device. However, this undesirable and inherent random attribute can be valuable in stochastic computing[25] and hardware security applications[26,27] in the coming era of the Internet of things (IoT), by acting as the physical entropy source of randomness.

Recently, some literature reported that a kind of true random number generator (TRNG) is realized based on the stochasticity of memristor switching processes.[28–32] Some researchers implemented random number generators (RNGs) based on the ionic resistance switching process.[20,33] The randomness of this kind of ionic memristor comes from the formation and dissolution of nanoscaled conducting filaments.[28] However, as is well known, the electronic resistance switching process has less power consumption, better reliability, and a high switching speed compared with the ionic counterpart,[20,34–36] which is of great significance in some applications requiring low power consumption, high stability, and quick response. Furthermore, the electronic resistance switching process was also reported to be adopted to realize RNGs, whose stochasticity is derived from the electrons trapping/de-trapping process.[30,37] By comparision, the RNG based on the electronic resistance switching process is more suitable to meeting the requirements for hardware security in the era of IoT.

Besides, before starting to generate random bits, most of the existing memristor-based RNGs inevitably need an electro-forming process to initialize the memristor.[29,32] The electro-forming process is generally achieved by applying a high voltage to the memristor which could cause the device to be damaged, affecting the reliability of the subsequent op-

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erations. In other words, some memristor-based RNGs that require electroforming may not be able to work well finally.

In this study, a forming-free electronic bipolar memristor based on the structure of Pt/Ti/$Ta_2O_5$/Pt is investigated, serving as a generator of random bits by utilizing its cycle-to-cycle variation. The resistive switching mechanism and stochasticity of the switching parameters of the Pt/Ti/$Ta_2O_5$/Pt-based memristor are carefully discussed. This device exhibits a forming-free characteristic, and the dominant resistive switching mechanism is the electric field-conducted electrons trapping/de-trapping in the deep-energy-level traps. The two characteristics make the designed generator more suitable for high reliability and low power applications.

## 2. Experiment

### 2.1. Fabrication of the Pt/Ti/$Ta_2O_5$/Pt memristor

The $SiO_2$ substrate was sequentially cleaned with acetone, isopropyl alcohol, and deionized (DI) water in an ultrasonic oscillator prior to the deposition. A 10-nm-thick Ti adhesion layer was deposited on a $SiO_2$ substrate chemically cleaned by an e-beam evaporation system with the chamber pressure of $1.5 \times 10^{-4}$ Pa. Then, a 40-nm-thick Pt bottom electrode (BE) was evaporated onto the Ti metal layer by the e-beam evaporation. An 80-nm-thick $Ta_2O_5$ layer was deposited on the BE in the same way by using a 99.995% $Ta_2O_5$ target. In the end, a 40-nm-thick Ti top electrode (TE) layer and a 10-nm-thick Pt protection layer were sequentially deposited on the $Ta_2O_5$ layer by using the e-beam evaporation, in which a copper grid with arrayed opening windows of 200 μm $\times$200 μm was used as a shadow mask.

### 2.2. Characterization

The semiconductor parameter analyzer (Keithley 4200 SCS) combined with a probe station was utilized to measure the *I*–*V* characteristics of the Pt/Ti/$Ta_2O_5$/Pt memristor at room temperature. A bias voltage was applied to the TE, and the BE was grounded during the electrical measurements. The optical microscope (Nikon ECLIPSE LV150NL) in 100$\times$ was used to capture the optical microscopy (OM) image of the device.

## 3. Electric resistive switching of Pt/Ti/$Ta_2O_5$/Pt memristor

Figure 1 exhibits the structure and the resistance switching behavior of the fabricated Pt/Ti/$Ta_2O_5$/Pt memristor. The top view from the optical micrograph is shown in Fig. 1(a). The insert of Fig. 1(a) shows the schematic structure of the device. The active field of the device is defined by the area of the TE, which was formed through the shadow mask in the deposition process. The bottom electrode was exposed by scraping the films after the whole fabrication as shown in Fig. 1(a). Figure 1(b) shows the *I*–*V* curves obtained from the multiple direct current (DC) voltage sweeping tests at room temperature. The voltage was swept in the sequence of 0 V$\rightarrow$ 1.5 V$\rightarrow$ 0 V $\rightarrow$ $-$1.0 V$\rightarrow$ 0 V in steps of 0.02 V. A compliance current of 1 mA was set to protect the device from breakdown during the electrical measurements. The characteristic of bipolar switching was successfully demonstrated with set and reset voltages of $\sim$ 0.75 V and $\sim$ $-$0.7 V respectively. The device shows forming-free property as the set voltage in the first sweep process [the switching from pristine state to the low resistance state (LRS)] nears 0.5 V, which is not much different from the following set voltages. Figures 1(c) and 1(d) show the resistances and switching voltages from the continuous 150 sweeping processes. Although both of them are fluctuant, the margins between the two parameters in each of them still exist. For resistances, the ratios of high resistance and low resistance are between $\sim$ 170 and $\sim$ 5, meaning that a boundary can be chosen to distinguish the two resistance states. For the switching voltages, the cycle-to-cycle variabilities are more obvious, which could be utilized to generate random bits.

To figure out the conduction and resistance switching mechanisms of the fabricated Pt/Ti/$Ta_2O_5$/Pt device, the carrier transport process is investigated by fitting the measured *I*–*V* curves. Figures 2(a) and 2(b) show the *I*–*V* curves of the set and reset processes in a double logarithmic scale, respectively. The slopes of the double logarithmic *I*–*V* curves in both high resistance state (HRS) and LRS show different values, which reflects that the conduction mechanism of LRS and HRS may be the space-charge-limited conduction (SCLC) mechanism.[38] Figure 2(a) shows that when a small positive voltage (0 V to 0.1 V) is applied to the device in HRS, few electrons are injected from the BE. On this occasion, most of the electrons are trapped in the trap position and jump to the adjacent position. The jump conduction mechanism in the small voltage region exhibits linear *I*–*V* characteristics.[38] Thus, ohmic conduction is observed as the slope in this region is $\sim$ 1. With the increase of the applied positive voltage, the *I*–*V* curve deviates from linear behavior due to the larger current injection as the slope of this region is $\sim$ 2. When the voltage increases further, the number of injected electrons increases, which causes more trap sites to be filled. Once the voltage reaches the threshold voltage [$V_{set}$, which is about 0.8 V as indicated in Fig. 2(a)], all the traps can be filled with electrons and substantial electrons hop into the conduction band, resulting in a surge in the free-carrier concentration in the device and a jump in the current, which is the so-called HRS-to-LRS switching. The de-trapping process is not an easy task due to the heavy depth of the trap level and the asymmetric energy barrier.[37] The device remains in LRS as long as the absolute value of the applied voltage is smaller than that of the abso-

lute value of the reset threshold voltage $V_{reset}$, which is about −0.6 V as can be seen in Fig. 2(b). It means that the traps are still filled with electrons under the positive (as shown by curve B) and negative (as shown by curve C) bias. Once the negative bias reaches $V_{reset}$, the trapped electrons begin to abscond to the bottom electrode, and consequently, the device switches back to HRS (as shown by curve D). Based on the analysis above, the switching behavior of the fabricated bipolar memristor can be concluded as the consequence of electron traps filling and emptying processes.[37]

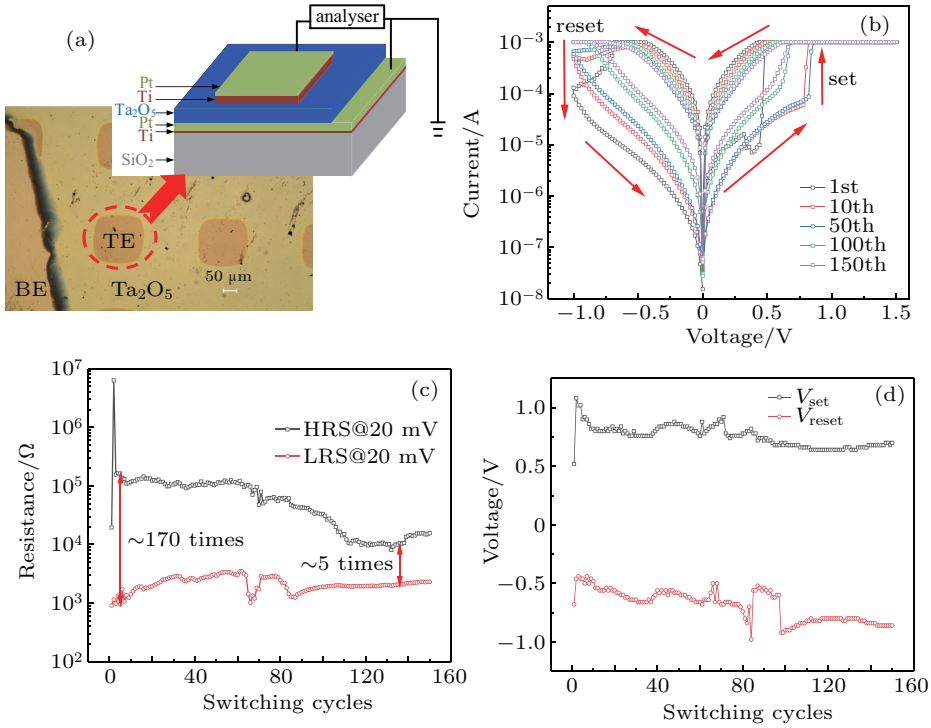



**Fig. 1.** (a) Optical microscopic image from top view of Pt/Ti/$Ta_2O_5$/Pt memristor with inset schematically indicating its structure; (b) *I*–*V* curves of Pt/Ti/$Ta_2O_5$/Pt memristor under voltage sweeping mode at 300 K; (c) resistance in HRS and LRS under the 20-mV read voltage at 300 K, and (d) switching voltages under 150-voltage sweepings.

Electron traps play a crucial role in the conduction and switching process of the electronic bipolar memristor. In the fabrication, the Pt layer was deposited to protect the Ti TE from being oxidized by oxygen in the air. Therefore, the Ti TE would grab the oxygen atoms from the $Ta_2O_5$ layer spontaneously and exclusively. As a result, the $TiO_{2-x}$ film with numerous oxygen vacancy defects holding deep energy levels (from ∼ 0.8 eV to ∼ 1 eV)[39–41] in the bandgap was formed in the Ti/$Ta_2O_5$ interface to act as the switching zone. This process could be called the "oxygen grabbing" process. Certainly, this process would also generate the same defects in the $Ta_2O_5$ layer, but these defects have little influence on the resistive switching behavior of the memristor because of their shallower energy levels (from ∼ 0.25 eV to ∼ 0.57 eV).[42] Figure 2(c) shows the imaginary schematic diagram of the initial physical state of the device, in which the "oxygen grabbing" process has not occurred. Figure 2(d) shows the real physical state of the device (after the "oxygen grabbing" process). According to previous reports, in $Ta_2O_5$, oxygen vacancy defects are more likely to form the conducting filament,[23,43] while they are prone to introduce the useful deep energy-level electronic traps into the $TiO_{2-x}$ film.[37] More importantly, as the film thickness values of the two film layers are different (Ti layer is 40-nm thick and $Ta_2O_5$ layer is 80-nm thick), the concentration of oxygen vacancy defects in titanium oxide is much higher than that in the tantalum oxide after the "oxygen grabbing" process. Therefore, the deep energy-level defects in the $TiO_{2-x}$ zone, originating from the spontaneous "oxygen grabbing" process, play a major role in the resistive switching process. Meanwhile, the defects in the $Ta_2O_{5-x}$ film constructed the conducting filament, which could be regarded as a virtual electrode that forms an ohmic contact with the BE.[37] Figures 2(e) and 2(f) exhibit energy band diagrams of the $TiO_{2-x}$ zone with plenty of the deep energy-level electronic traps in HRS and LRS respectively. When the electron traps in the $TiO_{2-x}$ zone are emptied, they capture the injected electrons and the device presents HRS. Once they are filled under high enough positive voltage ($V_{set}$), the device would be switched from the HRS to the LRS. On the contrary, when the applied voltage is higher than the reset voltage ($V_{reset}$), the electron traps would release the trapped electrons, making the device switched back to the HRS. It is worth noting that each electron trap captures/releases electrons randomly in the electron trapping/de-trapping process. This governs the randomness of switching voltages.

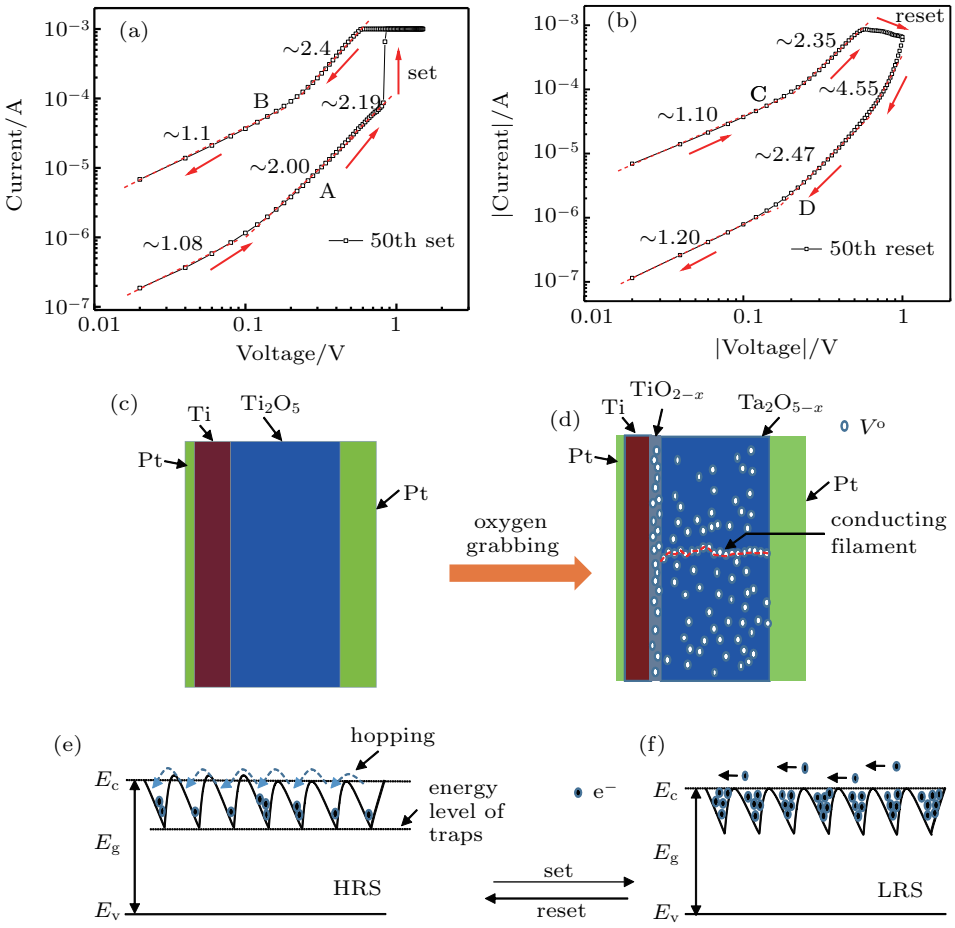



**Fig. 2.** The *I*–*V* characteristic curve of the memristor in double logarithmic scale for (a) set process of HRS and (b) reset process of LRS; schematic diagrams of device in (c) initial state and (d) stable state; energy band diagram of $TiO_{2-x}$ film when device is in (e) HRS and (f) LRS.

## 4. The generation of random bits by using Pt/Ti/$Ta_2O_5$/Pt memristor

The electron trapping/de-trapping procedure manifests stochasticity and could result in the variation of the switching parameters physically,[30] such as the resistances and the set/reset voltages which could be utilized to generate random bits. Figures 3(a) and 3(b) provide the cumulative probabilities of the two resistances and the two switching voltages. It can be found that the two resistance states do not interfere with each other even though the resistance of HRS shows a wider range ($\sim 8\times10^3$ Ω to $\sim 6\times10^6$ Ω) than that of LRS ($\sim 9\times10^2$ Ω to $\sim 3.5\times10^3$ Ω). Similarly, both the $V_{set}$ and the $V_{reset}$ present fluctuations and the range of $V_{set}$ ($\sim 0.5$ V to $\sim 1$ V) is narrower than that of $V_{reset}$ ($\sim -1$ V to $\sim -0.45$ V). The stochasticity in the switching voltage could act as the source of the random bits through utilizing the two fixed voltages of $V_{p1}$ and $V_{p2}$ (0.76 V and −0.66 V), which are the median values in the distribution of $V_{set}$ and $V_{reset}$. The larger variations in the resistance of HRS and $V_{reset}$ could be attributed to the electron de-trapping process with greater stochasticity. The more electrons are de-trapped during the reset switching, the higher the resistance of HRS, and the larger the set voltage required to fill up the electron traps for the set switching, as depicted in Fig. 3(c).

A scheme to generate random bits based on the fabricated device is carried out experimentally. Figure 3(d) indicates the flowchart of the method to generate random bits by using a memristor. Two random bits are produced in each operation cycle. The required operation voltages are shown in Fig. 3(e) and all of them have the same pulse width. The random bits are generated as the following steps. The original memristor is in HRS. When this memristor is exposed to a positive voltage pulse $V_{p1}$ (step i), the probability of the device switching into LRS (the present $V_{set} < V_{p1}$) or remaining in HRS (the present $V_{set} > V_{p1}$) is 50% due to the stochasticity of the set process. This unpredictable resistance could be regarded as the first random bit whose value can be known by applying a small read voltage pulse $V_{read}$ (20 mV) to the device (step ii). If this random bit is "1", which means that the device has been switched to LRS, we can go to step iv directly to generate the second random bit by applying a negative voltage pulse $V_{p2}$ (step iv) based on the randomness of the reset process and the small read voltage pulse of $V_{read}$ is also used to confirm the result (step v). However, if the result from step ii is "0", which means that the memristor remains in HRS, firstly, the

device should be applied with a sufficiently large set voltage pulse $V_{set}$ (for example $\sim$ 1.5 V in this study) to become in LRS (step iii). Then, the same procedures as those of step iv and step v are used to generate the second random bit. Certainly, the result from step v may be "0",which means that the inequality $|V_{reset}| < |V_{p2}|$ holds true and the device has been switched into HRS by $V_{p2}$, or "1", which means that the inequality $|V_{reset}| > |V_{p2}|$ holds true and the device remains in LRS, corresponding to different operations for beginning the next cycle. If the result from step v is "0", a new operation cycle could be triggered to generate new random bits. However, if the result from step v is "1", firstly, a negative reset voltage pulse $V_{reset}$ with a large absolute value ($\sim -1.5$ V in this work) should be applied to the device to switch it into HRS, then starting the next cycle (step vi). In this work, 10 operation cycles were completed, producing 20 random bits, which are shown in Fig. 3(f). Based on a similar variability of the resistance switching process to produce random bits, the TRNG in Ref. [32] generates only one random bit with four voltage pulses, while the method proposed in this paper requires up to six voltage pulses to yield two random bits. Besides, when the device is in LRS, the applied set voltage in Ref. [32] would result in big power consumption inevitably, while this problem is avoided by applying a comparison operation here.

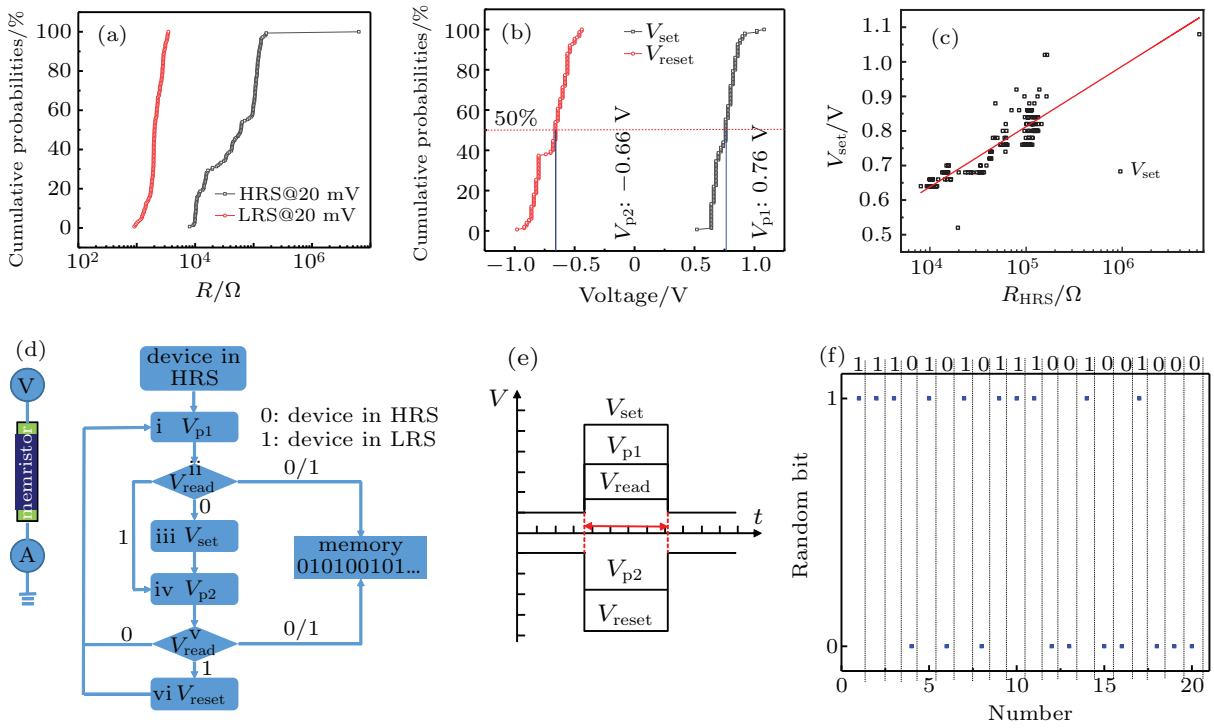



**Fig. 3.** (a) Plots of resistance cumulative probability *versus* resistance of HRS and LRS under 20-mV read voltage at 300 K; (b) plots of voltage cumulative probability *versus* values of $V_{set}$ and $V_{reset}$ at 300 K; (c) spread of $V_{set}$ varying with the resistance of HRS; (d) flowchart of generating random bits by using fabricated memristor; (e) the required operation voltages (the widths of the voltage pulses are the same); (f) random bit-streams obtained in 10-voltage operation cycles.

## 5. Conclusions

An electronic bipolar Pt/Ti/$Ta_2O_5$/Pt memristor is successfully fabricated to achieve a generator of random bits in this work. The resistance switching characteristics of the device are studied, which are attributed to the electrons trapping/de-trapping process in the deep-energy-level traps introduced by the spontaneous "oxygen grabbing" process. The stochasticity in the set/reset process of the device is analyzed. A scheme of utilizing two fixed operation voltages to trigger the random set or reset process is proposed to generate two random bits efficiently through using a single forming-free and electronic type memristor, which provides a simple way to generate random bits in low-power-consumption hardware security applications.

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