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Improvement of memory characteristics by employing a charge trapping layer with combining bent and flat energy bands*

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Designed $Zr_xSi_{1-x}O_2$ films with combining bent and flat energy bands are employed as a charge trapping layer for memory capacitors. Compared to a single bent energy band, the bandgap structure with combining bent and flat energy bands exhibits larger memory window, faster program/erase speed, lower charge loss even at 200 °C for 10^4 s, and wider temperature insensitive regions. The tunneling thickness together with electron recaptured efficiency in the trapping layer, and the balance of two competing electron loss mechanisms in the bent and flat energy band regions collectively contribute to the improved memory characteristics. Therefore, the proposed $Zr_xSi_{1-x}O_2$ with combining bent and flat energy bands should be a promising candidate for future nonvolatile memory applications, taking into consideration of the trade-off between the operation speed and retention characteristics.

Keywords: nonvolatile memory, bent and flat energy bands, charge trapping, memory capacitor

PACS: 77.55.df, 81.15.Gh, 73.40.Qv **DOI:** 10.1088/1674-1056/ab7224

1. Introduction

Recently, nonvolatile memories have been studied widely in order to satisfy the growing requirement for data storage.[1–4] As a competitive candidate for next-generation nonvolatile memories, the polysilicon/SiO_2/Si_3N_4/SiO_2/Si (SONOS) charge trapping memories have drawn much interest due to their better scalability, enhanced endurance and lower operating voltage.[5–7] However, an excessively reducing tunneling layer (TL) to obtain faster operation speed will increase the leakage current, resulting in significant charge loss,[8] and the trade-off between program/erase speed and data retention characteristics restricts the progress of conventional SONOS.[9,10] Many researches have been carried out to surmount the urgent problem, and the focus is mainly on the substitution of the Si_3N_4 charge trapping layer (CTL). In addition to the metals[11–15] or oxide nanocrystallites[16–19] as storage media, the high-k films with flat energy band (F-B) as the CTL, such as HfO_2, ZrO_2, Nd_2O_3, ZrSiO, HfAlO and TiAlO, were proved to be a promising solution for improving the charge trapping properties on account of their lower power and higher charge trapping ability.[20–29] Moreover, compared to F-B, the $Zr_xSi_{1-x}O_2$ CTL with bent energy band (B-B) induced by varying composition distribution shows enhanced memory characteristics.[30] On the one hand, the B-B decreases the electron tunneling thickness from the substrate to the conduction band of the CTL, increasing the program speed. On the other hand, the B-B simultaneously increases the electron tunneling thickness from the CTL conduction band to the blocking layer (BL), further improving operation speed as well as the data retention characteristics. Inspired by the previous results, we propose a kind of memory structure, in which the designed $Zr_xSi_{1-x}O_2$ film including nine $[(ZrO_2)_m(SiO_2)_n(ZrO_2)_m(SiO_2)_n]$ units is used as the CTL. A complex bandgap combining B-B and F-B is formed by regulating the m and n values in each unit. The effect of the complex bandgap on memory characteristics is systematically investigated, with the purpose of exploring effective energy band structure of the CTL and improving memory performance for prospective charge trapping memory applications.

2. Experiment

The atomic layer deposition technique was used to deposit the films. The $ZrCl_4$ and $SiH[N(CH_3)_2]_3$ precursors were adopted to synthesize ZrO_2 and SiO_2, respectively, and the O_3 served as the oxygen source. Prior to fabrication, the p-type Si substrates were cleaned by the Standard Radio Corporation of America. After that, 30 SiO_2 deposition cycles was deposited as the TL at a substrate temperature of 300 °C. Next, a $Zr_xSi_{1-x}O_2$ CTL including nine $[(ZrO_2)_m(SiO_2)_n(ZrO_2)_m(SiO_2)_n]$ units was deposited in sequence, in which the m and n are the numbers of atomic layer deposition cycles. In the first unit, the m/n is 1/5, i.e., 1 ZrO_2 deposition cycle, 5 SiO_2 deposition cycles. The 1 ZrO_2 deposition cycle and 5 SiO_2 deposition cycles were orderly deposited. From the second unit to the ninth unit, the m/n values were 2/4, 3/3, 4/2, 5/1, 4/2, 3/3, 2/4, and 1/5, respectively. Subsequently, 120 SiO_2 deposition cycles was deposited as the BL. Then, the rapid thermal annealed process was performed at 700 °C for 60 s in N_2 ambience, and the fabricated mem-

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ory capacitor was labeled as S1. For comparison, three memory capacitors were also fabricated and named as S2, S3 and S4, respectively, in which the $Zr_xSi_{1-x}O_2$ CTLs were designed by controlling the m/n in each unit, and the detailed parameters were listed in Table 1. The thicknesses of TL, CTL and BL are about 3 nm, 11 nm and 12 nm for S1, S2, S3, and S4, respectively, as shown by the transmission electron microscope (TEM) images in Fig. 1. The composition distribution in the CTL was detected by x-ray photoelectron spectroscopy (XPS). The capacitance-voltage curves, program/erase speed, and data retention were measured by a Keithely 4200 semiconductor characterization system.

Table 1. The detailed parameters for memory capacitors.

	TL	The m/n value in $Zr_xSi_{1-x}O_2$ CTL (nine $[(ZrO_2)_m(SiO_2)_n(ZrO_2)_m(SiO_2)_n]$ units)									BL
		unit 1	unit 2	unit 3	unit 4	unit 5	unit 6	unit 7	unit 8	unit 9	
S1	SiO_2	1/5	2/4	3/3	4/2	5/1	4/2	3/3	2/4	1/5	SiO_2
S2	SiO_2	1/5	2/4	3/3	4/2	5/1	3/3	2/4	1/5	1/5	SiO_2
S3	SiO_2	1/5	2/4	3/3	4/2	5/1	2/4	1/5	1/5	1/5	SiO_2
S4	SiO_2	1/5	2/4	3/3	4/2	5/1	1/5	1/5	1/5	1/5	SiO_2

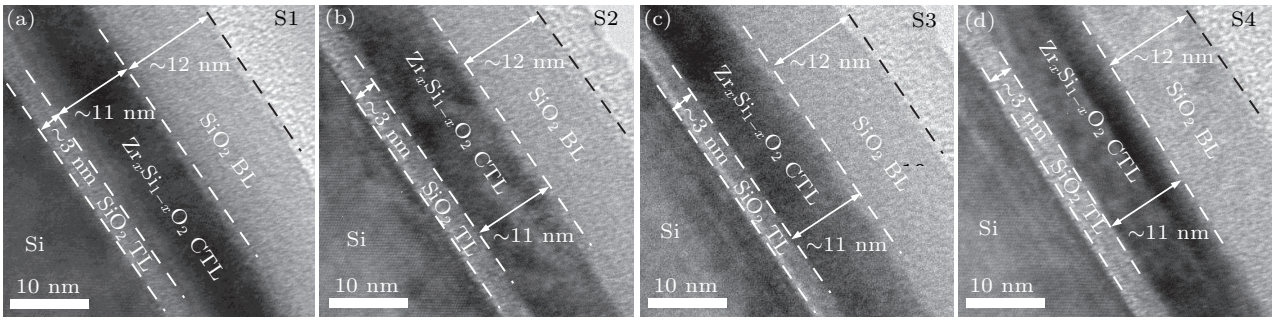


Fig. 1. Cross-sectional TEM images of the memory capacitors (a) S1, (b) S2, (c) S3, and (d) S4.

3. Results and discussion

Figure 2 displays the 1 MHz capacitance-voltage curves under different gate sweeping voltages for memory capacitors. The flat band voltage (V_{FB}) is determined by extracting half of the normalized capacitance,[31] and the difference of V_{FB} shifts between forward and backward in a sweeping range is defined as memory window (ΔV_{FB}).[30] The ΔV_{FB} are negligible in ±2 V sweeping range, indicating that the memory capacitors without memory behavior are in the fresh state, and the corresponding flat band voltages (V_{i-FB}) are −0.3 V, −0.4 V,

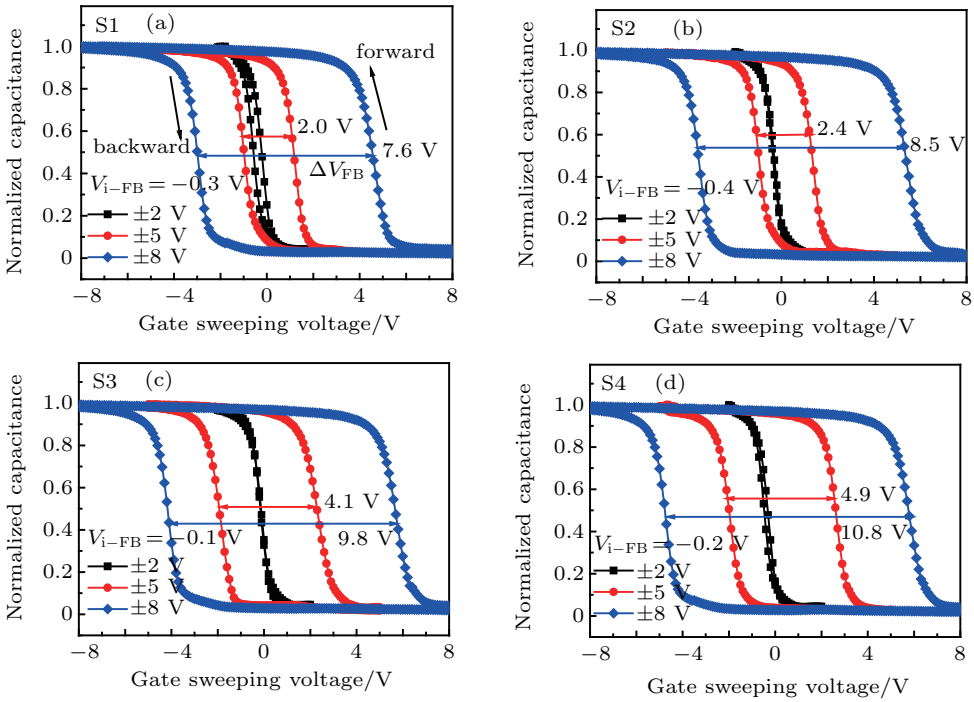


Fig. 2. Normalized high frequency capacitance-voltage curves under different gate sweeping voltages for the memory capacitors (a) S1, (b) S2, (c) S3 and (d) S4. The voltage sweep from positive to negative (forward), and then back to positive (backward).

−0.1 V and −0.2 V for S1, S2, S3, and S4, respectively. For ±5 V/± 8 V sweeping voltages, the ΔV_{FB} values are 2.0 V/7.6 V, 2.4 V/ 8.5 V, 4.1 V/9.8 V, and 4.9 V/10.8 V for S1, S2, S3, and S4, respectively, suggesting the better memory behavior.

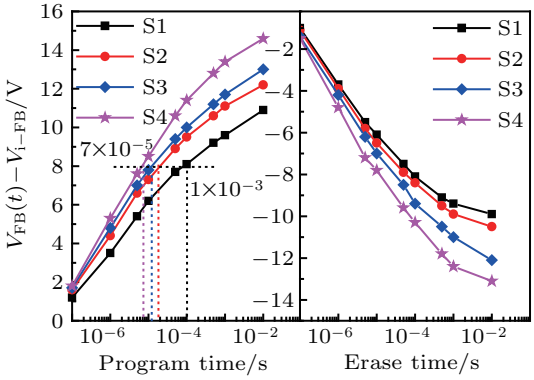


Fig. 3. Program and erase speed of the memory capacitors, in which the $V_{FB}(t)$ is the flat band voltage shift after operating with time t, and the program and erase voltages are fixed at ±10 V, respectively.

Figure 3 gives the V_{FB} shifts relative to fresh state ($V_{FB}(t) - V_{i-FB}$) as a function of program/erase time. The $V_{FB}(t) - V_{i-FB}$ increases gradually from S1 to S4 at the same program or erase time. Taking, e.g., $V_{FB}(t) - V_{i-FB} = +8$ V, the program times for S1, S2, S3, and S4 are about 1×10^{-3} s, 1.8×10^{-4} s, 1.2×10^{-4} s, and 7.5×10^{-5} s, respectively. The program times of S2, S3, and S4 are about one or two orders of magnitude smaller than S1, demonstrating their faster program speed.

Figure 4 shows the data retention characteristics of memory capacitors at different temperatures up to 10^4 s. The memory capacitors were firstly programmed to the same V_{FB} shift (+8 V), and the equation, charge loss $= (8 - V_{FB}^t)/8$[32] was used to calculate the charge losses, where V_{FB}^t is the remained V_{FB} shift after retention time t. Although the charge loss is aggravated with the increase of temperature, the influence degree exhibits obvious difference for the memory capacitors. As the temperature is increased from 20 °C to 200 °C, the charge losses increase from 0.7% to 7.1%, from 0.9% to 4.6%, from 1.0% to 6.0% and from 1.3% to 9.7% for S1, S2, S3, and S4, respectively, and the increase amplitudes of S2 and S3 are smaller than that of others, suggesting their better retention characteristics.

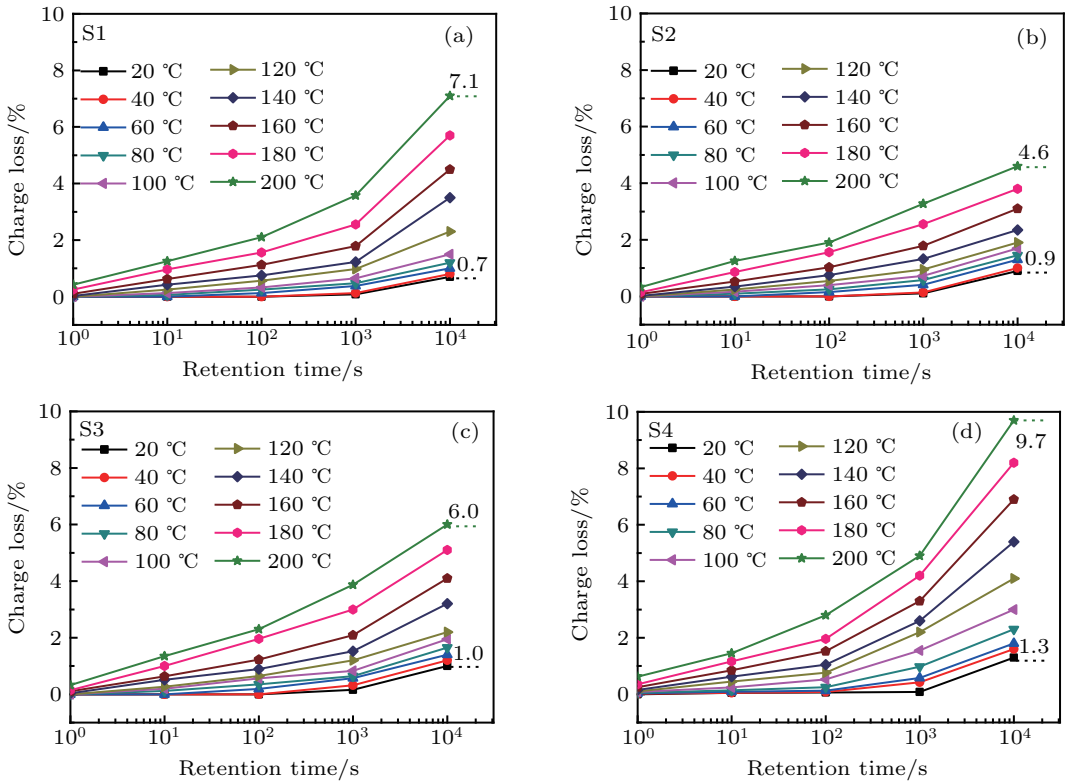


Fig. 4. Charge loss as a function of retention time at different temperatures to observe the retention characteristics for the memory capacitors (a) S1, (b) S2, (c) S3, and (d) S4.

Figure 5 is the correlation between charge loss after 10^4 s and temperatures for the memory capacitors. The relationship between temperature and charge loss can be divided into temperature insensitive and sensitive regions as separated by dotted lines. It is interesting that the turning temperatures between insensitive and sensitive regions are different, which can be determined as 105 °C, 133 °C, 120 °C, and 93 °C for S1, S2, S3, and S4 by the intersection of respective charge loss fitted lines, respectively.[30] In insensitive region, the effect of temperature is slight, and the charge losses orderly increase from S1 to S4 at same temperature. Nevertheless, the charge losses increase sharply with raising temperature in sensitive

region, and the S2 and S3 exhibit smaller charge loss than S1 and S4. The wider temperature insensitive region is beneficial for memory capacitors in view of practical application.[33] Obviously, the S4 is not an applicable memory structure due to its fastest program/erase speed at the expense of retention characteristics. From the viewpoint of the trade-off between the ΔV_{FB}, program/erase speed and data retention, the S2 and S3 should be feasible memory structures compared to S1, because of their faster program/speed, wider insensitive regions and relatively smaller charge loss.

In order to clearly illuminating the variation of memory characteristics, the composition distribution in the $Zr_xSi_{1-x}O_2$ CTL, i.e., atomic percent (at%) of Zr and Si were detected by XPS, as shown in and Figs. 6(a) and 6(b). The Zr at% (Si at%) increases (decreases) firstly and then decreases (increases), showing almost symmetrical trend around CTL center position for S1. Nevertheless, the S2, S3 and S4 present approximately constant regions of Zr at% and Si at% near the BL, and that the regions gradually expand from S2 to S4. Actually, the results are strongly associated with the varying m and n in $[(ZrO_2)_m(SiO_2)_n(ZrO_2)_m(SiO_2)_n]$ units of the CTL, as listed in Table 1. The uniform $[(ZrO_2)_1(SiO_2)_5(ZrO_2)_1(SiO_2)_5]$ units give rise to the constant regions for S2, S3 and S4.

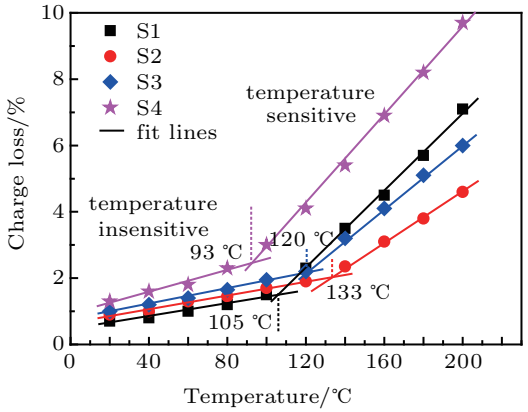


Fig. 5. Correlation between charge loss after 10^4 s and temperatures for the memory capacitors.

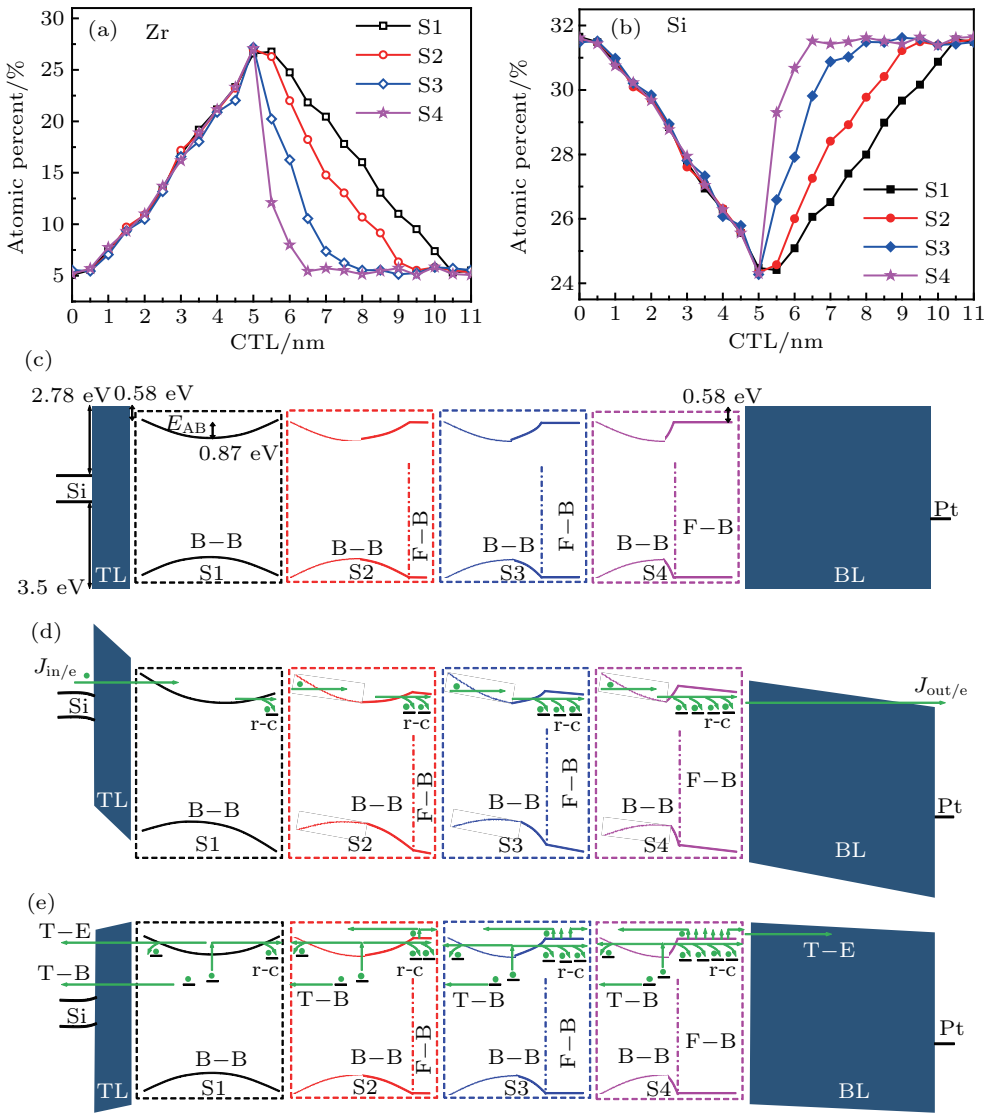


Fig. 6. (a) Zr and (b) Si composition distribution in the $Zr_xSi_{1-x}O_2$ CTL for memory capacitors. Schematic energy band diagrams of memory capacitors in (c) fresh state, (d) program state, and (e) retention state, in which the symbol − and · represent the traps and electrons in the CTL, respectively.

As is well known, the $Zr_xSi_{1-x}O_2$ bandgap depends on the composition distribution, and increasing Zr at% or decreasing Si at% can reduce the bandgap[34] and further modulate the energy band diagrams of memory capacitors.[26] It is reasonable that the variation of memory characteristics should be ascribed to the different energy band structures derived from composition distribution for memory capacitors. According to the previous results,[30] the energy band diagrams in fresh state are depicted for memory capacitors, as shown in Fig. 6(c). Increasing (decreasing) first then decreasing (increasing) of Zr at% (Si at%) will induce a single B-B with a potential well structure for S1. With regard to S2, S3 and S4, the constant regions of Zr at% and Si at% generate partial F-B and form a complex bandgap structure of combining B-B and F-B, and that the F-B regions gradually expand from S2 to S4. The F-B only faces a 0.58 eV potential barrier, while the B-B also introduces ever-changing additional potential barrier (E_{AB}).[30]

Figure 6(d) shows the schematic energy band diagrams of memory capacitors in the program state. The difference between injected electron from Si to the CTL ($J_{in/e}$) and the out-tunneling electron across the BL ($J_{out/e}$)[9] dominates the program speed, and the smaller $J_{out/e}$ can improve the program speed.[33] The electrons in $J_{in/e}$ have to pass through the partial CTL and BL due to the B-B bandgap, then forming $J_{out/e}$. The existing of F-B regions increases the electron tunneling thickness in the CTL and decrease the $J_{out/e}$. The electron tunneling thickness in the CTL gradually enlarges from S1 to S4, and the $J_{out/e}$ is effectively suppressed, especially for the S4 with the longest tunneling thickness in the CTL. Moreover, the electrons in $J_{in/e}$ can be re-captured (r-c) by the traps of CTL in the tunneling process, as indicated by curved lines, further inhibiting the $J_{out/e}$. The wider F-B is helpful for the r-c phenomenon, so the program speed becomes faster and faster from S1 to S4, as shown in Fig. 3.

The energy band diagrams in the retention state are depicted, as shown in Fig. 6(e). At lower temperatures, the stored electrons tunneling from the CTL traps to the substrate conduction band (T-B) plays an important role in charge loss process for memory capacitors,[35] and the time constant of tunneling increases exponentially with the increasing potential barrier.[36] For the trapped electrons in S1 with a single B-B bandgap, the potential barriers include 0.58 eV and E_{AB} throughout entire CTL, leading to better retention characteristics. Nevertheless, the increasing B-B is replaced by the F-B bandgap from S2 to S4, and E_{AB} is superseded correspondingly by 0.58 eV, decreasing the potential barriers as well as time constant. The above reason results in the successive worsening of retention characteristics at respective temperature insensitive region from S1 to S4, as shown in Fig. 3(b). With temperature increasing, the charge loss path gradually converts to thermal excitation (T-E), in which the trapped electrons exit to the CTL conduction band, then tunnel to the Si and BL.[37] Clearly, the B-B and F-B regions have different electron loss mechanisms. In B-B regions, a lots of excited electrons have to tunnel across the F-B regions, which increase the electron tunneling thickness in the CTL and strengthen the r-c efficiency, and a number of electrons across the BL is effectively hindered, improving the temperature insensitive region as well as retention characteristics. However, in F-B regions, the excited electrons without the r-c process only face a thinner thickness of the TL or the BL, and the electron loss process becomes easy, reducing the temperature insensitive region and retention characteristics. With the expanding of F-B regions from S1 to S4, the two loss mechanisms in B-B and F-B regions compete with each other, and collectively affect the retention characteristics. Hence, the wider temperature insensitive regions and lower charge loss for S2 and S3 should be attributed to the balance of the two competing loss mechanisms at elevated temperatures.

In order to evaluate the reliability of memory capacitors, the endurance characteristics are measured as shown in Fig. 7. The program (solid symbols)/erase (open symbols) conditions are +10 V for 1 ms and −10 V for 1 ms, respectively. The degradation of the memory windows after 10^5 program/erase cycles for S1, S2, S3, and S4 were about 11.4%, 9.8%, 10.8%, and 19.6%, respectively. The widest F-B region of S4 increases the r-c process and the deep-levels electrons,[6] which cannot be easily removed during the erase operation,[38] leading to the serious degradation of memory window. Compared to S1, the good endurance of S2 and S3 could be attributed to the accessible trapping levels and suitable energy-level distribution[6] in the complex bandgap structure combined B-B and F-B.

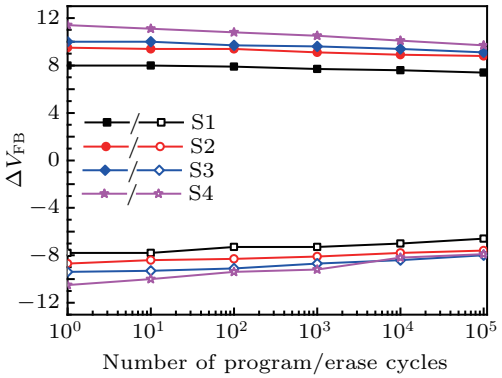


Fig. 7. Endurance characteristics of memory capacitors.

4. Conclusions

In summary, the $Zr_xSi_{1-x}O_2$ films including nine $[(ZrO_2)_m(SiO_2)_n(ZrO_2)_m(SiO_2)_n]$ units have been employed as a CTL for memory capacitors, and the bandgap structures with combining B-B and F-B are formed by regulating the m

and n in each unit. Compared to the S1 with a single B-B, the S2 and S3 with combining B-B and F-B exhibit better memory characteristics, such as the larger $\Delta V_{\rm FB}$ under the same sweeping voltage, the faster program/erase speed, the lower charge loss even at 200 °C for 10^4 s, the wider temperature insensitive regions, and the good endurance characteristics. The electrons tunneling thickness as well as r-c efficiency in the CTL and the balance of two competing electron loss mechanisms in B-B and F-B regions collectively contribute to the improved memory characteristics. In view of the trade-off between the operation speed and retention characteristics, the designed $Zr_xSi_{1-x}O_2$ CTL with combining B-B and F-B should be a promising candidate for future nonvolatile memory applications.

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