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Numerical and analytical investigations for the SOI LDMOS with alternated high-k dielectric and step doped silicon pillars*

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This paper presents a new silicon-on-insulator (SOI) lateral-double-diffused metal-oxide-semiconductor transistor (LDMOST) device with alternated high-k dielectric and step doped silicon pillars (HKSD device). Due to the modulation of step doping technology and high-k dielectric on the electric field and doped profile of each zone, the HKSD device shows a greater performance. The analytical models of the potential, electric field, optimal breakdown voltage, and optimal doped profile are derived. The analytical results and the simulated results are basically consistent, which confirms the proposed model suitable for the HKSD device. The potential and electric field modulation mechanism are investigated based on the simulation and analytical models. Furthermore, the influence of the parameters on the breakdown voltage (BV) and specific on-resistance ($R_{on,sp}$) are obtained. The results indicate that the HKSD device has a higher BV and lower $R_{on,sp}$ compared to the SD device and HK device.

Keywords: high-k dielectric, step doped silicon pillar, model, breakdown voltage

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1. Introduction

Silicon-on-insulator (SOI) lateral double-diffused metal oxide semiconductor (LDMOS) devices are applicable to high-voltage power integrated circuits for industrial and automotive applications, due to their properties of ideal isolation, high breakdown voltage, low leakage current, and good compatibility.[1–3] One of the most important issues in the design of SOI LDMOS devices is to relieve the contradiction between the breakdown voltage (BV) and specific on-resistance $R_{on,sp}$. To overcome such a contradiction, designs of drift doping profiles have been explored to modulate the electric field of SOI LDMOS devices.[4–6] The step doped (SD) profile is one of the most popular technologies, which has been applied to many structures of lateral power devices.[6–10] The SD technology leads to a higher BV than the uniformly doped profile while providing a simplification in the design and processing when compared to the linearly graded profile.[6] The analytical model and experimental results indicate that the step doping technology has a merit of the trade-off between the performance and fabrication cost.[9,10]

In this paper, a new SOI LDMOS device with alternated high-k dielectric and step doped silicon pillars (HKSD) is proposed. The electric field could be improved and the doping profile could be modulated due to the assistant depletion of the high-k dielectric pillars, which results in an improvement of the BV and reduction of the $R_{on,sp}$.[11–14] With the employed side high-k dielectric into the SD device, the electric field is further modulated and a higher BV and higher doping concentration can be obtained compared to the SD device without side high-k dielectric.

This paper also presents the analytical model for the HKSD device to reveal the modulation effect of step doped technology and the high-k dielectric pillars on the characteristics of this new device. The dependence of the electric field, the optimal breakdown voltage and the optimal doping profile on the device parameters are compared and discussed. This physical model matches the simulation results very well and provides a useful guide on the design of the HKSD device.

2. Device structure and analytical model

2.1. Device structure

The three-dimensional structure of the HKSD device is shown in Fig. 1(a). The drift region of the proposed HKSD device contains the alternated high-k pillars and silicon pillars. Each silicon pillar is divided into n uniformly doped zones, N_i $(i = 1,2,\ldots,n)$ is defined as the doping concentration for the i-th zone of the silicon pillar. The doping concentration is increased with steps of the doping increment ΔN. The schematic of the doping concentration in the silicon pillar is shown Fig. 1(a), N_i should satisfy $N_i = N_1 + 2(i-1)N_1$ according to the proposed model. By doping a suitable dose in each zone and employing a suitable high-k dielectric, the

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applied voltage is sustained by each zone averagely, resulting in a higher breakdown voltage.

The x–z cross-section of one basic unit of the HKSD device is shown in Fig. 1(b). W_D and W_S are the widths of the high-k dielectric pillar and silicon pillar, respectively. The relative permittivity of the high-k dielectric, silicon, and oxide are ε_D, ε_S and ε_{ox}, respectively. L_d and W_d are the total length of the drift region and the width of the basic unit. The basic parameters and their values used in this paper are presented in Table 1.

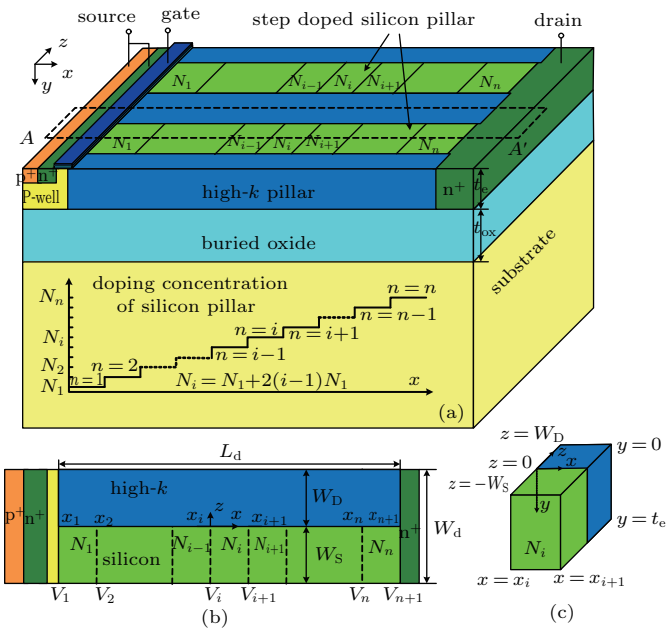


Fig. 1. (a) Three-dimensional structure of the HKSD device and the schematic of doping concentration in silicon pillar. (b) The x–z cross-section of one basic unit of the HKSD device. (c) The Gaussian box of the i-th zone.

Table 1. Device parameters and symbols.

Parameters	Value
thickness of epitaxial layer, t_e	1 μm
thickness of buried oxide layer, t_{ox}	3 μm
length of drift region, L_d	30, 40, 50, 60 μm
width of drift region of basic unit, W_d	2 μm
silicon width of one basic unit, W_S	0.5 μm
dielectric width of one basic unit, W_D	0.5 μm
permittivity of oxide, ε_{ox}	3.9
permittivity of silicon, ε_s	11.8
permittivity of dielectric, ε_D	25, 50, 80, 100
doping concentration of i-th zone, N_i	optimized

The main feature of the proposed HKSD device is the alternated high-k dielectric pillars and step doped silicon pillars in the drift region. The technique to realize the high-k dielectric pillars in the drift region has been discussed in Refs. [12,14]. After etching the trenches, the high-k dielectric is deposited into the trenches by pulsed-laser deposition. Then, the chemical mechanical polishing is used to polish the surface. The alternated high-k dielectric pillars and silicon pillars are formed. The next step is to realize the step doped silicon pillars, $n-1$ ions implanting with the specific dose are implemented, then the step doped silicon pillars are obtained after the drive-in anneal.[15,16] After the step doped silicon pillars are formed, the p-well, the gate oxide and polysilicon, the p^+ region, the n^+ source/drain regions, and the metal electrodes are formed by the standard deposition, patterning and metallization techniques in the CMOS process.

2.2. Potential and electric field model

For exploring the physical insight of the drift region with alternated high-k dielectric and step doped silicon pillars, the Gaussian box of the i-th zone is considered and illustrated in Fig. 1(c). The coordinate axis is established as shown in this figure. In the following discussion, the length of each zone is defined as a fixed value of L, which is equal to L_d/n. Typically, the potential functions $\varphi_{D(i)}(x,y,z)$ and $\varphi_{S(i)}(x,y,z)$ in the high-k region and silicon region of this Gaussian box satisfy the three-dimensional Poisson equation, expressed as

$$\frac{\partial^2\varphi_{S(i)}}{\partial x^2}+\frac{\partial^2\varphi_{S(i)}}{\partial y^2}+\frac{\partial^2\varphi_{S(i)}}{\partial z^2}=-\frac{qN_i}{\varepsilon_S},$$
$$x_i\leqslant x\leqslant x_{i+1},\quad 0\leqslant y\leqslant t_e,\quad -W_S\leqslant z\leqslant 0, \tag{1}$$
$$\frac{\partial^2\varphi_{D(i)}}{\partial x^2}+\frac{\partial^2\varphi_{D(i)}}{\partial y^2}+\frac{\partial^2\varphi_{D(i)}}{\partial z^2}=0,$$
$$x_i\leqslant x\leqslant x_{i+1},\quad 0\leqslant y\leqslant t_e,\quad 0\leqslant z\leqslant W_D. \tag{2}$$

The boundary conditions for the solutions are as follows:

(1) $[\varphi_S]_{x=x_i}=[\varphi_D]_{x=x_i}=V_i$ and $[\varphi_S]_{x=x_{i+1}}=[\varphi_D]_{x=x_{i+1}}=V_{i+1}$. The V_i and V_{i+1} are defined as the potential at the edge of the i-th zone.

(2) $[\partial\varphi_S/\partial y]_{y=0}=[\partial\varphi_D/\partial y]_{y=0}=0$ since the vertical electric field at the surface ($y=0$) may be minimized.[11]

(3) $[\partial\varphi_S/\partial y]_{y=t_e}=\varphi_S\varepsilon_{ox}/\varepsilon_S t_{ox}$ and $[\partial\varphi_D/\partial y]_{y=t_e}=\varphi_D\varepsilon_{ox}/\varepsilon_D t_{ox}$ due to the continuity of electric flux density at the silicon and oxide interface ($y=t_e$).[11]

(4) $[\partial\varphi_S(x,z)/\partial z]_{z=-W_S}=0$ and $[\partial\varphi_D(x,z)/\partial z]_{z=W_D}=0$ since $z=-W_S$ and $z=W_D$ are symmetrical lines.[13]

(5) $[\varphi_S]_{z=0}=[\varphi_D]_{z=0}$, $\varepsilon_s[\partial\varphi_S/\partial z]_{z=0}=\varepsilon_D[\partial\varphi_D/\partial z]_{z=0}$ and $[\partial^2\varphi_S/\partial x^2]_{z=0}=[\partial^2\varphi_D/\partial x^2]_{z=0}$ according to the continuances of the potential, electric field, and doping at the interface of the high-k and silicon region.[13]

Solving the 3D Poisson equation for the Gaussian box under the boundary conditions,[14] the potential expression and electric field expression at the x-direction along the AA' line is derived as

$$\varphi_{S(i)}(x)=(V_{i+1}-\phi_i)\frac{\sinh[(x-x_i)/T]}{\sinh(L/T)}+(V_i-\phi_i)\frac{\sinh[(x_{i+1}-x)/T]}{\sinh(L/T)}+\phi_i, \tag{3}$$

$$E_{S(i)}(x) = \frac{V_{i+1}-\phi_i}{T}\frac{\cosh[(x-x_i)/T]}{\sinh(L/T)} - \frac{V_i-\phi_i}{T}\frac{\cosh[(x_{i+1}-x)/T]}{\sinh(L/T)}, \quad (4)$$

with

$$T = t_S\sqrt{[1+(W_D/W_S)(\varepsilon_D/\varepsilon_S)]/[1+(W_D/W_S)]},$$
$$t_S = \sqrt{t_e^2/2 + t_{ox}t_e\varepsilon_s/\varepsilon_{ox}},$$
$$\phi_i = \frac{qN_it_S^2}{\varepsilon_s}\frac{W_S}{(W_S+W_D)}.$$

The V_i in Eqs. (3) and (4) can be obtained by solving the $E_{S(i)}(x=x_i) = E_{S(i-1)}(x=x_i)$ together with the condition of $V_1 = 0$, expressed as

$$V_i = V_{i+1}A_{i-1} + B_{i-1}, \quad i = 1,\ldots,n, \quad (5)$$

with

$$\begin{cases} A_i = 1/[2\cosh(\Delta x/T) - A_{i-1}], \\ B_i = A_iB_{i-1} + A_i(\phi_{i+1}+\phi_i)[\cosh(\Delta x/T)-1], \end{cases}$$

V_{n+1} equals the external voltage V_d applied on the drain, therefore V_i can be obtained by the boundary conditions $V_{n+1} = V_d$. Actually, the voltage V_d can be sustained by each zone averagely when considering the optimization of the HKSD device, then V_i will be expressed as $V_B \cdot (i-1)/n$.

3. Simulation and analytical results

To investigate the mechanism of the proposed HKSD device, the comparison between the HKSD devices with different n (n = 1, 2, 3, and 4) are conducted. The equipotential contours for the HKSD devices at their respective optimal BV are shown in Fig. 2. In Fig. 2(a), the device with $n = 1$ represents the HK device which has no step doped zones in the silicon pillar. For this device, the potential lines in the middle of the drift region are still sparsely distributed although the high-k dielectric can modulate the distribution of the potential lines.[11] Therefore, the SD technology is introduced to improve the breakdown voltage by the further modulation of SD technology on the equipotential contours. As depicted in Fig. 2(b), the potential lines are concentrated in the middle of the drift region, where is the interface of the different doped zones. Obviously, there are also concentrate effect of the potential lines in Figs. 2(c) and 2(d). Therefore, the applied voltage can be sustained by each zone regularly and the electric field has been modified, leading to the improvement of breakdown voltage.

Figure 3 illustrates the simulated and analytical results of the potential distributions along the A–A' line for the HKSD devices at their respective optimal BV. The results of the SD devices with the same n are also given to make a comparison. The solid lines represent the analytical results of Eq. (4), and the dots are the simulated results extracted from the TCAD simulator. The analytical model and simulation results are matched perfectly. As shown in Fig. 3, the potential drops always locate at the interfaces of different zones or the junctions, which produces the electric field peaks. The potential drops could be reduced by increasing n, then the electric field peaks reduce accordingly. Compared to the SD device with the same n, it is obvious that the HKSD device has a better potential distribution due to the modulation of the high-k dielectric pillar.

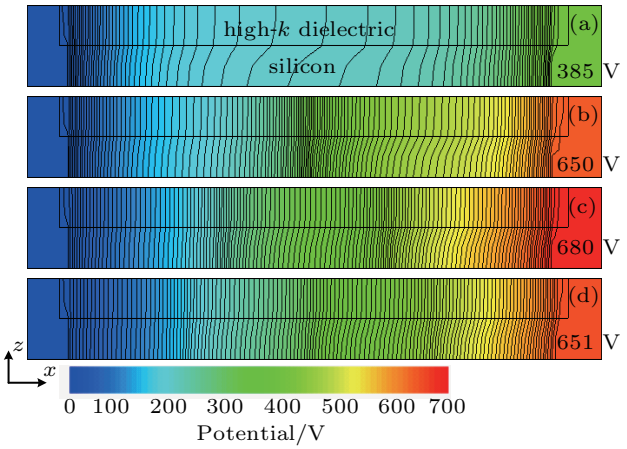


Fig. 2. The equipotential contours for the HKSD devices ($\varepsilon_D = 100$, $L_d = 60$ μm) with different n, (a) $n = 1$, (b) $n = 2$, (c) $n = 3$, (d) $n = 4$.

Figure 4 illustrates the simulated and analytical results of the electric field distribution along the A–A' line for the HKSD devices at their respective optimal BV. The analytical results and the simulated results are basically consistent. As seen from Fig. 4(a), the device with $n = 1$ has a low electric field in the middle of the drift region, which results in a low BV. With introducing the SD technology, new electric field peaks are formed at the interface of the different doped zones. Therefore, the HKSD device has a higher BV compared to the device without step doped zones. With the increasing n, it achieves a more uniform electric field and a higher breakdown voltage. On the other hand, figure 4 also indicates that the electric field valley of each zone in the HKSD device is higher than that of the SD device, while the electric field peak of the HKSD device is lower than that of the SD device, this is because the high-k dielectric enhances the RESURF effect. Therefore, the HKSD device has a higher BV compared to the SD device. Note that the BV of the HKSD device with $n = 3$ is higher than the HKSD device with $n = 4$, this is because of the more step doped zones will reduce the electric field peaks, which may cause the decreasing BV. Therefore, the reasonable design of the step doped zones in HKSD devices is necessary for obtaining the highest BV.

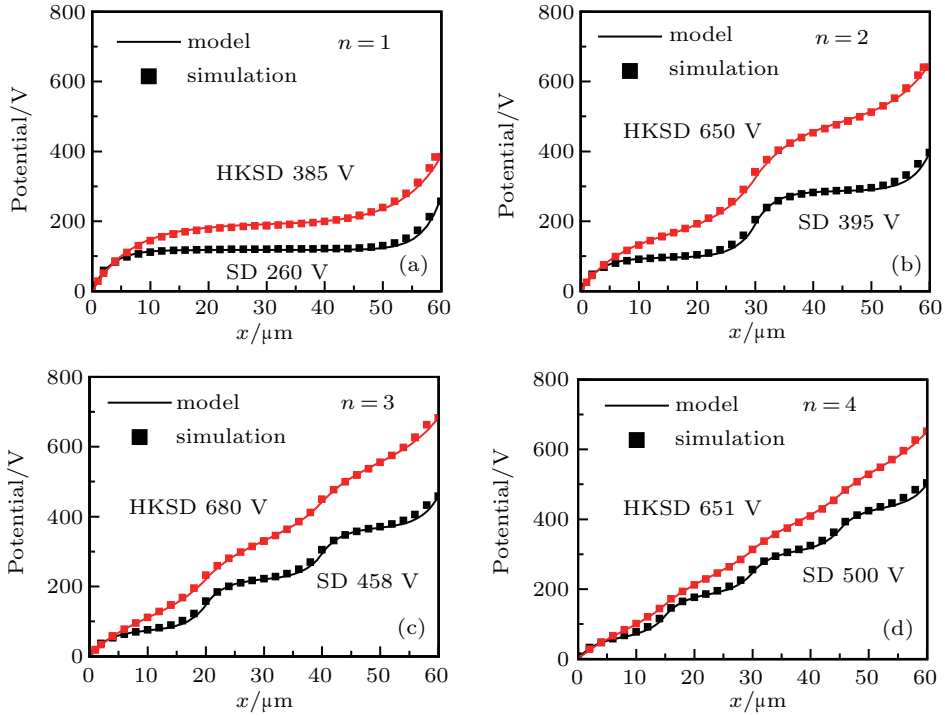


Fig. 3. The potential distributions for the HKSD devices ($\varepsilon_D = 100$, $L_d = 60$ μm) and SD devices ($L_d = 60$ μm) with different n: (a) $n = 1$, (b) $n = 2$, (c) $n = 3$, (d) $n = 4$.

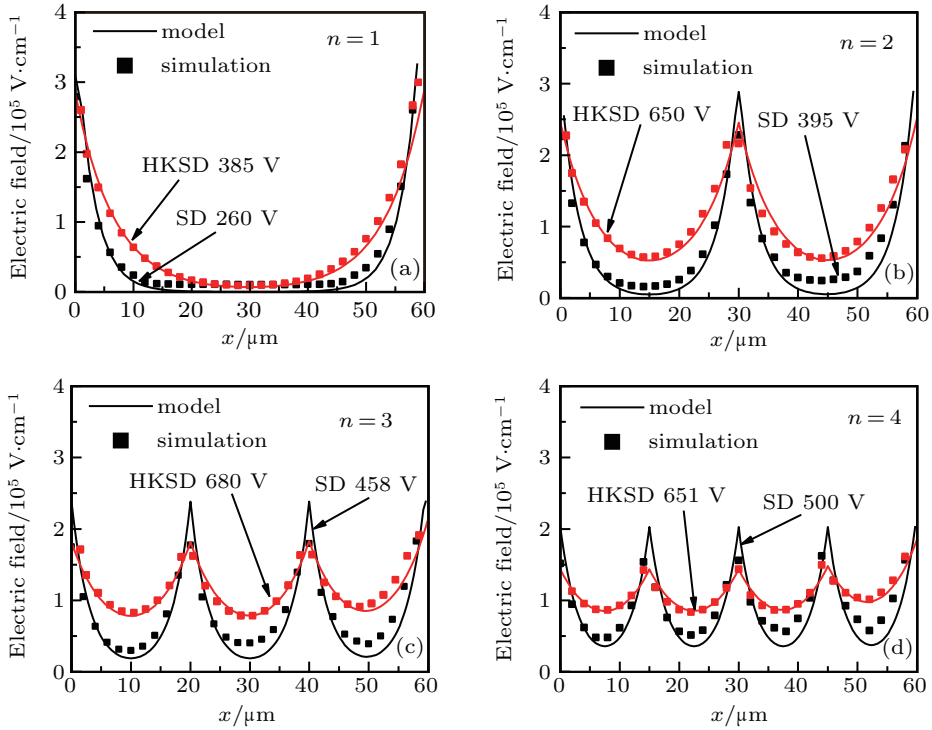


Fig. 4. The electric field distributions for the HKSD devices ($\varepsilon_D = 100$, $L_d = 60$ μm) and SD devices ($L_d = 60$ μm) with different n: (a) $n = 1$, (b) $n = 2$, (c) $n = 3$, (d) $n = 4$.

4. Optimizations and discussion

For the HKSD device, the step doped profile brings electric field peaks at the interfaces of the adjacent zones, which comes from the mechanism same as the SD device. To optimize the breakdown voltage, the peck values are equal and they should be equal to the critical value of E_C. Substituting Eq. (4) into $E_{S(i)}(x = x_i) = E_{S(i)}(x = x_{i+1}) = E_C$, the optimal breakdown voltage (BV_{opt}) is satisfied:

$$BV_{opt} = 2nE_C T \tanh(L_d/2nT), \tag{6}$$

and the doping concentration N_i is satisfied:

$$N_i = N_1 + 2(i-1)N_1, \tag{7}$$

where N_1 is the doping concentration of the first zone, expresses as

$$N_1 = E_C \varepsilon_s T \tanh(L_d/2\,nT) W_d/W_S q t_S^2. \quad (8)$$

Then, the doping increment ΔN equals $2N_1$. For the conventional SD device, T equals t_S, then equation (6) can be expressed as $BV_{opt} = 2nE_C t_S \tanh(L_d/2nt_S)$ and equation (8) can be expressed as $N_1 = E_C \varepsilon_s \tanh(L_d/2nt_S)/qt_S$, which are corresponding to Ref. [7].

Figure 5 gives the dependence of BV_{opt} on n for the HKSD device and the SD device. The analytical results are in agreement well with the simulation results for both the devices. As shown in Fig. 5, the BV of the HKSD device is much larger than that of the SD device with the same n because of the employed high-k dielectric. For the SD device, the BV increases regularly with the increase of n. While for the HKSD device with $n = 2$, 3 or 4, their BVs are at the same level. The HK device ($n = 1$) has a low BV because its middle drift region does not sustain the appropriate voltage as shown in Fig. 2. When n is large enough, the $\tanh(L_d/2nT)$ approximates to $L_d/2nT$, then equaiton (6) can be written as $BV_{ideal} = E_C L_d$. This means that the breakdown voltage is irrelevant to structure parameters except for the L_d. Therefore, the BVs with or without the side high-k dielectric will be the same.

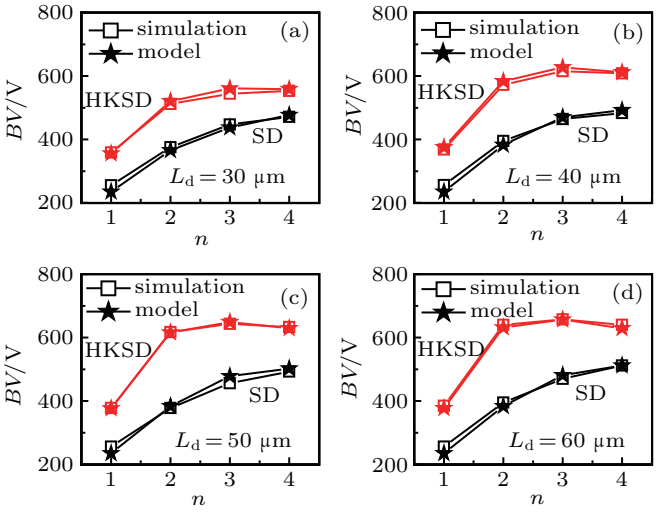


Fig. 5. Dependence of BV on n for the HKSD device ($\varepsilon_D = 100$) and the SD device.

Figure 6 gives the dependence of N_1 on n for the HKSD device and the SD device, the doping concentration of the i-th zone satisfies Eq. (7). The analytical results and simulation results are well matched. The results indicate that the N_1 reduces with the increasing n, which can be explained by Eq. (8). As shown in the figure, N_1 decreases smoothly with the increase of n for the SD device, while N_1 decreases rapidly with the increase of n for the HKSD device. The doping concentration of the HKSD device is much higher than that of the SD device, which is due to the assistant depletion of the high-k dielectric. When nT is larger enough, N_1 of the HKSD device is W_d/W_S times of N_1 of the SD device, which only depends on the width of the high-k dielectric pillar but not on the permittivity of the high-k dielectric.

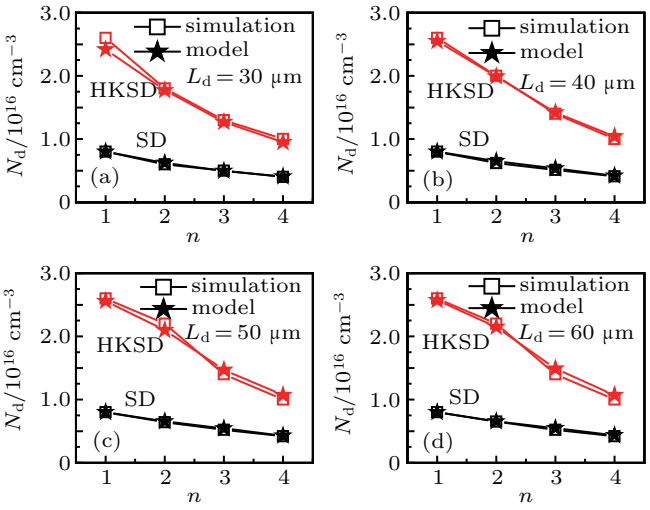


Fig. 6. Dependences of N_d on n for the HKSD device ($\varepsilon_D = 100$) and the SD device.

Figure 7 shows the on-state characteristic of the SD device, the HK device, and the HKSD ($n = 2$) device. According to the subgraph, the threshold voltage of all the three devices is 1.2 V, because they have the same parameters of the channel and gate oxide layer. The I–V curves show that the HK and HKSD devices have higher I_{DS} compared to the SD device at the same V_{DS}. The slopes of the linear region in the I–V curves of the HK and HKSD devices are much higher than that of the SD device, which means that the HKSD device has lower specific on-resistance.

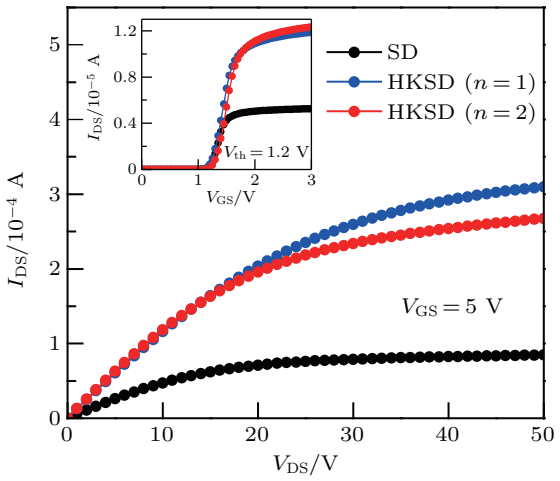


Fig. 7. Transfer and I–V characteristics of the HKSD and SD devices.

The specific on-resistance plays a relevant role in the lateral device. For the step doped region, the drift region resistance R_d is obtained by connecting the resistor of each zone in

series, expressed as:

$$R_{\rm d} = \sum_{1}^{n} \frac{L_{\rm d}/n}{q\mu_n N_i W_{\rm S}}. \tag{9}$$

Therefore, the specific on-resistance of the HKSD device can be expressed as:

$$R_{\rm on,sp} = (R_{\rm d} + R_x) \times S, \tag{10}$$

where S is the area of the device containing the dielectric pillar and silicon pillar, R_x is defined as the additional resistances such as the channel resistance, contact resistance, source resistance, and drain resistance.

Figure 8 shows the dependence of $R_{\rm on,sp}$ on n for the HKSD and SD devices. We calculate the drift region resistance and add a fixed value of R_x when analyze the total device on-resistance. The calculated specific on-resistance fits the simulated results well with the given parameters. As shown in this figure, the resistance of the HKSD device is lower than that of the SD device with the same step number n due to the assistant depletion of high-k dielectric on the doping profile of the silicon pillar. The specific on-resistance of the HKSD device with $n = 2$ is smallest. When n increases, the reduced N_1 results in a higher resistance of the first zone, the total resistance of the drift region serially connected by the resistance of each zone will be increased accordingly. Contrasting the four subgraphs of Fig. 8, the device with longer drift region has a large specific on-resistance because the large device area.

Since the $R_{\rm on,sp}$ strongly depends on the ratio $W_{\rm D}/W_{\rm S}$, figure 9 illustrates the influence of $W_{\rm D}/W_{\rm S}$ on the doping concentration and $R_{\rm on,sp}$ under a given $W_{\rm S}$. $W_{\rm D}/W_{\rm S} = 0$ means the SD device without high-k dielectric. It is obvious that the $R_{\rm on,sp}$ is reduced by employing the high-k dielectric because of the modulation of the high-k dielectric on the doping concentration. As shown in the figure, the doping concentration increasing regularly with the increasing $W_{\rm D}/W_{\rm S}$. However, the higher $W_{\rm D}/W_{\rm S}$ means a larger surface area, which results in the increasing $R_{\rm on,sp}$. In consideration of the process tolerance, $W_{\rm D}/W_{\rm S} = 1$ is suitable for design of the HKSD device.

According to the above discussions, the high-k materials can improve the breakdown voltage by modulating the electric field and reduce the $R_{\rm on,sp}$ by increasing the doping concentration of silicon pillars. Therefore, figure 10 gives the simulation results of dependence of BV and $R_{\rm on,sp}$ on the permittivity $\varepsilon_{\rm D}$. The permittivity values of 25, 50, 80, and 100 are corresponding to the high-k materials of HfO_2,[17] $ZrTiO_4$,[18] TiO_2,[19]

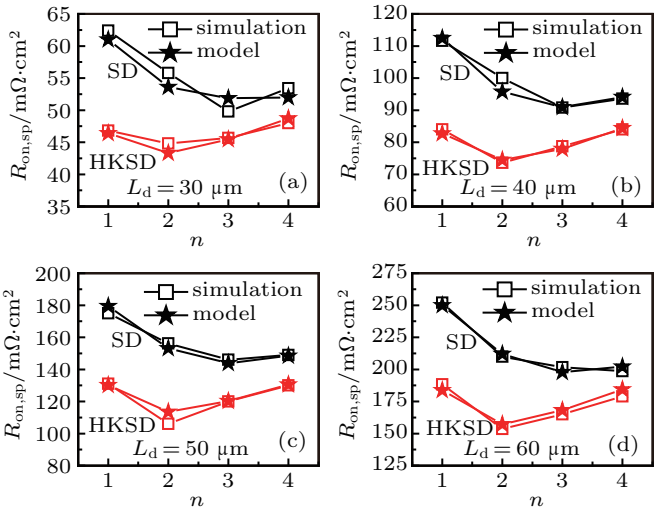


Fig. 8. Dependence of $R_{\rm on,sp}$ on n for the HKSD device ($\varepsilon_{\rm D} = 100$) and the SD device.

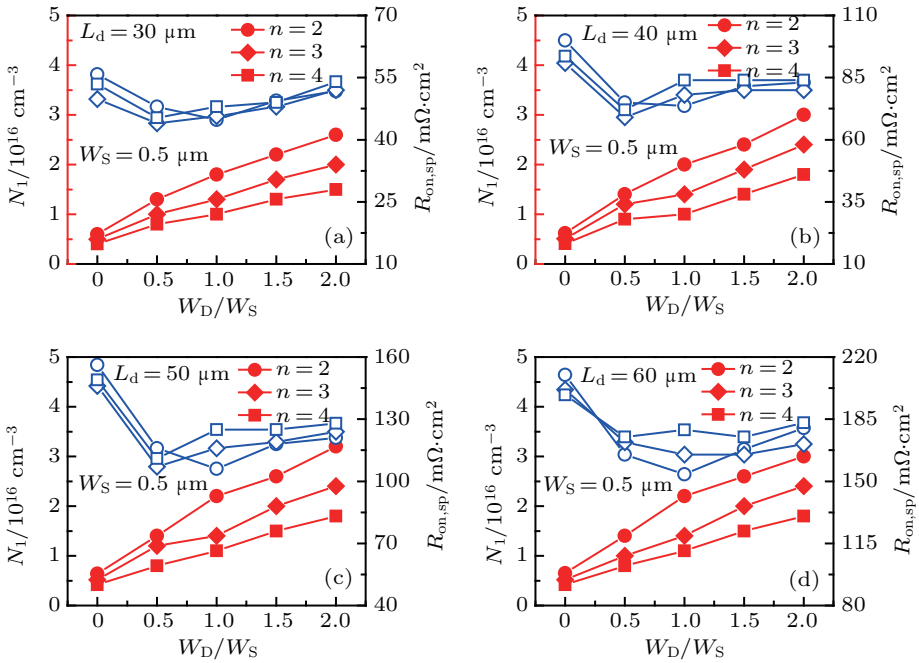


Fig. 9. Dependences of N_1 and $R_{\rm on,sp}$ on $W_{\rm D}/W_{\rm S}$ for the HKSD devices with different $L_{\rm d}$.

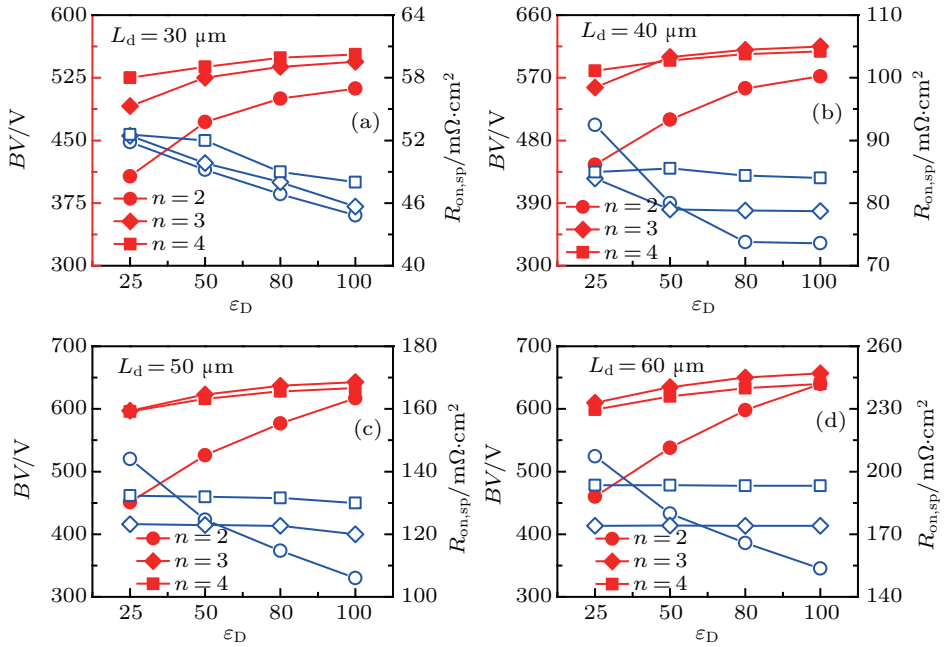


Fig. 10. Dependences of BV and $R_{on,sp}$ on ε_D for the HKSD devices with different L_d.

$SrTiO_3$.[20] As shown in this figure, the HKSD device with the higher ε_D has a higher BV. It is obvious that the HKSD device with $n = 2$ is more easily affected by ε_D, but with a high ε_D, the BV approaches equality. The HKSD device with $n = 3$ demonstrates the highest BV among all the devices when L_d is large enough. Figure 10 also indicates that the ε_D has great influence on the $R_{on,sp}$ of the HK device with $n = 2$, while has small influence when $n = 3$ and $n = 4$. When L_d is large enough, the $R_{on,sp}$ is almost the same.

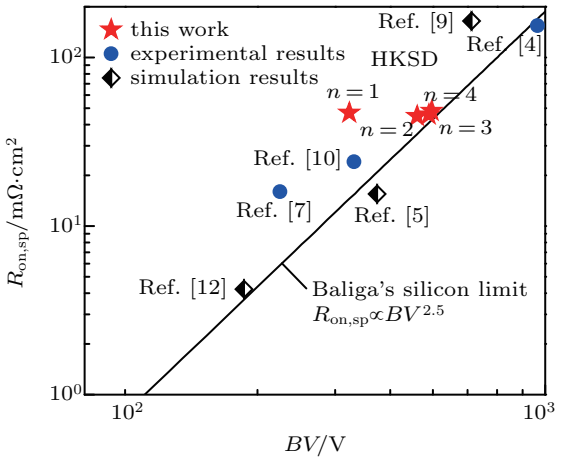


Fig. 11. $R_{on,sp}$ versus BV for different LDMOS devices.

The relationship between the $R_{on,sp}$ and BV of the HKSD device in this work together with some experimental data[4,7,10] and simulated data[5,9,12] reported previously are given in Fig. 11. The results of this work are related to the HKSD devices with $L_d = 30$ μm, $\varepsilon_D = 100$ and the specific structure parameters given in Table 1. Baliga's ideal silicon limit curve[21] is also used to make the comparison. We can see that the results of the HKSD devices with $n = 2$, $n = 3$ and $n = 4$ almost approach to the silicon limit rather than the HKSD devices with $n = 1$ and some other devices. Thus, the HKSD device exhibits a super performance on the trade-off between the $R_{on,sp}$ and BV.

5. Conclusions

A novel HKSD SOI LDMOS device and its analytical model are presented in this paper. The main feature of this new device is the alternated high-k dielectric and step doped silicon pillars of the drift region. First, the potential and electric field are obtained to investigate the mechanism of the HKSD device, then the optimal breakdown voltage and the optimal doping profile of each zone are calculated to guide the design of HKSD devices. The analytical results fit the simulation results well, which provides the validity of the proposed model. The on-state characteristic is also given to show the advance of the HKSD device. The results have demonstrated that the HKSD device has a higher breakdown voltage and lower specific on-resistance compared to the SD and HK devices.

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