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Improved performance of back-gate MoS_2 transistors by NH_3-plasma treating high-k gate dielectrics*

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NH_3-plasma treatment is used to improve the quality of the gate dielectric and interface. Al_2O_3 is adopted as a buffer layer between HfO_2 and MoS_2 to decrease the interface-state density. Four groups of MOS capacitors and back-gate transistors with different gate dielectrics are fabricated and their C–V and I–V characteristics are compared. It is found that the Al_2O_3/HfO_2 back-gate transistor with NH_3-plasma treatment shows the best electrical performance: high on–off current ratio of 1.53×10^7, higher field-effect mobility of 26.51 $cm^2/V{\cdot}s$, and lower subthreshold swing of 145 mV/dec. These are attributed to the improvements of the gate dielectric and interface qualities by the NH_3-plasma treatment and the addition of Al_2O_3 as a buffer layer.

Keywords: MoS_2 transistor, high-k dielectric, NH_3-plasma treatment, oxygen vacancy, mobility

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1. Introduction

In recent years, molybdenum disulfide (MoS_2), as one of the most representative two-dimensional semiconductor materials, has attracted more and more attention of researchers for its unusual electronic and optical properties.[1,2] Compared to graphene, atomically thin MoS_2 has a thickness-dependent band gap ranging from 1.2 eV to 1.9 eV[3] and a relatively high intrinsic electron mobility at room temperature,[1] which make it possess great advantages in device application. The field-effect transistor (FET) based on ultra-thin (monolayer or multilayer) MoS_2 channel exhibits high on–off current ratio ($I_{on}/I_{off} > 10^6$), near-ideal sub-threshold swing, and reasonably high electron mobility,[1,4–9] which is very suitable for fabricating low-power logic circuits,[10] non-volatile memory,[11,12] and ultra-sensitive photodetectors.[13,14] However, although great progress has been made in this field, yet the performance of the MoS_2 transistors is far from its theoretical value.[15,16]

As a channel material, forming a good interface with the gate dielectric is an important issue that should be addressed for fabricating high-performance transistors. The use of high-k dielectrics is extensively considered for the MoS_2 transistor due to their roles of reducing the interface-state density and the strong dielectric screening effect on Coulomb scattering. As reported, Al_2O_3 and HfO_2 are the most commonly used high-k dielectrics and to our best knowledge, Al_2O_3 is often used as a buffer layer between HfO_2 and MoS_2 to form a stack structure of $HfO_2/Al_2O_3/MoS_2$ because of its lower interface-state density with MoS_2.[17–20] However, due to the effect of self-growth, a large number of oxygen vacancies exist in the gate dielectric,[21–23] which would block the carrier transportation in the channel. For solving this problem, some treatments were carried out to improve the quality of the gate dielectric, e.g., NH_3-plasma treatment. Hong Bae Park *et al.* firstly confirmed that NH_3-plasma treatment on the Al_2O_3 interlayer between HfO_2 and Si substrate can result in a significant reduction of the fixed charge density and interfacial defects of the obtained MOS capacitors.[24] Wen *et al.* annealed the gate dielectrics (HfO_2 and HfTiO) of back-gate MoS_2 transistors in NH_3 atmosphere, obtaining a great improvement of the device performance.[25,26] So, it has been showed that the NH_3-plasma treatment has a potential of greatly improving the quality of the gate dielectric to achieve good device performances. Therefore, in this work, back-gate MoS_2 FETs with HfO_2 or Al_2O_3/HfO_2 as the gate dielectrics are fabricated, and the NH_3 plasma is applied to treat the two gate dielectrics before transferring the MoS_2. The involved mechanisms that the NH_3-plasma treatment improves the electrical performance of the MoS_2 transistor are analyzed by means of the C–V measurement of the relevant MOS capacitors before and after the NH_3-plasma treatment. Excellent electrical properties have been achieved for the MoS_2 transistors with the NH_3-plasma treatment, demonstrating that it is an effective way to improve the quality of gate dielectrics and thus the electrical performance of MoS_2 transistors.

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2. Experiments

Heavily-doped p^+ silicon with resistivity of $\sim$ 0.01 Ω·cm was used as the starting substrate and back gate. An amorphous HfO_2 was deposited by the atomic layer deposition (ALD) method using tetrakis (dimethylamino) hafnium (TDMAH) and H_2O as the precursors and high-purity nitrogen as the carrier and purge gas. The TDMAH source was heated to 75 ℃ while the H_2O source was kept at room temperature. The pulse time for TDMAH and H_2O was 0.1 s and 0.02 s, respectively. The post-TDMAH or H_2O pulse purge was 30 s. The HfO_2 film was deposited at 200 °C and finished after 175 cycles or 152 cycles, respectively, resulting in a thickness of 15 nm or 13 nm. Subsequently, Al_2O_3 was deposited on the surface of the 13-nm HfO_2 using trimethylaluminum (TMA) and H_2O as the precursors and nitrogen as the carrier and purge gas. The deposition temperature was maintained at 200 °C and the injection schedule for one cycle of Al_2O_3 deposition was 0.02 s/15 s/ 0.015 s/15 s of TMA/purge/H_2O/purge. The deposition was finished after 20 cycles to form a 2-nm Al_2O_3 film. Then, an NH_3 (99.9995%)-plasma treatment was performed at 300 ℃ for 10 min with a flow rate of 10 sccm, 26.66-Pa vacuum, and 120-W power for a part of gate dielectrics of 15-nm HfO_2 or 2-nm Al_2O_3/13-nm HfO_2, which are reasonably good NH_3-plasma treatment conditions summarized from our previous experiments. Multilayer MoS_2 flakes ($\sim$ 6 nm) were mechanically exfoliated from bulk MoS_2 crystals and transferred to the surface of the HfO_2/p^+-Si or $Al_2O_3/HfO_2/p^+$-Si stack gates, because the multilayer MoS_2 flake has larger drive current than monolayer MoS_2 due to its higher density of states, multiple conduction channels, and higher extrinsic carrier mobility resulted from the stronger Thomas–Fermi screening.[1,4] Source/drain regions (50 μm ×50 μm) were defined on the top of the MoS_2 flakes using e-beam lithography (EBL, JEOL6510 with Nanometer Pattern Generation System) and Cr (15 nm) and Au (50 nm) were deposited by electron-beam evaporation at room temperature, followed by a liftoff process. The samples were then annealed at 300 °C in a vacuum tube furnace for 180 s to remove resist residues and decrease the contact resistance. For clarity, the above four groups of devices without or with NH_3-plasma treatment are denoted as HfO_2, NH_3-HfO_2, Al_2O_3/HfO_2, and NH_3-Al_2O_3/HfO_2 samples, respectively. At least four transistors were measured for each sample and the extracted parameters were their average values. Since the samples were fabricated under the same conditions, their contact resistances could be at a similar level.

The surface topography of the HfO_2 and Al_2O_3/HfO_2 gate dielectrics was measured by atomic force microscopy (AFM, Bruker Dimension Edge SPM System). High-frequency (HF, 1 MHz) *C*–*V* characteristics were measured at room temperature using Agilent 4284A precision LCR meter, and the current–voltage curve of the transistors was measured using Keithley 4200-SCS semiconductor parameter analyzer. All measurements were performed at room temperature in a dark atmospheric environment with electromagnetic shielding.

3. Results and discussion

Figures 1(a) and 1(b) show the cross-sectional diagrams of the MoS_2 FETs with two kinds of back-gate structures. Figure 1(c) shows the thickness of the MoS_2 film corresponding to different colors under optical microscope and figure 1(d) is the fabricated back-gate MoS_2 FET under optical microscope. The channel length (*L*) is 2 μm and the channel width (*W*) is 1.2–3.1 μm depending on the flake shape as shown in Fig. 1(d).

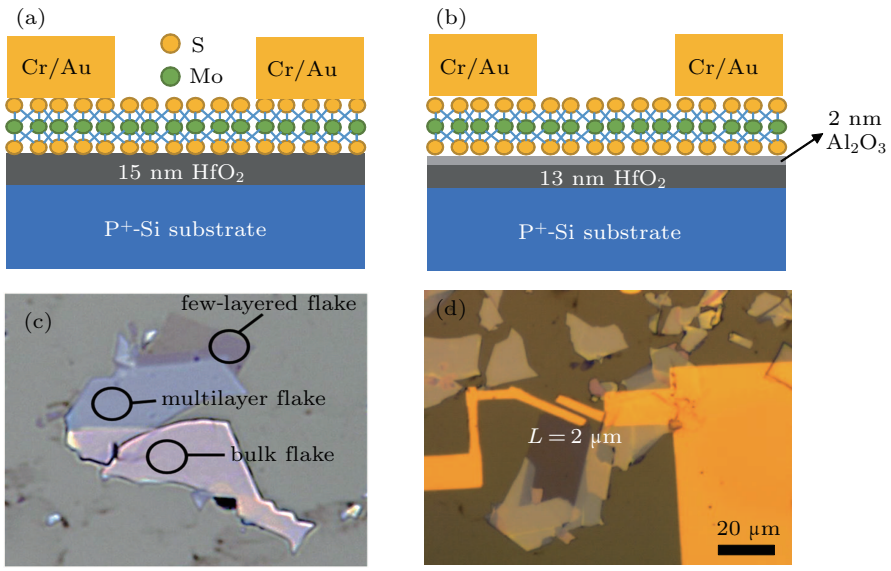


Fig. 1. Schematic diagram of the back-gate MoS_2 transistor structure: (a) HfO_2 gate dielectric, (b) Al_2O_3/HfO_2 gate dielectric, (c) thickness of MoS_2 film corresponding to different colors under optical microscope, (d) MoS_2 flake selected to fabricate transistor with *L* of 2 μm.

Figure 2(a) shows the typical HF C–V (1 MHz) curves for the metal/HfO_2/p^+-Si and metal/Al_2O_3/HfO_2/p^+-Si MOS capacitors with or without NH_3-plasma treatment. As compared to the NH_3-plasma treated samples, the HfO_2 and Al_2O_3/HfO_2 MOS capacitors without NH_3-plasma treatment exhibit poorer C–V characteristics: smaller depletion-region slope and decreased accumulation capacitance C_{ox} (38 pF and 35 pF, respectively). According to the formula $k_{eq} = C_{ox}t_{ox}/A\varepsilon_0$, where ε_0 and k_{eq} are the vacuum permittivity and the equivalent dielectric constant of the gate dielectric, respectively, A is the electrode area (7.85×10^{-5} cm^{-2}), and t_{ox} is the physical thickness of the gate dielectric, k_{eq} can be found to be 8.2 and 7.6 for the HfO_2 and Al_2O_3/HfO_2 gate dielectrics, respectively. However, after the NH_3-plasma treatment, the accumulation capacitance of the NH_3-HfO_2 and NH_3-Al_2O_3/HfO_2 samples is increased to 49 pF and 44 pF, and the relevant k_{eq} becomes 10.6 and 9.5, respectively. In addition, the flat-band voltage (V_{fb}) and the equivalent oxide-charge density (Q_{ox}) of these MOS capacitors can be extracted using the following equations:[27]

$$C_{fb} = C_{ox} \cdot \left(1 + \frac{75.7\sqrt{T/300}}{t_{ox}\sqrt{N_A}}\right), \quad (1)$$

$$Q_{ox} = -C_{ox} \cdot (V_{fb} - \varphi_{ms})/q, \quad (2)$$

where C_{fb} is the flat-band capacitance corresponding to V_{fb}, φ_{ms} is the work function difference between the gate electrode and substrate, T is the measurement temperature, q is the electron charge, C_{ox} is the oxide capacitance (accumulation capacitance) per unit area, and N_A is the substrate concentration. The electrical parameters of the four groups of MOS capacitors are listed in Table 1. Obviously, after the NH_3-plasma treatment, Q_{ox} can be significantly reduced and the relevant V_{fb} shifts positively. This is mainly attributed to the fact that the N atoms produced by NH_3 plasma can be incorporated into the oxide to form HfON[28] and AlON[29] with higher k_{eq}, and also can repair oxygen vacancies in the oxide[30,31] to reduce the positive trap charges and shift V_{fb} in the positive direction. The XPS analysis is used to confirm N incorporation due to the NH_3 plasma treatment, as shown in Figs. 2(b)–2(d). The Al 2p spectra of the Al_2O_3/HfO_2 and NH_3-Al_2O_3/HfO_2 samples are shown in Figs. 2(b) and 2(c), respectively. The obvious peak at 74.6 eV is in a good agreement with the banding energy of Al–O bond.[32] While in Fig. 2(c), a peak occurred at 73.1 eV is corresponding to the banding energy of Al–N bond,[33] indicating N incorporation into the stack dielectric, which is further supported by a distinct increase of N 1s peak after the NH_3-plasma treatment (NH_3-Al_2O_3/HfO_2 sample).

Table 1. Electrical parameters of p^+-Si/HfO_2/metal and p^+-Si/HfO_2/Al_2O_3/metal MOS capacitors with and without NH_3-plasma treatment.

Sample	Al_2O_3/HfO_2	NH_3-Al_2O_3/HfO_2	HfO_2	NH_3-HfO_2
C_{ox}/μF·cm^{-2}	0.45	0.56	0.48	0.62
$Q_{ox}/10^{12}$ cm^{-2}	2.30	1.63	2.31	1.85
V_{fb}/V	–0.67	–0.46	–0.75	–0.59
k_{eq}	7.6	9.5	8.2	10.6

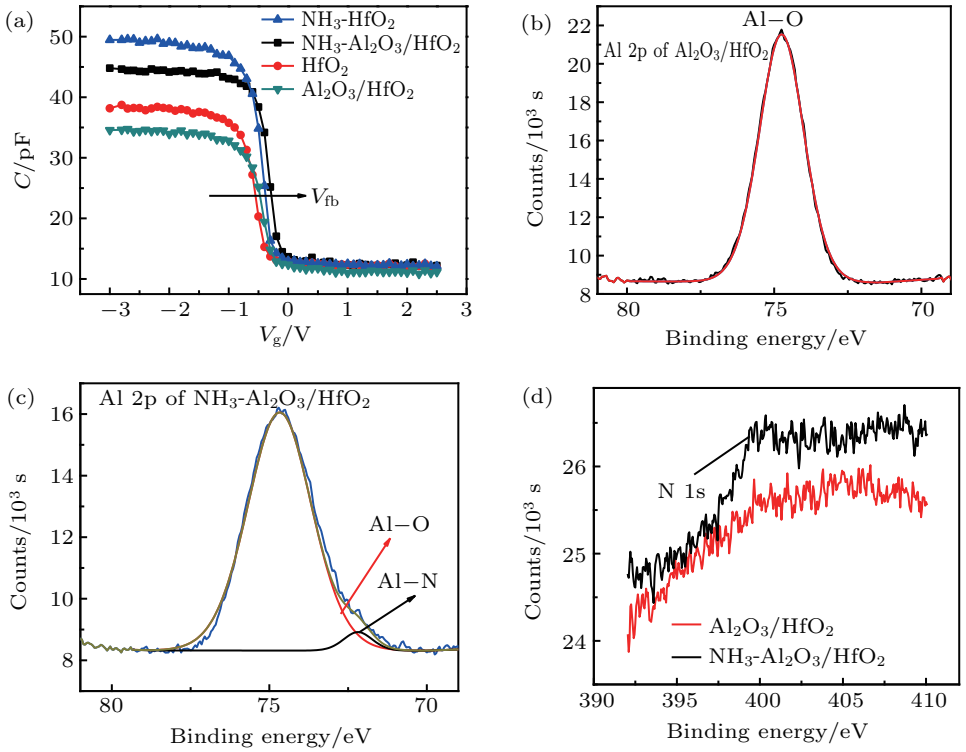


Fig. 2. (a) High-frequency C–V curves of all the MOS capacitors. Al 2p XPS spectra for (b) Al_2O_3/HfO_2 sample and (c) NH_3-Al_2O_3/HfO_2 sample. (d) N 1s XPS spectra before and after NH_3-plasma treatment on the stack dielectric of Al_2O_3/HfO_2.

Figure 3 shows the drain–source current (I_{ds}) versus drain–source voltage (V_{ds}) curves for high-k gate dielectric HfO_2 and Al_2O_3/HfO_2 back-gate MoS_2 transistors with or without NH_3-plasma treatment. It can be seen that all back-gate transistors are in n-channel enhancement mode. Furthermore, when gate–source voltage $V_{gs} = 3$ V and $V_{ds} = 2$ V, the driving current of the HfO_2 or Al_2O_3/HfO_2 back-gate MoS_2 transistor can be increased from 2.4 μA/μm or 3.4 μA/μm before the NH_3-plasma treatment to 12.4 μA/μm ($\sim 5.2\times$) or 15.6 μA/μm ($\sim 4.6\times$) after the NH_3-plasma treatment. The significant increase of the driving current is ascribed to the NH_3-plasma treatment that reduces the trap charges in the gate dielectric and thus Coulomb scattering on the channel carriers, improves the interfacial quality, and decreases the gate leakage, as shown below.

Figure 4 shows the transfer characteristic (I_{ds} vs. V_{gs}) of the four groups of back-gate MoS_2 transistors with $V_{ds} = 0.1$ V. The devices have a low off current (10^{-12} A) with an on/off current ratios of 10^6 and 10^7 before and after the NH_3-plasma treatment, respectively. Subthreshold swing (SS) can be extracted to be 281 mV/dec, 182 mV/dec, 240 mV/dec, and 145 mV/dec for the HfO_2, NH_3-HfO_2, Al_2O_3/HfO_2, and NH_3-Al_2O_3/HfO_2 samples, respectively. Obviously, the NH_3-plasma-treated samples exhibit a largely decreased SS, indicating an improved interface quality after the NH_3-plasma treatment. The interface-state density (D_{it}) between MoS_2 and the gate dielectric can be calculated by the following equations:[34]

$$SS = \ln 10 \times \frac{kT}{q} \times \left(\frac{C_{ox} + C_{it}}{C_{ox}}\right), \tag{3}$$

$$D_{it} = \frac{C_{it}}{q^2}, \tag{4}$$

where k is Boltzmann's constant and C_{it} is the interface trap capacitance per unit area. According to the SS and C_{ox} extracted for each sample above, D_{it} can be found to be 1.1×10^{13} $eV^{-1}\cdot cm^{-2}$, 8.0×10^{12} $eV^{-1}\cdot cm^{-2}$, 8.4×10^{12} $eV^{-1}\cdot cm^{-2}$, and 5×10^{12} $eV^{-1}\cdot cm^{-2}$ for the HfO_2, NH_3-HfO_2, Al_2O_3/HfO_2, and NH_3-Al_2O_3/HfO_2 samples, respectively, with the smallest D_{it} for the NH_3-Al_2O_3/HfO_2 sample.

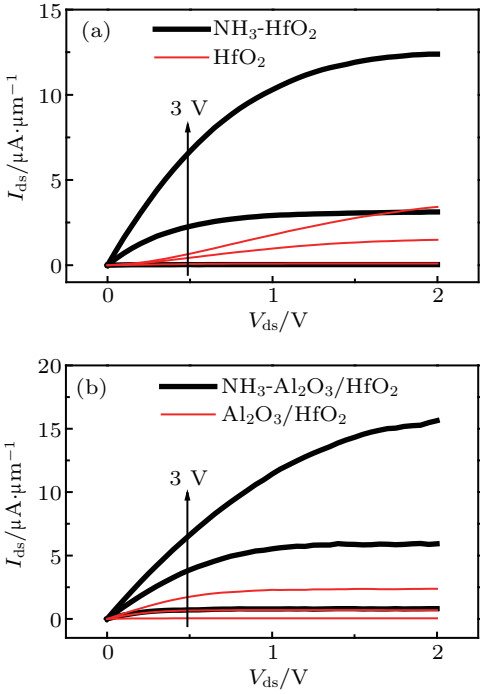


Fig. 3. Output characteristics of the MoS_2 transistors with or without NH_3-plasma treatment on (a) HfO_2 gate dielectric and (b) Al_2O_3/HfO_2 stack gate dielectric. V_{gs} increases from 1 V to 3 V in steps of 1 V.

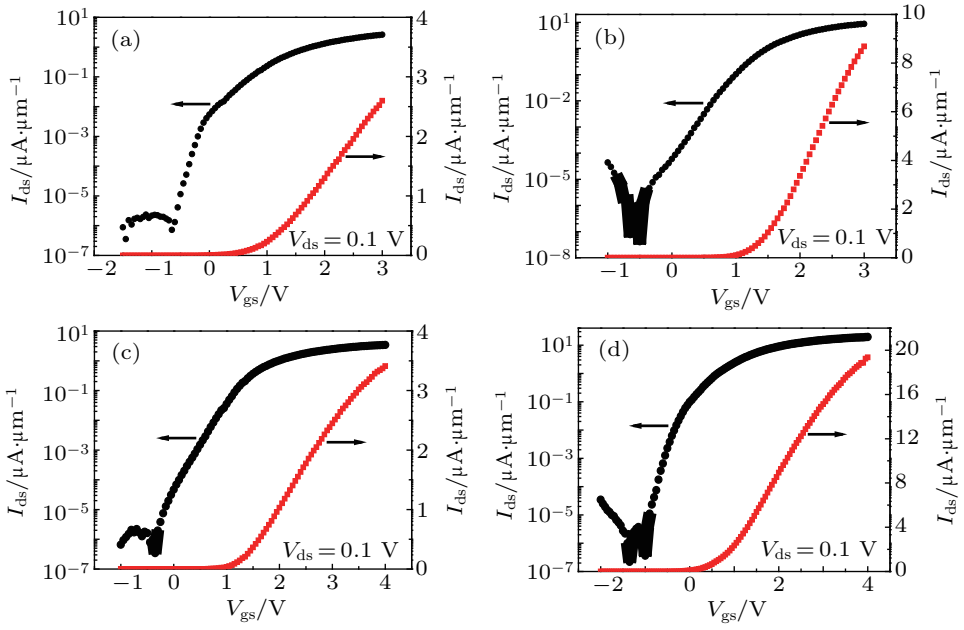


Fig. 4. Transfer characteristic in semi-logarithmic and linear scales for (a) HfO_2 sample, (b) NH_3-HfO_2 sample, (c) Al_2O_3/HfO_2 sample, and (d) NH_3-Al_2O_3/HfO_2 sample.

From the transfer curves in the linear region with $V_{ds} = 0.1$ V in Fig. 4, the electron mobility can be extracted using

$$\mu = \frac{\Delta I_{ds}}{\Delta V_{ds}} \times \frac{L}{W} \times \frac{1}{C_{ox}} \times \frac{1}{V_{ds}}. \quad (5)$$

The peak mobility for the four groups of transistors is found to be 6.33 $cm^2/V{\cdot}s$ (HfO_2 sample), 19.22 $cm^2/V{\cdot}s$ (NH_3-HfO_2 sample), 8.99 $cm^2/V{\cdot}s$ (Al_2O_3/HfO_2 sample), and 26.51 $cm^2/V{\cdot}s$ (NH_3-Al_2O_3/HfO_2 sample). The largely enhanced μ is obtained for the transistors with the NH_3-plasma treatment, which can be explained as follows. 1) The N atoms produced by the NH_3 decomposition can be incorporated into the high-k gate dielectric to repair the oxygen vacancies, reducing the defects in the gate dielectric and thus Coulomb scattering on the channel carriers. 2) NH_3 plasma can passivate the surface of the gate dielectric to reduce the dangling bonds and thus the surface roughness as shown in Fig. 5. The roughness (root-mean-square, an average value measured at four points for two samples) of the HfO_2 and Al_2O_3/HfO_2 before the NH_3-plasma treatment is 0.88 nm and 0.54 nm, respectively, which is decreased to 0.63 nm and 0.37 nm after the NH_3-plasma treatment. For comparison, the above two dielectrics were also thermally treated under the same temperature (300 °C) without using NH_3 plasma, and the resulted roughness is 0.80 nm and 0.49 nm, respectively, as shown in Figs. 5(c) and 5(f), indicating that the plasma treatment rather than temperature is the main reason for the roughness reduction, which is similar to the results in Ref. [35]. The smooth surface of gate dielectrics is conducive to carrier transport due to weakened surface roughness scattering. 3) Last but not least, the interfacial Coulomb scattering is effectively suppressed due to the superior interface quality between the MoS_2 channel and Al_2O_3 buffer layer, especially for the NH_3-plasma treated Al_2O_3/HfO_2 sample, since NH_4 functional groups may also exist on the surface of the NH_3-plasma treated dielectrics, which would highly increase the surface hydrophilicity, thus improving the contact status between MoS_2 and the dielectric surface (a possible mechanism for better performance). It is expected that the I_{ds}–V_{ds} characteristics of the MoS_2 FETs could be further improved by fabricating top-gate MoS_2 FET,[19] adding encapsulation layer,[36] or functionalization of MoS_2 surface, e.g., using sulfide treatment.[37]

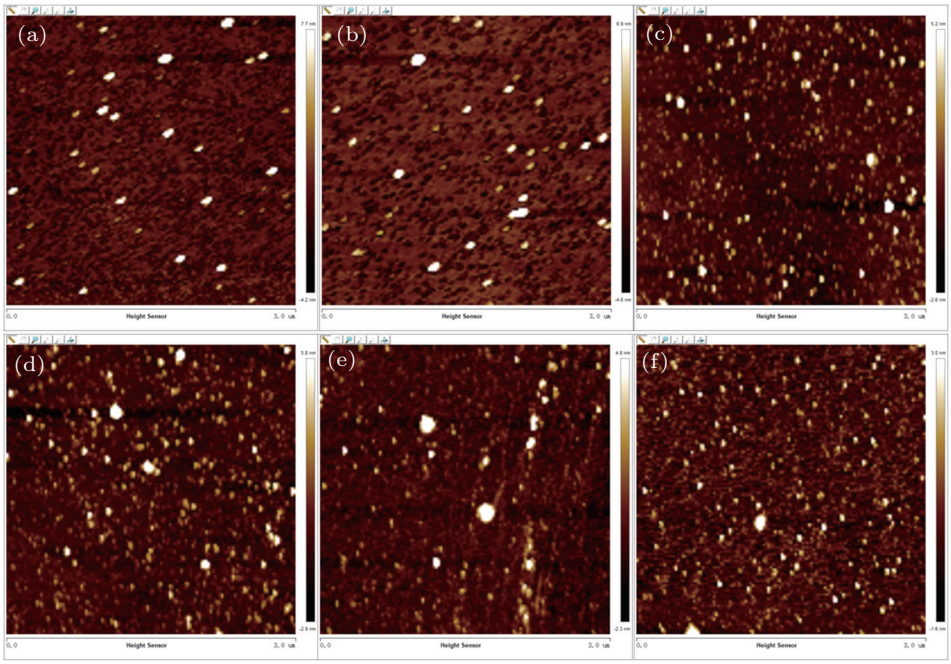


Fig. 5. Surface topography of gate dielectrics for (a) HfO_2 sample, (b) NH_3-HfO_2 sample, (c) only thermally-annealing HfO_2 sample, (d) Al_2O_3/HfO_2 sample, (d) NH_3-Al_2O_3/HfO_2 sample, and (f) only thermally-annealing Al_2O_3/HfO_2 sample.

Figure 6 shows the transfer characteristic curves in linear scale and the hysteresis behavior of the transistors with or without NH_3-plasma treatment. According to the transfer curve, the threshold voltage (V_{th}) can be calculated to be 1.19 V for the NH_3-HfO_2 sample and 0.89 V for the NH_3-Al_2O_3/HfO_2 sample, which are larger than their counterparts without NH_3-plasma treatment (0.54 V for the HfO_2 sample and 0.76 V for the Al_2O_3/HfO_2 sample). The increase of V_{th} after the NH_3-plasma treatment is mainly attributed to the decrease of the oxygen vacancies in the gate dielectrics and thus the negatively-charged interfacial states become dominant, decreasing ever depleting the electrons induced in the MoS_2 channel and giving rise to a larger V_{th}. In addition, the transistors with NH_3-plasma treatment have smaller hysteresis (0.3 V for the NH_3-HfO_2 sample and 0.2 V for the NH_3-Al_2O_3/HfO_2 sample) as compared with the transistors without NH_3-plasma treatment (0.33 V for the HfO_2 sample and 0.31 V for the Al_2O_3/HfO_2 sample). The alleviated hystere-

sis can also be attributed to the reduced trap charges in the gate dielectrics and the improved interface quality by the NH_3-plasma treatment.[17]

The electrical properties of the HfO_2 and Al_2O_3/HfO_2 back-gate MoS_2 transistors with and without NH_3-plasma treatment are summarized in Table 2. Because the NH_3-plasma treatment can decrease the oxygen vacancies in the gate dielectrics and surface roughness, and Al_2O_3 as the buffer layer has a good interface quality with MoS_2, the back-gate MoS_2 transistor with the stacked gate dielectric of Al_2O_3/HfO_2 plus NH_3-plasma treatment exhibits excellent electrical performances.

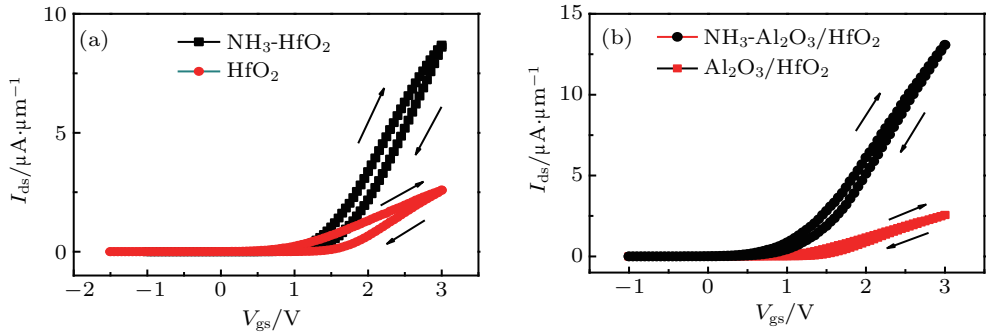


Fig. 6. Transfer characteristic in linear scale for (a) HfO_2 and NH_3-HfO_2 samples, (b) Al_2O_3/HfO_2 and NH_3-Al_2O_3/HfO_2 samples.

Table 2. Electrical properties of HfO_2 and Al_2O_3/HfO_2 back-gate MoS_2 transistors with and without NH_3-plasma treatment.

Sample	unit	HfO_2	NH_3-HfO_2	Al_2O_3/HfO_2	NH_3-Al_2O_3/HfO_2
μ	$cm^2/V{\cdot}s$	6.33	19.22	8.99	26.51
I_{ds} ($V_{gs}=3$ V, $V_{ds}=2$ V)	μA/μm	2.4	12.4	3.4	15.6
SS	mV/dec	281	182	240	145
I_{on}/I_{off}		3.70×10^6	1.30×10^7	7.32×10^6	1.53×10^7
D_{it}	$eV^{-1}{\cdot}cm^{-2}$	1.1×10^{13}	8.0×10^{12}	8.4×10^{12}	5.0×10^{12}
Hysteresis	V	0.33	0.30	0.31	0.2
V_{th}	V	0.54	1.19	0.76	0.89

4. Conclusions

In summary, the back-gate MoS_2 transistors with HfO_2 or Al_2O_3/HfO_2 as gate dielectric have been fabricated and effects of NH_3-plasma treatment on the device performances are investigated by measuring the I–V curves of the transistors and high-frequency C–V curves of the relevant MOS capacitors. The reduction of the trap charges and the positive shift of the flat-band voltage in the MOS capacitors imply the decrease of oxygen vacancies in the gate dielectrics after the NH_3-plasma treatment. The Al_2O_3/HfO_2 back-gate MoS_2 transistor with NH_3-plasma treatment shows the best electrical performances with high on–off current ratio of 1.53×10^7, higher field-effect mobility of 26.51 $cm^2/V{\cdot}s$, and lower subthreshold swing of 145 mV/dec. The involved mechanisms are mainly attributed to the repair of oxygen vacancies in the gate dielectric by the NH_3-plasma treatment and the passivation of dangling bonds on the dielectric surface, which reduces the defects in the gate dielectric and at the dielectric/MoS_2 interface. In addition, the addition of the Al_2O_3 buffer layer is also conducive to the improvement of the interface quality between MoS_2 and the gate dielectrics. Therefore, the stacked gate dielectric of Al_2O_3/HfO_2 plus NH_3-plasma treatment is a potential way to prepare high-performance MoS_2 transistors.

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