ISSN 1674-1056
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Citation: Chin. Phys. B . 2019, 28(12): 127201 . **doi:** 10.1088/1674-1056/ab4e89
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Ultra-high voltage 4H-SiC gate turn-off thyristor for low switching time*

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(Received 26 July 2019; revised manuscript received 27 September 2019; published online 22 November 2019)

An ultra-high voltage 4H-silicon carbide (SiC) gate turn-off (GTO) thyristor for low switching time is proposed and analyzed by numerical simulation. It features a double epitaxial p-base in which an extra electrical field is induced to enhance the transportation of the electrons in the thin p-base and reduce recombination. As a result, the turn-on characteristics are improved. What is more, to obtain a low turn-off loss, an alternating p^+/n^+ region formed in the backside acts as the anode in the GTO thyristor. Consequently, another path formed by the reverse-biased n^+–p junction accelerates the fast removal of excess electrons during turn-off. This work demonstrates that the turn-on time and turn-off time of the new structure are reduced to 37 ns and 783.1 ns, respectively, under a bus voltage of 8000 V and load current of 100 A/cm^2.

Keywords: 4H-SiC, gate turn-off (GTO) thyristor, turn-on, turn-off

PACS: 72.80.Ey, 73.40.Kp, 85.30.De, 85.30.Rs **DOI:** 10.1088/1674-1056/ab4e89

1. Introduction

In recent years, global demand of high voltage power semiconductor devices has been increasing in many industrial fields. In particular, high voltage gate turn-off (GTO) thyristor based on SiC has rapidly developed in simulations and experiments for being used as the ultra-high voltage direct current (UHVDC) converters. The SiC GTO thyristors can withstand higher blocking voltage, operate at higher junction temperature and have faster switching speed than Si thyristor,[1,2] because SiC material has characteristics of wide bandgap, high breakdown electric field, high thermal conductivity, and radiation-resistance.[3,4] Currently, the asymmetrical 22-kV 4H-SiC GTO thyristor with a thickness of 160-μm p^- drift layer is reported by Cree, Inc.[5] In fact, the development of SiC GTO thyristor with n-type drift layer is ahead of that of SiC GTO thyristor with p-type drift layer. Owing to the limitation of technology level, the SiC GTO thyristors with n-type thyristor use p-type SiC substrates that will induce a high resistance connected in series with the devices. Hence, the SiC GTO thyristor with p-type drift layer has been reported and investigated most during the past three decades. However, in 2015, the 27-kV/20-A 4H-SiC IGBTs with n-type drift layer was fabricated successfully on an n-type substrate and subsequently the n^+ substrate was removed by mechanical grinding or chemical mechanical polishing (CMP).[6] Additionally, in 2017, a low cost substrate removal process was developed commercially to obtain lightly doped free standing epitaxial SiC wafers with atomically flat surfaces on both Si- and C-faces. Using this process, a 350-μm-thick n^+-SiC substrate has been successfully removed to fabricate 180-μm–250-μm-thick 4-inch-sized (1 inch = 2.54 cm) n-SiC epitaxial free standing wafers by electrochemical etching process.[7] Hence, the fabrication of the SiC thyristors with thick n-type drift layer is feasible. Besides, n-type GTO thyristors have a high upper transistor gain α_{NPN} (~ 0.95) due to the strong electron injection from the upper n^+ emitter. What is more, the n-type GTO thyristors have a small lower transistor gain α_{PNP} (~ 0.05–0.2) caused by the low hole injection from the bottom p^+ emitter.[8] Thus, the turn-on and turn-off characteristics of n-type GTO thyristor are ferior to those of p-type GTO thyristor.

In our previous work, a double epitaxial n-base in p-type SiC thyristors[9] is induced to reduce the turn-on time. But unfortunately, the turn-off time of the thyristor is increased. In view of this, we consult the method to gain low turn-off loss in Si thyristor by the anode- or cathode-shorts[10,11] to improve the turn-off characteristics in SiC thyristors.

In this paper, an ultra-high voltage 4H-SiC GTO thyristor with n^- drift layer for low switching time is proposed and demonstrated by numerical simulations, which shows excellent turn-on and turn-off performance.

2. Device structure and simulation setup

Figure 1(a) shows the schematic cross section of the proposed n-type 4H-SiC GTO thyristor. It features a heavily doped p region and a slightly doped p^- region in narrow p-base. And the double epitaxial p-base could be grown by the modified epitaxial process.[12] Furthermore, an alternating n^+

*Project supported by the National Natural Science Foundation of China (Grant No. 51677149).

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and p^+ emitter on the anode side to improve the turn-off characteristics. Here, W represents the width of the p^+ region and is 12.5 μm. During turn-on, the high-low doped p-base introduces an extra electrical field to enhance the transit of electrons by drift action, and thus reducing the recombination. Hence, the turn-on speeds up. In the turn-off process, another path will form to force the extra electrons in n^- drift layer and n buffer layer to be extracted, and thus improving the turn-off characteristics. It can be observed that the p emitter is induced in the proposed n-type GTO thyristor to ensure a desirable injection of holes. As a result, the device is still in the on-state when the gate-triggered-on current is removed.

Figure 1(b) shows the conventional p-type 4H-SiC GTO thyristor with a 160-μm-thick p^- drift layer and 2-μm-thick p^+ buffer layer. And the design and fabrication details of the p-type SiC GTO thyristor can be seen in Ref. [13]. Note that the concentration and thickness of n^-/p^- drift and n^+/p^+ buffer layers are chosen according to Refs. [5] and [14] which can support 20-kV forward blocking voltage.

Figure 1(c) shows the fabrication process for the proposed SiC GTO thyristor with an n^- drift layer.

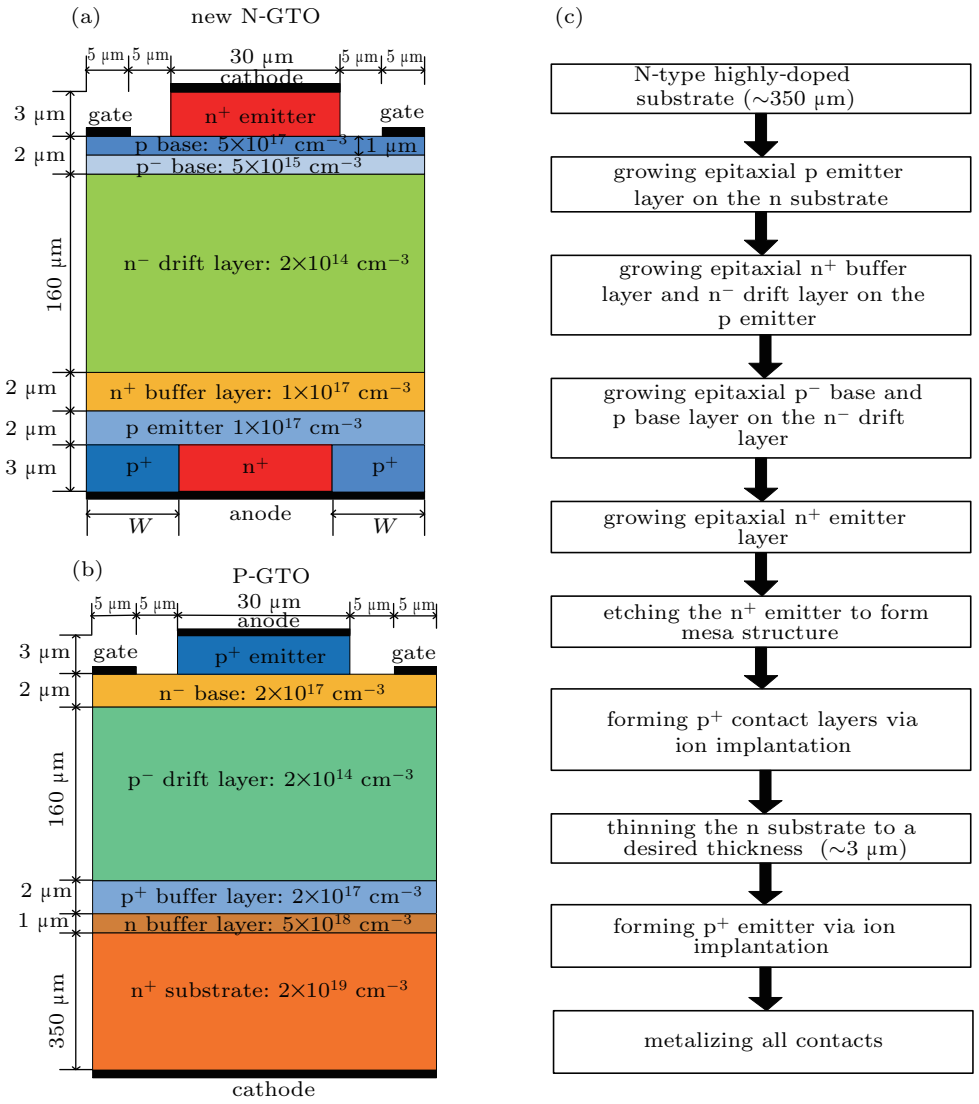


Fig. 1. Cross-sectional schematic diagram of (a) proposed 4H-SiC n-GTO thyristor, (b) conventional p-GTO thyristor, and (c) simple fabrication process of proposed n-GTO thyristor.

To investigate the static and dynamic characteristics of the developed n-type GTO thyristor, two-dimensional device-level simulation software Sentaurus-TCAD[15] is used. In simulations, some models must be adopted, including incomplete ionization,[16] band-gap narrowing,[17] Auger recombination,[18] electron–hole scattering,[19] doping, temperature, and field-dependent mobility models,[20] Shockley–Read–Hall recombination with the Scharfetter.[21] For impact-ionization modeling, the anisotropic model is used for the SiC-based GTO thyristor.[22] In the highly-doped p^+/n^+ emitter layers, the carrier lifetime is given by the semi-empirical formula[23,24]

$$\tau_{n0,p0(\text{emitter})} = \frac{\tau_{n0,p0}(\text{drift})}{1+[(N/N_n)]^{\alpha}}, \quad (1)$$

where $\tau_{n,p}$(drift) are the values of the parameters τ_n and τ_{p0} in the thick n^-/p^- drift layer, N is the doping concentration for the heavily doped emitters, and N_n and α are the fitting parameters, $N_n = 7\times10^{17}$ cm^{-3}, and $\alpha = 1$. Table 1 shows several important physical models and their parameters in this simulation. Moreover, all simulations are carried out by using Fermi–Dirac statistics. The temperature involved in all simulations is assumed to be room temperature (300 K). Moreover, in the simulation, the minority carrier lifetime in the drift layer and buffer layer are set to be 2.0 μs and 1.5 μs, respectively.[23]

Table 1. Physical models and parameters.

Model name	Models	Parameters
Incomplete ionization of impurities	$N_D^+ = N_D/[1+g_D(n/n_i)]$, $n_i = N_c\exp(-\Delta E_D/K_BT)$ for $N_D < N_{D,crit}$ $\Delta E_D = E_C - E_D$	$\Delta E_D = 70$ meV, $g_D = 2$ $N_c(300) = 1.689\times10^{19}$ cm^{-3}
	$N_A^- = N_A/[1+g_A(P/P_i)]$, $P_i = N_V\exp(-\Delta E_A/K_BT)$ for $N_A < N_{A,crit}$ $\Delta E_A = E_A - E_V$	$\Delta E_A = 191$ meV, $g_V = 4$ $N_V(300) = 2.494\times10^{19}$ cm^{-3}
Auger	$R^A = (C_n n + C_p p)(np - n_i^2)$	$C_n = 5\times10^{-31}$ cm^6·s^{-1} $C_p = 2\times10^{-31}$ cm^6·s^{-1}
SRH	$\tau_{n,p(drift)} = \tau_{max}(T/300)^{\beta}/\{1+[(N_D+N_A)/N_{ref}]^{\gamma}\}$	$\tau_{max} = 2.0$ μs, $\beta = 1.72$ $N_{ref} = 3\times10^{17}$ cm^{-3}, $\gamma = 0.3$
Mobility	$\mu_n = \mu_{max}(T/300)^{-\alpha}/\{1+[(N_D+N_A)/N_{ref}]^{\gamma}\}$	$\mu_{max} = 950$ cm^2/s, $\alpha = 2.4$, $\gamma = 0.61$, $N_{ref} = 1.94\times10^{17}$ cm^{-3}
	$\mu_p = \mu_{max}(T/300)^{-\alpha}/\{1+[(N_D+N_A)/N_{ref}]^{\gamma}\}$	$\mu_{max} = 124$ cm^2/s, $\alpha = 2.15$, $\gamma = 0.34$, $N_{ref} = 1.76\times10^{17}$ cm^{-3}
Impact ionization	$\alpha = \alpha_0\exp[-((E_c/E)^m)]$	$\alpha_0 = 1.69\times10^6$ cm^{-1} $E_C = 9.69\times10^6$ V/cm, $m = 1.6$
	$\beta = \beta_0\exp[-((E_c/E)^m)]$	$\beta_0 = 3.32\times10^6$ cm^{-1} $E_C = 1.07\times10^6$ V/cm, $m = 1.1$
Carrier-carrier scattering	$\mu_{eh} = [D(T/300)^{3/2}/\sqrt{np}][\ln(1+F(T/300)^2(np)^{-1/3})]^{-1}$	$D = 6.9000\times10^{20}$ (cm·V·s)$^{-1}$ $F = 7.4520\times10^{13}$ cm^{-2}

3. Results and discussion

In this section, we will investigate the static and dynamic characteristics for the SiC GTO thyristors comparatively. The results and analyses are presented as follows. Also the device active area is taken to be 1 cm^2 for simplicity. The test circuit as shown in Fig. 2 is used to investigate the dynamic performance of the structures. The power is supplied by the voltage source $V_S = 8000$ V, V_G and R_G form the gate drive circuits, and the values of the inductor L and the load resistance R_L are fixed at 5 mH and 80 Ω·cm^2, respectively, therefore the load current density is about 100 A/cm^2. The free wheeling diode D is used to reduce the voltage overshoot across the GTO thyristor. The turn-off snubber circuit consisting of R_s, C_s, and D_s is applied to minimize the risk of dV/dt turn-on.[25]

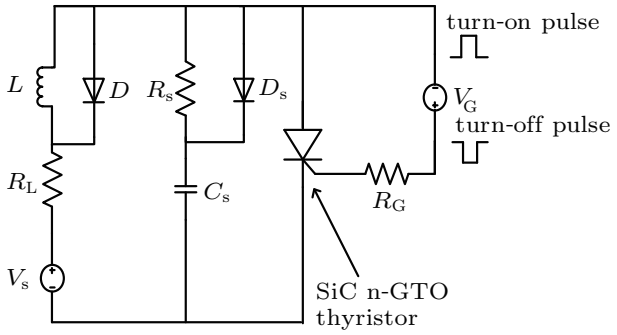


Fig. 2. Test circuit of dynamic characteristics of 4H-SiC GTO thyristor.

Figures 3 and 4 show the switching waveforms of the n-type GTO and p-type GTO thyristor, respectively. In the simulation, both the turn-on gain and turn-off gain are approximately 3. Based on the switching waveforms, turn-on time and turn-off time are extracted from Figs. 3 and 4. Note that the turn-on time of 4H-SiC thyristor contains two parts, the delay time (t_d) and the rise time (t_r). The former t_d is defined as the time interval from the 10%I_g-on (I_g-on is gate-triggered-on current) to the 90%V_{AK} (V_{AK} is the voltage between the anode and cathode), while the latter t_r is the time interval that V_{AK} drops from 90%V_{AK} to 10%V_{AK}. The turn-off time is determined by storage time (t_s), fall time (t_f), and tail time (t_t). Here, t_s is a time interval that starts from 10%I_g-off (I_g-off is gate-triggered-off current), the on-state cathode current I_T (I_T is on-state current) drops to 90%I_T; t_f is a period of time that the on-state current drops from 90%I_T to 10%I_T; and t_t time interval is set to be the value as 10%I_T drops to 25%I_{tail} (I_{tail} is tail current).

Results show that comparing with the p-type GTO, the turn-on time and turn-off time of the n-type GTO decrease extremely, which can be explained by the higher injection efficiency of the top n^+–p junction and the smaller transistor current gain of the bottom p–n–p transistor of the n-type GTO than those of p-type GTO. Hence, the switching performance of the n-type GTO is superior to p-type GTO.

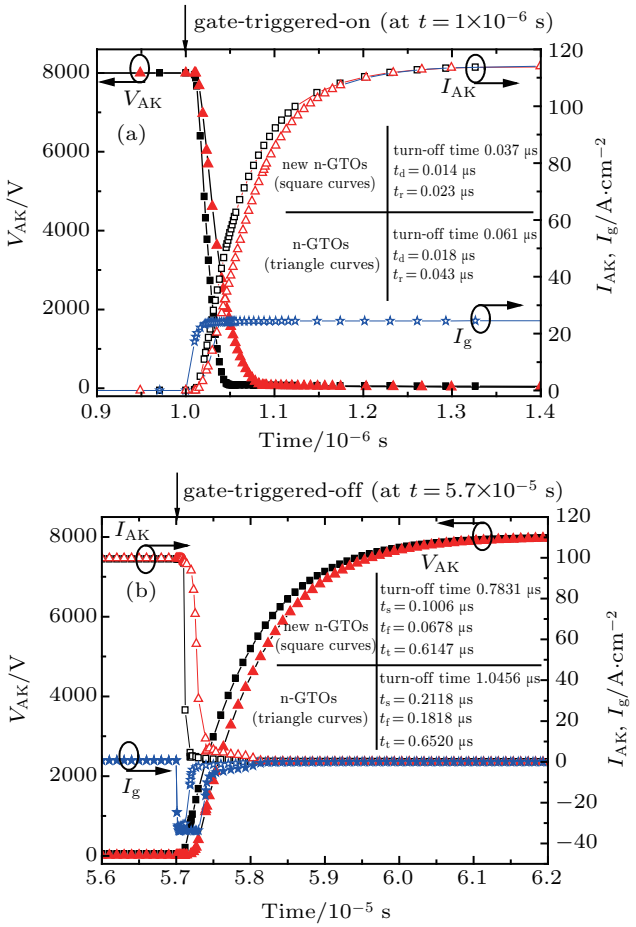


Fig. 3. Switching waveforms of proposed n-GTO and n-GTO thyristors for (a) turn-on case and (b) turn-off case.

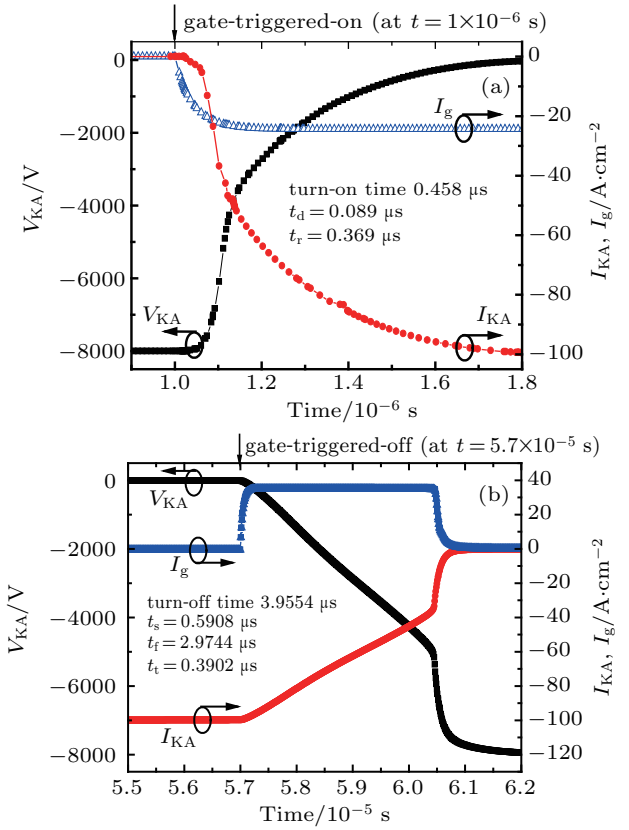


Fig. 4. Switching waveforms of p-GTO thyristors for (a) turn-on case and (b) turn-off case.

Besides the dynamic characteristics of the structures, the forward on-state characteristics of the developed SiC GTO thyristors are also presented as follows.

Figure 5(a) shows the forward J–V characteristics of the structures shown in Fig. 1. It can be seen that the on-state characteristic of the proposed n-type GTO thyristor is deteriorated slightly. Based on the forward J–V characteristics, the forward voltage drop (at $J_{AK} = 100$ A/cm^2) of the new n-type GTO, n-type GTO, and p-type GTO are approximately 4.61 V, 3.89 V, and 4.23 V, respectively. The forward voltage drop of the new structure is larger than that of n-type GTO thyristor. Owing to the n^+ region instead of the partial backside p^+ region leads the injection efficiency of the holes to decrease, and thus weakening the conductivity modulation in the n^- drift layer during on-state. Figure 5(b) shows the carrier density distribution in thick drift layer during on-state. Obviously, the hole density in new n-GTO is lower than that in conventional n-GTO thyristor.

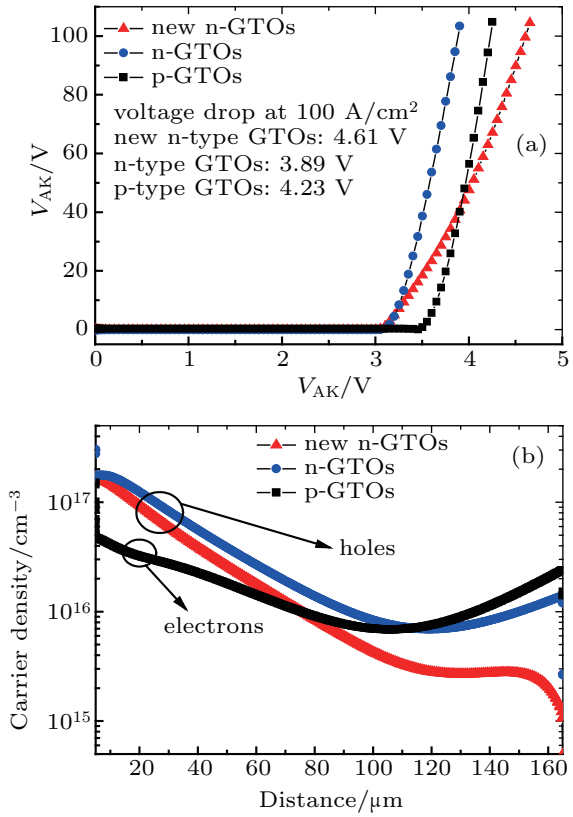


Fig. 5. (a) Forward J–V characteristics of structures, and (b) distribution of holes/electrons in n/p drift layer at on-state current density of 100 A/cm^2.

The comparison between the dynamic performance and the static performance given above shows that the switching characteristics of the proposed 4H-SiC n-type GTO thyristor is improved significantly at the sacrifice of a little on-state performance. Subsequently, the turn-on and turn-off mechanisms of the new n-type GTO thyritsor are investigated in detail.

3.1. Analysis of turn-on mechanism

As can be seen from the results of Fig. 3(a), the turn-on time is substantially reduced to 37 ns in the new 4H-SiC n-type GTO thyristor. To further understand the turn-on process for new n-type GTO thyristor, figure 6 shows the minority carrier (electron/hole) density in thin p-base/n-base of the structure as shown in Fig. 1 in turn-on process. First, the minority electron density in thin p-base of n-type GTO thyristor is higher than the hole density in thin n-base of p-type GTO thyristor, which contributes to the larger injection efficiency of the upper n^+–p than that of p^+–n junction, owing to the fact that the highly doped p^+ emitter is not fully ionized at room temperature. Second, for the n-type GTO thyristor, the electron density in p-base of the new structure is higher than that for conventional n-type GTO thyristor in the turn-on process. In the new structure, the thin p-base consists of a heavily doped p region and a slightly doped p^- region. As a result, an extra electrical field is induced in p-base, consequently, accelerating the transportation of the electron in p-base and therefore reducing the recombination in the turn-on process.

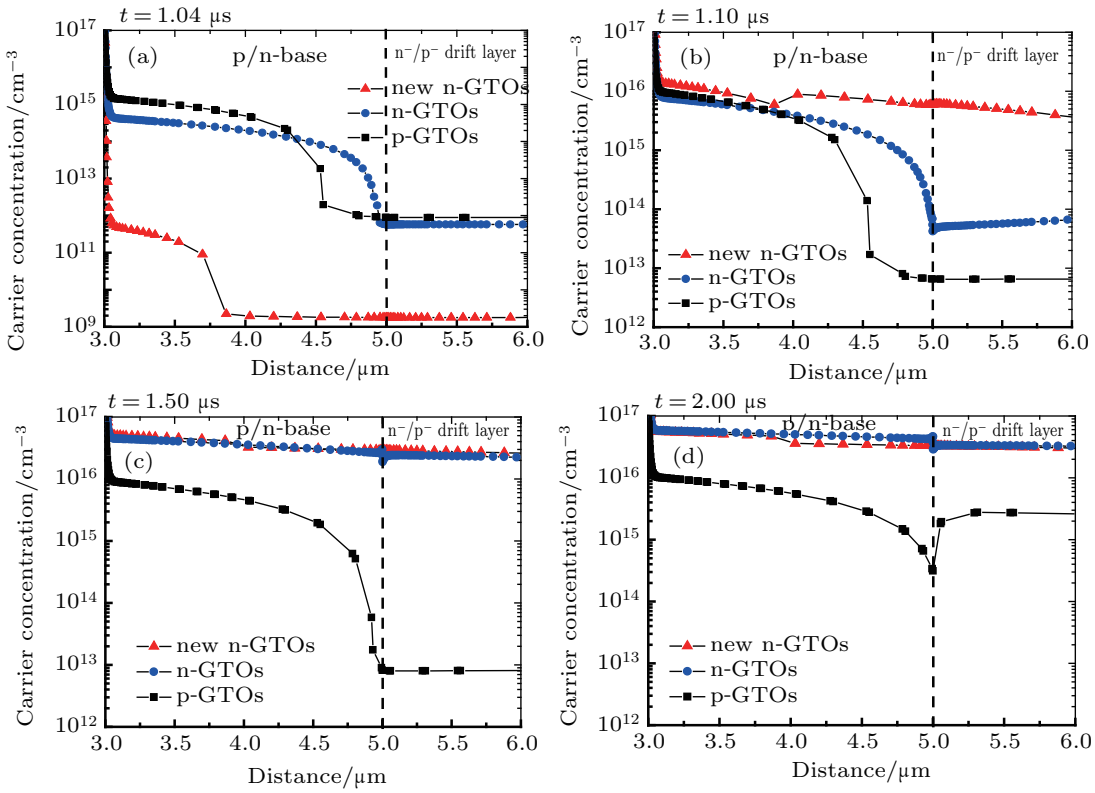


Fig. 6. Plots of minority carrier (electron/hole) density *versus* distance in thin p-base/n-base of SiC GTO thyristors in turn-on process.

Figure 7 shows the recombination rate in thin p-base of the two n-type GTO thyristors during the turn-on state. Obviously, the recombination rate declines in new structure. Therefore, the turn-on time of the proposed new 4H-SiC n-type GTO thyristor is reduced significantly.

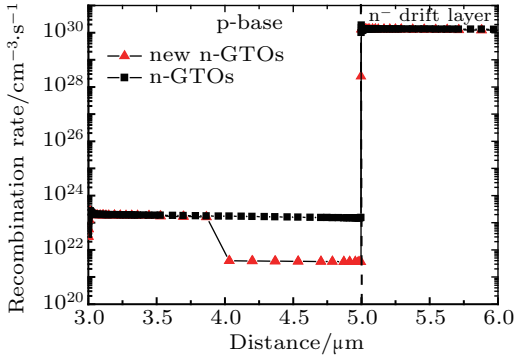


Fig. 7. Recombination rate *versus* distance of two n-type GTO thyristors during turn-on state.

3.2. Analysis of turn-off mechanism

The dynamic turn-off characteristics of the structures, which are obtained with a 33-A/cm^2 absolute value of gate current (the turn-off gain $\beta_{\rm off} \approx 3$), are shown in Figs. 3(b) and 4(b). The turn-off times of these structures are summarized in the illustration. Primarily, the much faster turn-off speed of the n-type GTO thyristor than that of the p-type GTO thyristor mainly results from the lower current gain of p–n–p transistor in the n-type GTO thyristor than that of n–p–n transistor in p-type GTO thyristor. As a result, the excellent turn-off performance of the n-type GTO thyristor is improved in storage time, especially fall time. Besides, the turn-off time of the proposed n-type GTO thyristor is approximately 783.1 ns, which is smaller than that of conventional n-type GTO thyristor (1045.6 ns).

Figure 8 presents the electron/hole density distribution in

thick p^-/n^- drift layer of the p-type and n-type GTO thyristors during turn-off state. Due to the low transistor current gain of p–n–p transistor in n-type GTO thyristor, the extraction of the minority carriers is faster than that of the p-type GTO thyristor. Furthermore, comparing with the conventional n-type GTO thyristor, the hole density of n^- drift layer in the proposed structure is low at the same turn-off time, which results from the fact that the new structure has two paths to extracting the extra carriers. One is a conventional way to recombination through $p–p^+$ junction, and the other is a novel path to sweeping out the electrons rapidly through the reverse biased $p–n^+$ junction during turn-off state. Figure 9(a) shows the distribution of potential and electrical field on the back-side of the new n-type GTO thyristor during turn-off state, indicating that the potential drop is about 2.9 V and bottom $n^+–p$ junction is reverse biased. Consequently, a high electrical field is induced at the $p–n^+$ interface, which is expected to accelerate the extraction of excess electrons. Figure 9(b) shows the recombination rate on the back-side in the structure. It is indicated that the electrons/holes are extracted only by recombination in p-type and conventional n-type GTO thyristors, whereas the electrons are removed through recombination and swept out by the reverse biased $p–n^+$ junction in the new structure. Hence, the electron density of the new n-type GTO thyristor is lowest as shown in Fig. 10.

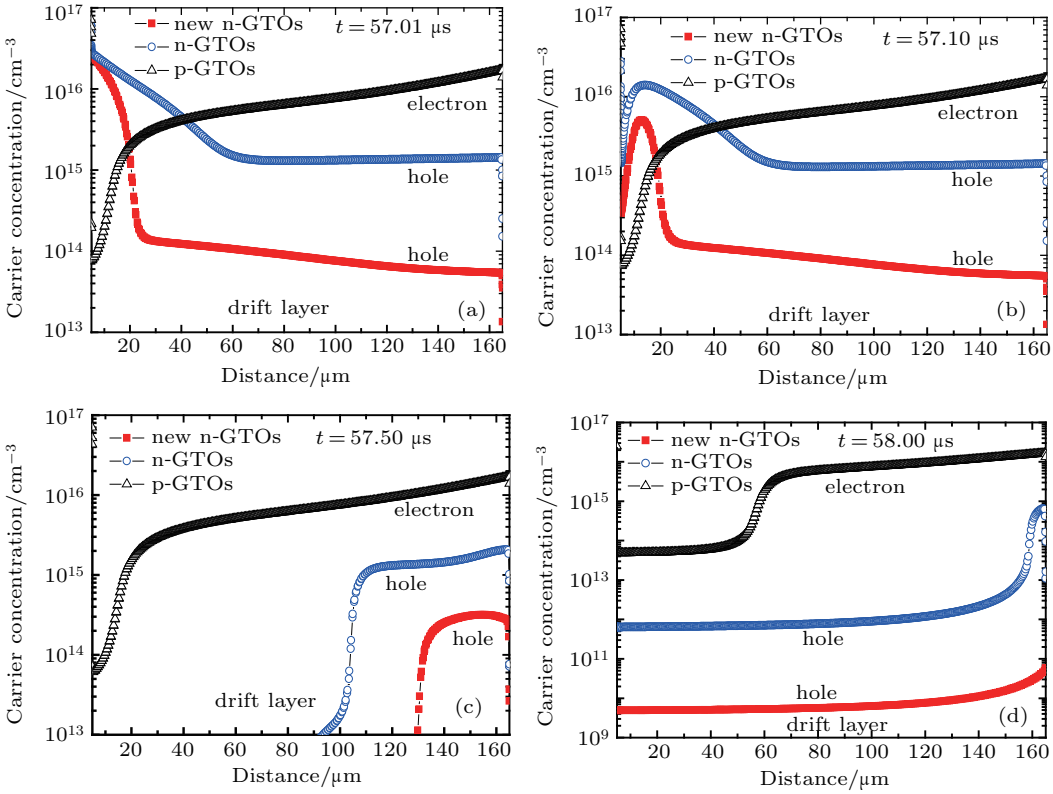


Fig. 8. Minority carrier concentration distributions at different times during turn-off state.

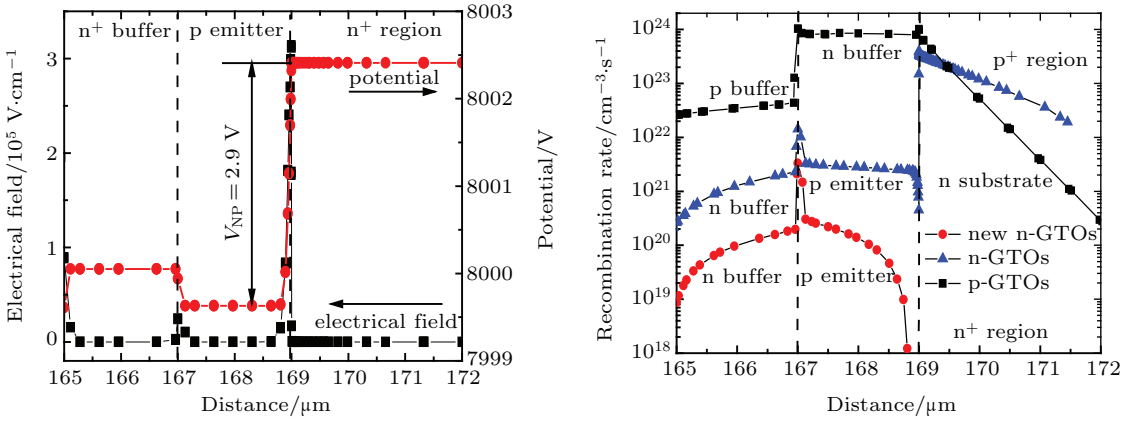


Fig. 9. (a) Electrical field distribution in new 4H-SiC GTO thyristor and (b) recombination rate distribution during turn-off state for different structures.

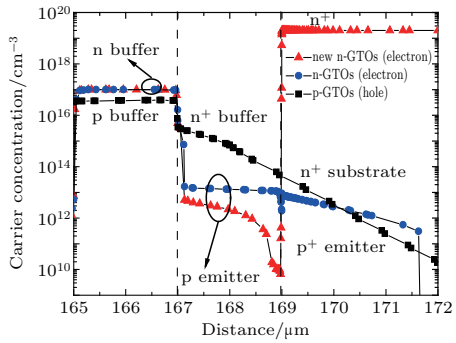


Fig. 10. Carrier density distributions during turn-off state for different structures.

Figure 11 shows the electron current density distribution on the anode-side during turn-off state in n-type GTO thyristor. It is confirmed that the extraction of the carriers in the proposed structure is faster than that in the conventional n-type GTO thyristor. What is more, for the proposed n-type GTO thyristor, the extraction of electrons from the side of the reverse biased p–n$^+$ junction becomes more and more obvious and dominant. Therefore, the turn-off speed is substantially faster than that of the conventional n-GTO thyristor and obtains a distinctly low turn-off loss.

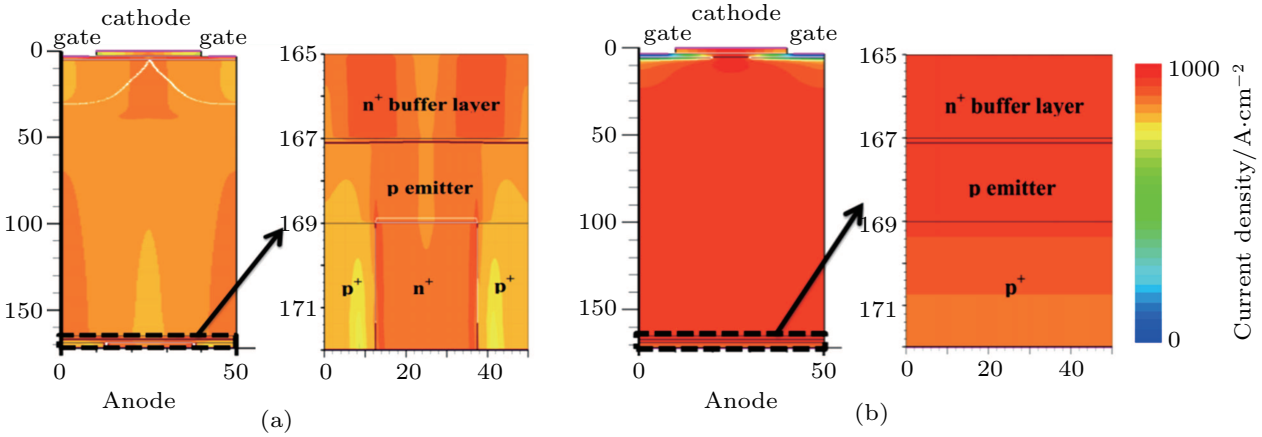


Fig. 11. Current density distribution during turn-off state in (a) new n-GTO thyristor and (b) conventional n-GTO thyristor.

4. Conclusions and perspectives

In this paper, a novel ultra-high voltage 4H-SiC GTO thyristor for low switching loss is presented. The results demonstrate that for the proposed 20-kV n-type 4H-SiC GTO thyristor, the turn-on time and turn-off time are reduced to 37 ns and 783.1 ns, respectively. During turn-on state, the extra electric field introduced by the high–low p–p$^-$ junction in the thin p-base enhances the transit of the electrons and reduces the recombination. During the turn-off state, the outstanding turn-off characteristics are attributed to the following two aspects. First, the extra carriers in an n$^-$ drift layer are less during the turn-on state in the new n-type GTO thyristor. Second, and most important thing of all, during the turn-off state, is that the bottom n$^+$–p junction is reverse-biased, which accelerates the extraction of electrons. As a result, the turn-on and turn-off characteristics of the proposed structure are improved significantly with a slight degradation of the forward voltage drop. The idea can be a promising solution for fast switching the ultra-high voltage SiC GTO thyristor.

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