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SPECIAL TOPIC — A celebration of the 100th birthday of Kun Huang

Charge trapping memory device based on the Ga_2O_3 films as trapping and blocking layer*

Bing Bai(白冰)[1,†], Hong Wang(王宏)[1,†], Yan Li(李岩)[1], Yunxia Hao(郝云霞)[1], Bo Zhang(张博)[1], Boping Wang(王博平)[1], Zihang Wang(王子航)[1], Hongqi Yang(杨红旗)[1], Qihang Gao(高启航)[1], Chao Lü(吕超)[2], Qingshun Zhang(张庆顺)[1,‡], and Xiaobing Yan(闫小兵)[1,3,§]

[1] *Key Laboratory of Optoelectronic Information Materials of Hebei Province, Key Laboratory of Digital Medical Engineering of Hebei Province, College of Electron and Information Engineering, Hebei University, Baoding* 071002, *China*

[2] *Department of Electrical and Computer Engineering, Southern Illinois University Carbondale, Carbondale, Illinois* 62901, *United States*

[3] *Department of Materials Science and Engineering, National University of Singapore, Singapore* 117576, *Singapore*

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We present a new charge trapping memory (CTM) device with the Au/Ga_2O_3/SiO_2/Si structure, which is fabricated by using the magnetron sputtering, high-temperature annealing, and vacuum evaporation techniques. Transmission electron microscopy diagrams show that the thickness of the SiO_2 tunneling layer can be controlled by the annealing temperature. When the devices are annealed at 760 °C, the measured *C*–*V* hysteresis curves exhibit a maximum 6 V memory window under a ±13 V sweeping voltage. In addition, a slight degradation of the device voltage and capacitance indicates the robust retention properties of flat-band voltage and high/low state capacitance. These distinctive advantages are attributed to oxygen vacancies and inter-diffusion layers, which play a critical role in the charge trapping process.

Keywords: charge trapping memory, SiO_2 tunneling layer, annealing temperature

PACS: 68.35.Fx, 85.25.Hv, 06.60.Ei, 21.10.Ft **DOI:** 10.1088/1674-1056/ab3e62

1. Introduction

Some new types of memory have attracted extensive attention from researchers.[1–3] In particular, charge trapping memory (CTM) is receiving more and more attention due to its strong charge trapping capability, good durability, and low program/erase voltages.[4–6] However, technology scaling is a major obstacle to improve the memory performance and capacity of modern CTMs.[7,8] As the size of the CTM device shrinks, the charge trapping efficiency decreases. In addition, as the charge tunnel breaks down due to thinner trapping or blocking layers, the trade-off between data retention and access time cannot be balanced,[9] and the crosstalk between adjacent floating gates is gradually increasing.[10] To address these challenges, scientists have developed a variety of new CTM devices. For example, the structures of ZrO_2/Al_2O_3/ZrO_2 and HfO_2/Al_2O_3/HfO_2 have outstanding performance due to their strong charge trapping capability and fast programming speed associated with high-*k* materials.[11–16] In addition, fast and high-density oxide materials for non-volatile memories have been studied for a long time because of their robust switching mechanisms and storage immunities to read disturbances.[19–23] There are also many studies on two-dimensional (e.g., WS_2, graphene, MoS_2) and oxide materials (e.g., HfO_2, Al_2O_3, ZrO_2) used for memory, which can improve the memory properties.[2,11–14,36] Moreover, one well-developed oxide layer as charge trapping and blocking layers has shown great potential in recent years.[24–26] Ga_2O_3 is a wide bandgap semiconductor material with numerous physical properties, such as electrical conductivity and luminescence, which is widely used in photodiodes, thin film electroluminescent devices, and ultraviolet detectors.[15–18]

In this study, we explored the Ga_2O_3 film as charge trapping and blocking layers in CTMs. Particularly, we studied the charge storage and data retention characteristics of CTMs based on an Au/Ga_2O_3/SiO_2/Si structure. Magnetron sputtering, high-temperature annealing, and vacuum evaporation techniques were adopted to prepare the device sam-

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†These authors contributed equally to this work.

‡Corresponding author. E-mail: 87086486@qq.com

§Corresponding author. E-mail: yanxiaobing@ime.ac.cn; xiaobing yan@126.com

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ples. Memory windows of the fabricated the Ga_2O_3 samples were measured after annealing at different temperatures. The largest memory window is found to correspond to an annealing temperature of 760 °C. Transmission electron microscopy (TEM) analysis shows that the thickness of the SiO_2 tunneling layer varies with the annealing temperature, indicating that the annealing temperature changes the charge storage capability. The measured long-term retention of flat-band voltage and high/low state capacitances also demonstrates that this proposed device has excellent retention characteristics as a charge trapping memory.

2. Method

A (100)-oriented p-type silicon was in turn immersed in deionized water, acetone, and alcohol. Next, it was placed in an ultrasonic cleaner for 5 min and then immersed in a diluted hydrogen fluoride solution (1%) for 90 s. Then, it was soaked in deionized water and placed in an ultrasonic cleaner for 5 min. A 70 nm-thick Ga_2O_3 film was sputtered on the Si substrate for 140 min under 3 Pa, 80 W, and Ar : $O_2 = 25 : 25$. Then, rapid high-temperature annealing was performed for 5 min at 600 °C, 680 °C, 760 °C, and 780 °C in the 35 sccm O_2 gas environment, respectively. Finally, Au electrodes with a thickness of 80 nm were grown by vacuum evaporation. After these device samples were fabricated, memory storage windows and high/low state capacitances for each annealing temperature were tested by the Keithley 4200 SCS. The relationship between the annealing temperature and the thickness of the SiO_2 tunneling layer was investigated using the TEM. Meanwhile, the x-ray photoelectron spectroscopy (XPS) of various etching depths was used to analyze the CTM memory mechanism.

3. Results and discussion

Figure 1(a) depicts the schematic view of an Au/Ga_2O_3/SiO_2/Si CTM structure. A 70 nm-thick Ga_2O_3 layer was grown on the p-type silicon substrate. Figure 1(b) plots the capacitance–voltage (C–V) curves of the samples tested with a 1 MHz gate voltage. The memory window ($\Delta V_{\rm fb}$) is defined as the flat band voltage ($V_{\rm fb}$) difference between programming and erasing states. As shown in Fig. 1(b), the memory window decreases after annealing at temperatures above 680 °C. The memory windows are about 1.6 V, 3 V, 4.8 V, and 1.5 V, respectively. At low-annealing temperatures, the charge trapping performance is poor due to the very thin SiO_2 layer between the Ga_2O_3 film and silicon substrate. Tests in high-frequency environments can easily create leaky channels and generate leakage currents. When the annealing temperatures are high, the SiO_2 film is very thick so charges hardly pass through the tunneling oxide layer, thus the Ga_2O_3 film captures fewer charges. On the other hand, when the device is annealed at a high temperature in a dry O_2 environment, the Ga_2O_3 film with a reduced oxygen vacancy concentration cannot provide an enough defect level for charge trapping.[26,27] Among these four annealing temperature choices, the 760 °C annealed devices exhibit the largest memory window because the Ga_2O_3/SiO_2 interface produces an inter-diffusion layer that enhances the charge trapping property. The thickness of this inter-diffusion layer is controlled by the annealing temperate.[9]

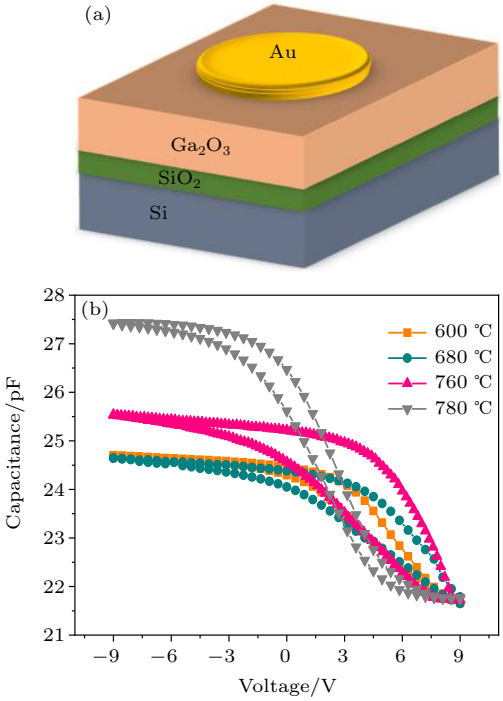


Fig. 1. (a) Schematic view of the Au/Ga_2O_3/SiO_2/Si structure, (b) C–V curves of the fabricated samples with different annealing temperatures.

The device annealed at 760 °C was selected and applied with different scanning gate voltages to measure the C–V curves. As shown in Fig. 2(a), the memory window increases with the rise of the scanning gate voltage. When the scanning voltage is ±13 V, the measured memory window is up to 6 V, which indicates a remarkable charge trapping capability. As the scanning voltage continues to rise, the resultant high electric fields increase the number of trapped electrons tunneling through the SiO_2 layer. Therefore, the memory storage window becomes even wider and finally gets saturated.[27,28] If the scanning gate voltage further increases, device breakdown will occur. The explanation for this phenomenon is briefly described as follows. Charges are more likely to pass through the tunneling oxide layer over a wider voltage range. Meanwhile, as the device leakage current becomes larger, the number of trapped charges is reduced, so the memory storage window is smaller.[27,28]

The planar charge trapping density per unit area ($N_{\rm t}$) is estimated as[29,30]

$$N_{\rm t} = \frac{C_{\rm ox}\Delta V_{\rm fb}}{qA}, \tag{1}$$

where C_{ox} is the capacitance of the memory devices in the accumulation region, A is the effective area (i.e., 1.256×10^{-4} cm^2) of the Au electrode, q stands for the electron charge, and ΔV_{fb} is the memory window of the device. At a working voltage range of ± 13 V, the planar density is about 7.6×10^{11} cm^{-2}.

Data retention property of the flat-band voltage is another important metric to characterize the memory performance. The device changes from a low capacitance state to a high capacitance state during a ± 13 V sweep. Then, a small area near the flat-band voltage is selected every 15 min for C–V scanning. This voltage range is not charged or trapped in the C–V measurements. Similarly, a voltage of -13 V to $+13$ V shifts the device from a high capacitance state to a low capacitance state. As shown in Fig. 2(b), the flat-band voltage decays slightly at the beginning of this test, and it remains stable after 10^4 s, indicating good long-term retention of the flat-band voltage.

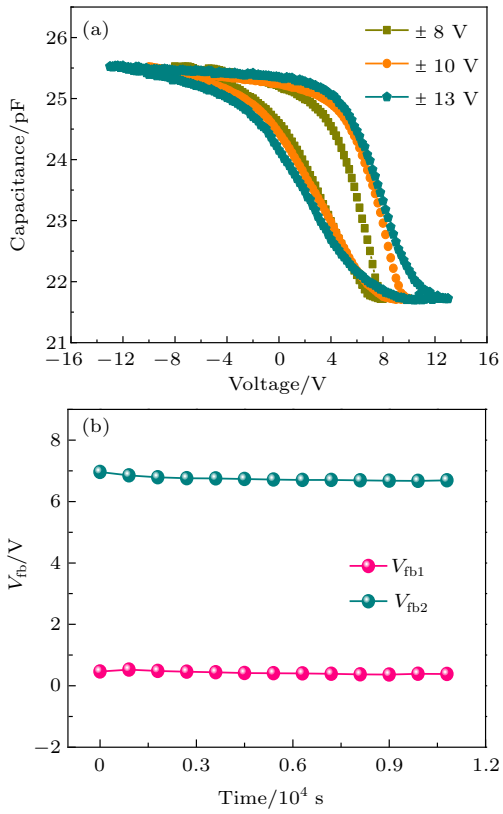


Fig. 2. (a) The C–V curves with different scan voltages and (b) the flat band voltage retention of the fabricated sample with 760 °C annealing.

In order to in-depth investigate the data retention property, the capacitance retention was also tested for the device annealed at different annealing temperatures. As shown in Fig. 3, the high/low state capacitances were tested using a scanning gate voltage of ± 13 V. The high (or low) capacitance was measured at a fixed voltage of -3 V (or 3 V) every 10 s. Obviously, figure 3(c) shows the optimal retention characteristics. After about 10^4 s of device testing, the degradation of high and low state capacitances is 1% and 1.7%, respectively, indicating great data retention capability of this proposed CTM device.

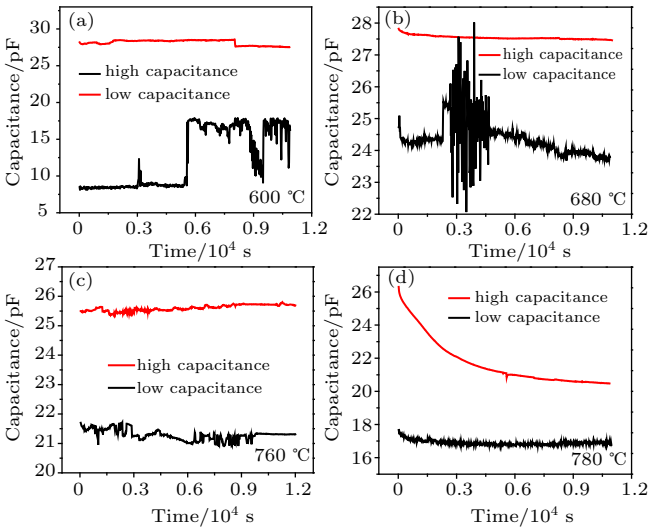


Fig. 3. Long-term retention measurement of the high/low state capacitances for CTM devices annealed at (a) 600 °C, (b) 680 °C, (c) 760 °C, and (d) 780 °C, respectively.

The CTM device based on the 760 °C annealing has such excellent performance, which is originated from oxygen vacancies and an inter-diffusion layer that improves the charge trapping capability.[9,35] To further confirm the memory mechanism, its microscopic characterization analysis was studied by TEM and XPS in detail. Figures 4(a)–4(d) are the cross-sectional TEM images for the different annealing temperatures, respectively. The TEM figures show that the thickness of the SiO_2 layer annealed at 600 °C, 680 °C, and 780 °C is respectively 2.0 nm, 2.4 nm, and 3.3 nm, while the thickness is 3.0 nm for the devices annealed at 760 °C. The thickness of the SiO_2 tunneling layer is controlled by the annealing temperature, which is a simple and low-cost way to fabricate a series of charge trapping memories with different characteristics.[31,32] Meanwhile, the interface of Ga_2O_3/SiO_2 becomes unclear enough, which indicates that there are inter-diffusion layers generated with the increase of the annealing temperature.

Figure 5 displays the XPS spectra in various depths from the Ga_2O_3 to SiO_2 layers of the CTM device annealed at 760 °C. The binding energy peaks of Ga 3d, Ga $2p_{1/2}$, and Ga $2p_{3/2}$ originated from the Ga–O bonding of Ga_2O_3 are respectively centered at 19.5 eV, 1143.6 eV, and 1116.8 eV, as shown in Fig. 5(a), which is consistent with the report of Kong *et al.*[33] The diversification of the various Si suboxides with depths at the Ga_2O_3/SiO_2 interfaces is obviously reflected in Fig. 5(b).[34] Figure 5(c) shows that the peaks of O 1s binding energy are located at 530.1 eV. The peak width of oxygen XPS broadens close to the SiO_2 layer due to the increase of the lattice oxygen, which demonstrates the presence of oxy-

gen vacancies.[9,35] Atom concentration of Ga, Si, and O elements is counted in the various depths from Ga_2O_3 to SiO_2 layers as shown in Fig. 5(d). The above results show that oxygen vacancies and an inter-diffusion layer are critical for the performance improvement of CTM devices.

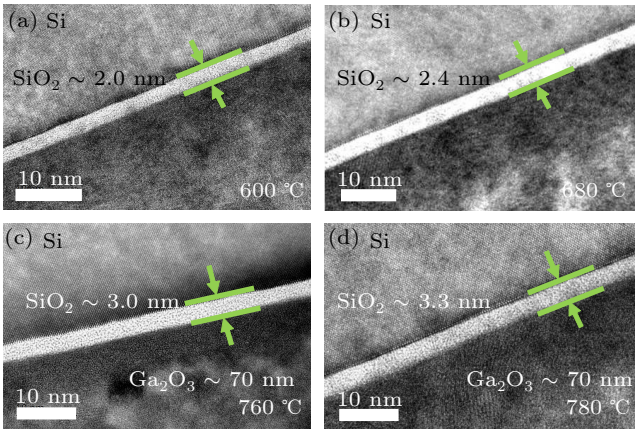


Fig. 4. Cross-sectional TEM images of Au/Ga_2O_3/SiO_2/Si structures annealed at (a) 600 °C, (a) 680 °C, (a) 760 °C, and (a) 780 °C.

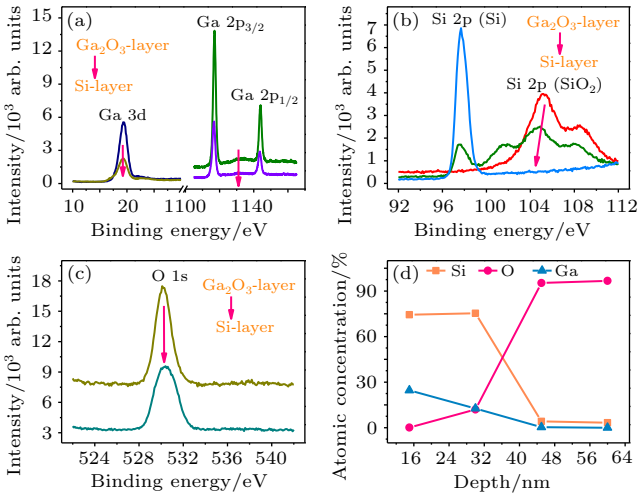


Fig. 5. XPS depth analysis of the device annealed at 760 °C: (a) Ga $2p_{3/2}$, $2p_{1/2}$, and 3d spectrum, (b) Si 2p spectrum, (c) O 1s spectrum, and (d) atom concentration with various depths from Ga_2O_3 to Si layers.

4. Conclusion

In summary, we have studied the charge storage and data retention characteristics of the CTM device with an Au/Ga_2O_3/SiO_2/Si structure. The memory storage windows vary with annealing temperatures, and the largest memory window is 6 V resulted from an annealing temperature of 760 °C. At a working voltage range of ±13 V, the planar charge trapping density of this CTM device is approximately 7.6×10^{11} cm^{-2}. After about 10^4 s of device testing, the degradation of high and low state capacitances is 1% and 1.7%, respectively. These properties are attributed to the oxygen vacancies and the inter-diffusion layer of Ga_2O_3 and SiO_2. This proposed Au/Ga_2O_3/SiO_2/Si structure is promising for the next-generation of CTM devices.

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