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Citation: Chin. Phys. B . 2019, 28(10): 108501 . **doi:** 10.1088/1674-1056/ab3a8b
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Analysis of non-uniform hetero-gate-dielectric dual-material control gate TFET for suppressing ambipolar nature and improving radio-frequency performance*

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(Received 5 January 2019; revised manuscript received 25 July 2019; published online 17 September 2019)

A tunnel field-effect transistor (TFET) is proposed by combining various advantages together, such as non-uniform gate–oxide layer, hetero-gate-dielectric (HGD), and dual-material control-gate (DMCG) technology. The effects of the length of non-uniform gate–oxide layer and dual-material control-gate on the on-state, off-state, and ambipolar currents are investigated. In addition, radio-frequency performance is studied in terms of gain bandwidth product, cut-off frequency, transit time, and transconductance frequency product. Moreover, the length of non-uniform gate–oxide layer and dual-material control-gate are optimized to improve the on-off current ratio and radio-frequency performances as well as the suppression of ambipolar current. All results demonstrate that the proposed device not only suppresses ambipolar current but also improves radio-frequency performance compared with the conventional DMCG TFET, which makes the proposed device a better application prospect in the advanced integrated circuits.

Keywords: non-uniform gate–oxide layer, ambipolar current, radio-frequency performances, tunnel field-effect transistor

PACS: 85.30.Mn, 81.05.Ea, 85.30.Tv **DOI:** 10.1088/1674-1056/ab3a8b

1. Introduction

In order to be better applied to integrated circuits, reduce the cost, and improve the on-state current (I_{on}) and high-frequency characteristics, the size of device needs to be reduced continuously. However, downscaling of the device leads to the increased power dissipation in electronic circuits because of increased leakage current in the off-state. As far as the traditional metal–oxide–semiconductor field-effect transistor (MOSFET) is concerned, it is very difficult to reduce the supply voltage for the purpose of preventing power from dissipating due to the minimum achievable thermionic emission limit of the subthreshold swing (SS) ($SS = 60$ mV/decade) and large off-state current (I_{off}). The appearance of tunnel field-effect transistor (TFET) is consistent with the trend of the continuous downsizing of devices for future ultralow power dissipation integrated circuit applications. The TFET can achieve an SS value less than 60 mV/decade at room temperature due to the fact that the carrier injection of the device from source region to channel region is based on band-to-band tunneling (BTBT).[1] Moreover, the TFET can offer other advantages such as low I_{off} when the barrier width at the source-channel junction is very large in the off-state,[2–4] high immunity against short-channel effects (SCEs), and small supply voltage below 0.5 V.[5,6] However, the TFET has some shortcomings such as low I_{on}, ambipolar current (I_{amb}), and large Miller capacitance. The I_{on} should be enhanced and ambipolar behavior and Miller capacitance should be well reduced in order to make TFET a better application prospect in the future integrated circuit. Therefore, researchers should comprehensively carry forward the advantages of TFET and overcome its shortcomings. Up to now, many techniques have been proposed to improve I_{on}, such as narrow bandgap materials,[7–11] high-k gate dielectric,[12] hetero-junction mechanism,[13,14] and doping-less TFETs,[15] source-side pocket doping,[16] hetero-stacked TFET,[17] heteromaterial gate,[18,19] *etc*. The I_{amb} can be reduced by using the dual-material control-gate (DMCG) TFETs,[20] charge plasma-based TFETs with gate engineering,[21,22] gate material workfunction engineering,[23] lightly doped drain,[24] and gate–drain underlap structure.[25,26] Moreover, a hetero-gate-dielectric (HGD) TFET with a high gate–oxide dielectric near the source side and a low gate–oxide dielectric near the drain side can enhance I_{on} and obtain promising radio frequency performance.[27–29]

The downscaling of gate–oxide layer thickness is an important method to enhance the steep switching characteristics of TFETs. But it also leads to large gate leakage current. Moreover, the thickness of the gate–oxide layer is assumed to be uniform in almost all existing TFET devices. Therefore, it is necessary to study the variation of the TFET characteristics in the case of non-uniform gate–oxide layer thickness. The non-uniform structure is defined as a structure whose gate–oxide thickness is thinner on the source-channel side while larger gate–oxide thickness on the drain-channel side. Recently, a TFET with non-uniform gate–oxide shape and an

*Project supported by the University Natural Science Research Key Project of Anhui Province, China (Grant No. KJ2017A502), the Introduced Talent Project of Anhui Science and Technology University, China (Grant No. DQYJ201603), the Excellent Talents Supporting Project of Colleges and Universities, China (Grant No. gxyq2018048), and the Innovation and Entrepreneurship Training Program for College Students, China (Grant No. 2018S10879052).

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asymmetric hetero-dielectric engineered dual-material double gate (DG) TFET has been analyzed.[30,31] In the present work, a novel device is proposed by combining various advantages together such as non-uniform gate–oxide shape, HGD and DMCG, and named NDMCG TFET. It is intended that in the proposed device the I_{amb} value can be reduced, the on-off current ratio can be enhanced, and the radio-frequency (RF) performance can be improved by optimizing the structural parameters of device.

2. Device structure

The structure of NDMCG TFET is shown in Fig. 1. The gates closer to the source and the drain are denoted as G (tunneling gate) and G_2 (auxiliary gate), respectively. The gate between G and G_2 is marked as G_1 (control gate). In the proposed device, the work function of G is selected to be the same as that of G_2, but their work functions are less than that of G_1. The parameters used in the following simulations are P+ source, channel, and N+ drain, and they are doped with concentration 10^{20} cm^{-3}, 10^{16} cm^{-3}, and 5×10^{19} cm^{-3}, respectively. The thickness of silicon (t_{si}) is 10 nm, the thickness of HfO_2 (t_1) and the maximum thickness of SiO_2 (t_2) are 1 nm and 3 nm, respectively. The length of P+ source (L_s), channel (L_{ch}), and N+ drain (L_d) are 50 nm, 50 nm, and 50 nm, respectively. The length of HfO_2, G, G_1, and G_2 are L_{ox}, L_1, L_2, and L_3, respectively.

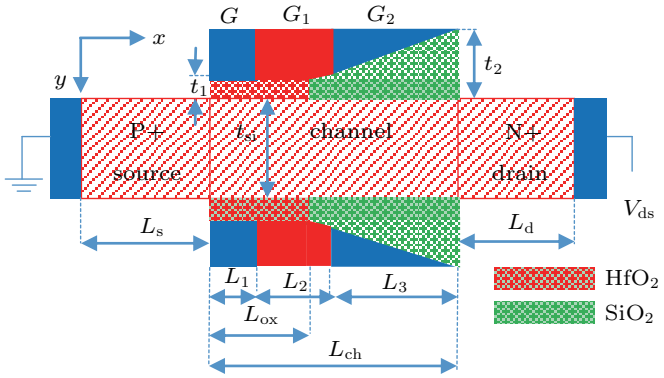


Fig. 1. Structure of non-uniform gate–oxide layer hetero-gate-dielectric DMCG TFET.

The simulations are performed by using silvaco atlas simulator,[32] and the models such as dynamic nonlocal band-to-band tunneling model, Shockley–Read–Hall model, auger recombination model, bandgap narrowing model, and Fermi statistics model are used in this work. The dynamic nonlocal band-to-band tunneling model is an important model in describing the operating principle of TFET. Using the Kane model,[33] the band-to-band tunneling generation rate is expressed as[34]

$$G_{BTBT} = AE^{D}\exp\left(-\frac{B}{E}\right), \tag{1}$$

where A and B are the tunneling parameters, which are 4×10^{14} cm$^{-1/2}\cdot$V$^{-5/2}\cdot$s^{-1} and 1.9×10^{7} V/cm, respectively;[32] E is the lateral electrical field; D is a material-dependent constant, which is 2 and 2.5 for the direct and indirect band-gap materials, respectively. The values of I_{on}, I_{off}, and I_{amb} defined at V_{gs} = 0.8 V, 0 V, and −0.5 V respectively are calculated when V_{ds} is fixed at 0.5 V, here V_{gs} and V_{ds} are the gate–source voltage and drain–source voltage, respectively.

3. Results and discussions

3.1. Performance comparison between NDMCG TFET and DMCG TFET

Figure 2 shows the energy band, carrier concentration, and electric field for two devices under thermal equilibrium

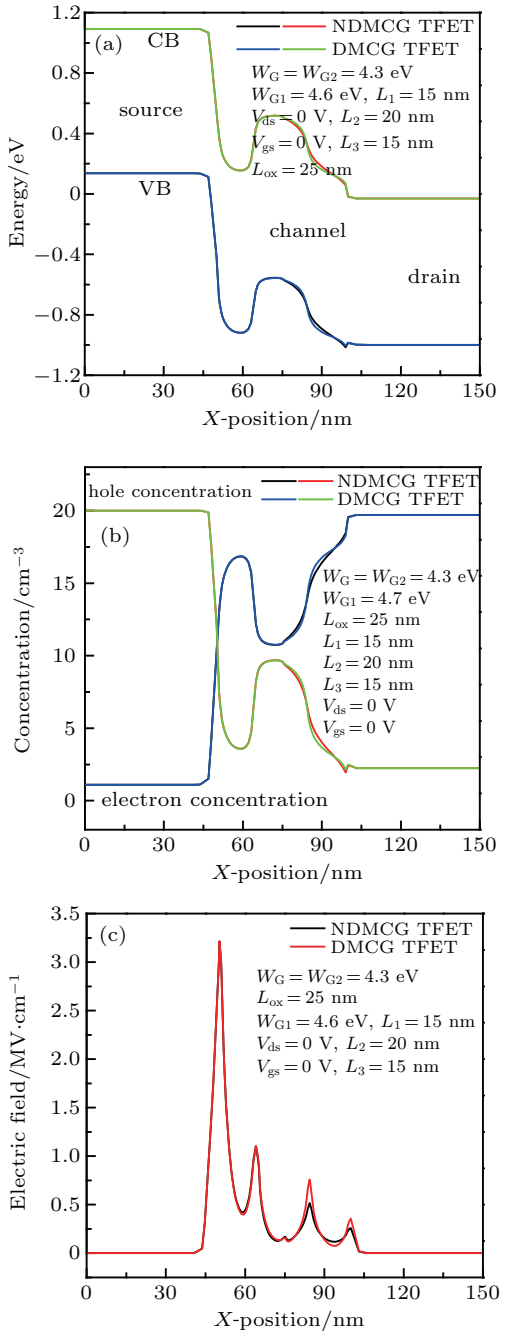


Fig. 2. Comparisons of curves of (a) energy band, (b) carrier concentration, and (c) electric field *versus* X pointion between NDMCG TFET and DMCG TFET under thermal equilibrium state.

state. From Fig. 2(a), it can be found that there is no change of the tunneling distance at the source/channel interface since the modification is made on the channel close to the drain side. However, the increased tunneling barrier at the drain/channel junction can be seen for the NDMCG TFET. The NDMCG TFET provides higher hole concentration and lower electron concentration than the DMCG TFET as shown in Fig. 2(b). Hence, the electric field varies at the drain/channel junction along the lateral direction between NDMCG TFET and DMCG TFET as shown in Fig. 2(c). The reduced electric field can be observed for the NDMCG TFET due to the varying band levels and the different carrier concentrations.

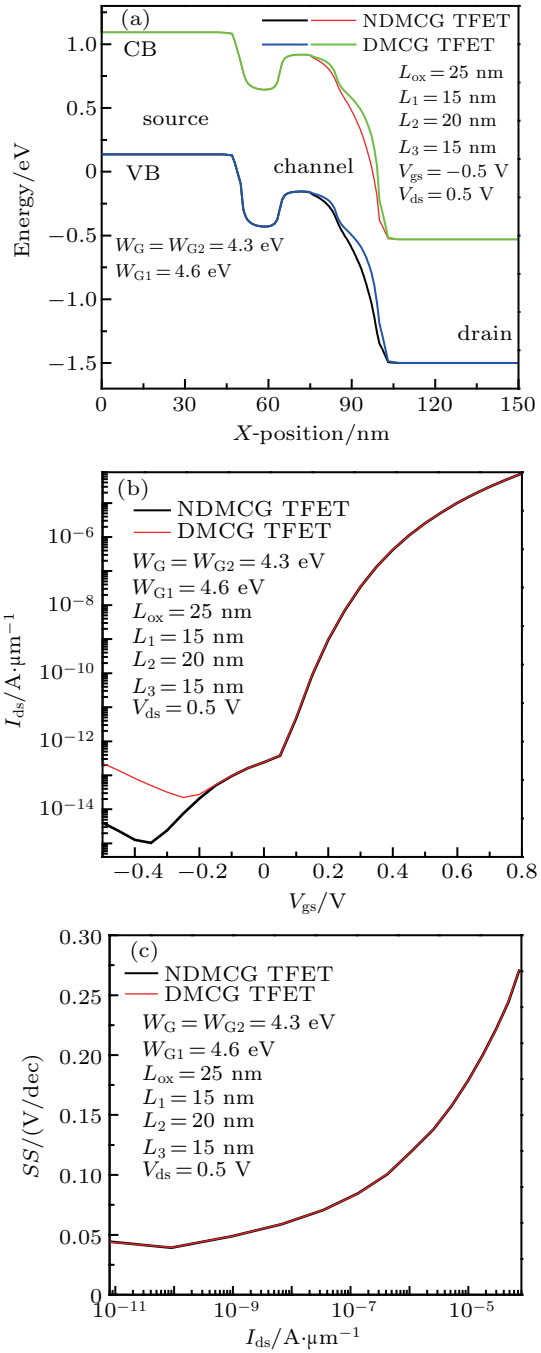


Fig. 3. Comparisons (a) energy band under ambipolar state, (b) transfer characteristics, and (c) subthreshold swing between NDMCG TFET and DMCG TFET.

Figure 3 shows the energy bands under ambipolar state, transfer characteristics, and *SS* for two devices. It can be seen that the tunneling width of NDMCG TFET is larger than that of the DMCG TFET at the drain/channel junction under ambipolar state, which can limit the number of holes to tunnel from the drain to the channel. Therefore, the NDMCG TFET can reduce the ambipolar current as depicted in Fig. 3(b). The *SS* as a function of I_{ds} is shown in Fig. 3(c). It can be seen that the extracted *SS* behavior appears relatively gradual lasting nearly 4 orders of magnitude of drain current variation. But it is worth noting that the two devices show little difference in *SS*. This is mainly due to the fact that the non-uniform gate–oxide shape of NDMCG TFET is made on the channel close to the drain side, so it has little effect on the ΔG_{BTBT} increament as well as on the drain current increament $\Delta \log I_{ds}$ with V_{gs} increasing.

3.2. Optimization of L_1, L_2, and L_{ox} for NDMCG TFET

This subsection is dedicated to the study of the influence of variation in L_2 on I_{on} and I_{off} for NDMCG TFET as depicted in Fig. 4(a). In this case, L_1 is fixed at 15 nm. The increase in L_2 leads to the reduction of I_{on} when the length of L_2 is larger than 5 nm. Moreover, the NDMCG TFET can generate optimum results of I_{off} and I_{on} when L_2 is fixed at 10 nm. The I_{amb} for NDMCG TFET is less than that for the DMCG TFET because the tunneling width of NDMCG TFET is larger than that of the DMCG TFET at the drain/channel junction, hence tunneling of carriers from drain to channel is reduced, resulting in reduced I_{amb} as shown in Fig. 4(b). Therefore, we can conclude that the proposed device provides a decent amount of suppression in I_{amb} and large on-off current ratio when L_1, L_2, and L_3 are 15, 10, and 25 nm, respectively.

Figure 5(a) is dedicated to the study of the influence of variation in L_1 on I_{on} and I_{off} for NDMCG TFET. In this case, L_3 is fixed at 15 nm. The NDMCG TFET can generate a large on-off current ratio when L_1 is 15 nm. However, I_{amb} for NDMCG TFET is not significantly degraded with variation in L_1 since the energy band at the drain/channel junction hardly changes under these conditions as indicated in Fig. 5(b). The I_{amb} for NDMCG TFET is less than that for DMCG TFET, which is due to the fact that the tunneling width of NDMCG TFET is larger than that of the DMCG TFET at the drain/channel junction. Hence, we can infer that selecting $L_1 = 15$ nm along with $L_2 = 20$ nm and $L_3 = 15$ nm provides a decent amount of suppression in I_{amb} and large on-off current ratio. Based on the preceding analysis, it is clear that the optimized dual-material control-gate lengths (L_1, L_2, L_3) are 15, 10, 25 nm and 15, 20, 15 nm in terms of suppression in I_{amb} and large on-off current ratio.

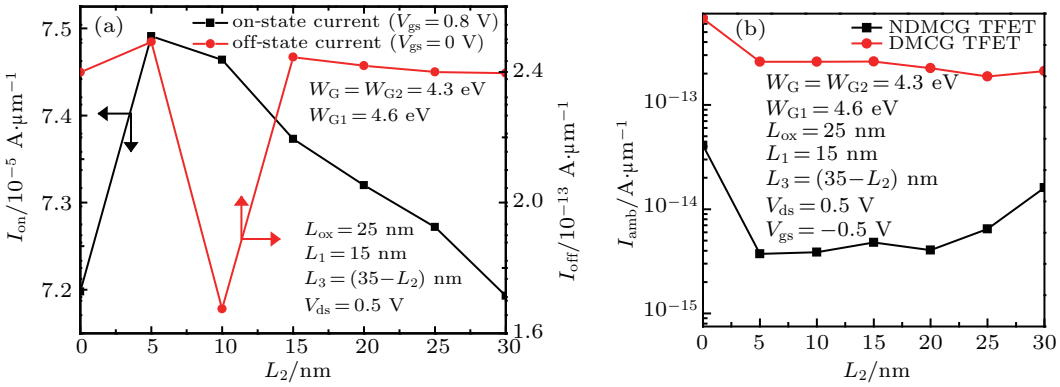


Fig. 4. (a) I_{on} and I_{off} varying with L_2 for NDMCG TFET, and (b) I_{amb} varying with L_2 for NDMCG TFET and DMCG TFET.

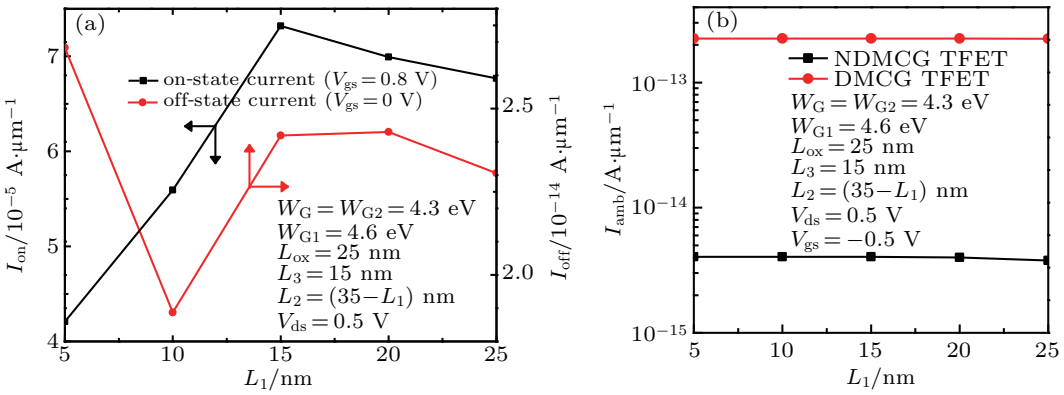


Fig. 5. (a) I_{on} and I_{off} varying with L_1 for NDMCG TFET, and (b) I_{amb} varying with L_1 for NDMCG TFET and DMCG TFET.

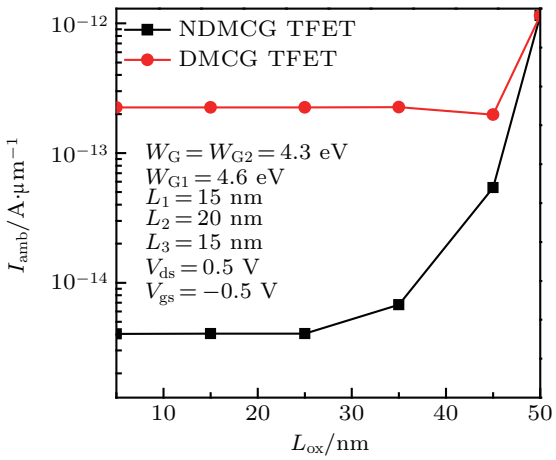


Fig. 6. I_{amb} varying with L_{ox} for NDMCG TFET and DMCG TFET.

Figure 6 shows the influence of variation in L_{ox} on I_{amb} for NDMCG TFET and DMCG TFET when L_1, L_2, and L_3 are fixed at 15, 20, and 15 nm, respectively. It is expected that as I_{amb} increases the L_{ox} increases because the gate control is strengthened. Moreover, when the length of L_{ox} is longer than 35 nm, I_{amb} is increased sharply. It should be noted that the length of L_{ox} is 50 nm, which represents the uniform HfO_2 case ($t_1 = t_2 = 1$ nm). The proposed device can generate small I_{amb} especially when L_{ox} is less than 35 nm. Generally speaking, suppression in I_{amb} and large on-off current ratio can be obtained by optimizing L_1, L_2, L_3, and L_{ox} for the NDMCG TFET, but the optimized device has not achieved superior performance about *SS* compared with the DMCG TFET. However, a hetero-stacked TFET with stacked source configuration can effectively suppress the *SS* degradation behavior and obtain a steeper average *SS* by self-adaptive current replenishing with bandgap engineering.[17,35] The optimization of *SS* for the NDMCG TFET is not considered and it will be dealt with in our subsequent work.

3.3. Parasitic capacitance and radio-frequency performance for NDMCG TFET

This subsection is dedicated to the study of the influence of variation in L_3, and L_1 on the gate–drain capacitance (C_{gd}) of NDMCG TFET as depicted in Fig. 7. The increase in C_{gd} with V_{gs} is due to the formation of an inversion layer in the channel region from the drain to the source. Moreover, C_{gd} is dominated by the inversion capacitance in the on-state. The increase of L_3 in Fig. 7(a) or L_1 in Fig. 7(b) represents the decrease of L_2 in the proposed device. Therefore, the effect of control gate's work function on the threshold voltage of the device becomes smaller with L_2 decreasing. The threshold voltage of the proposed device decreases, which leads to an increase in charge and ultimately an increase in capacitance.

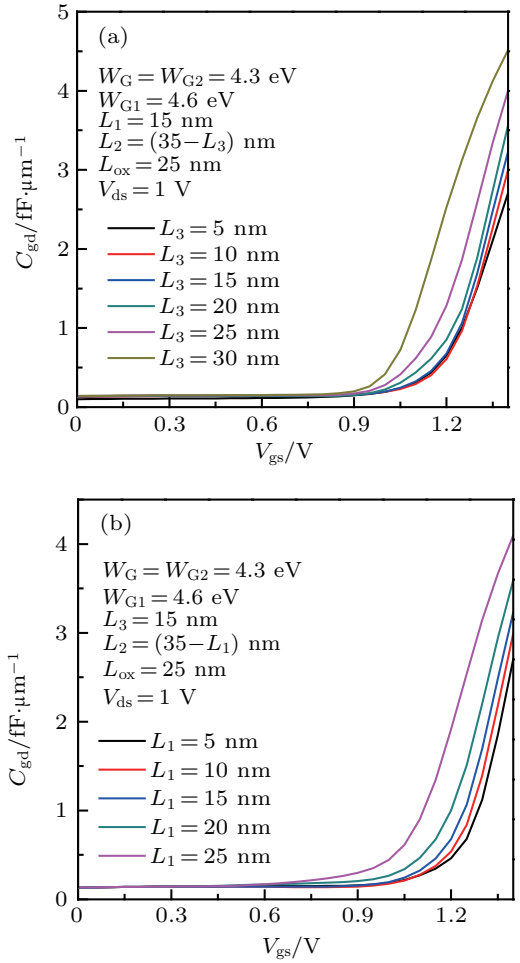


Fig. 7. C_{gd} varying with (a) L_3 and (b) L_1 for NDMCG TFET.

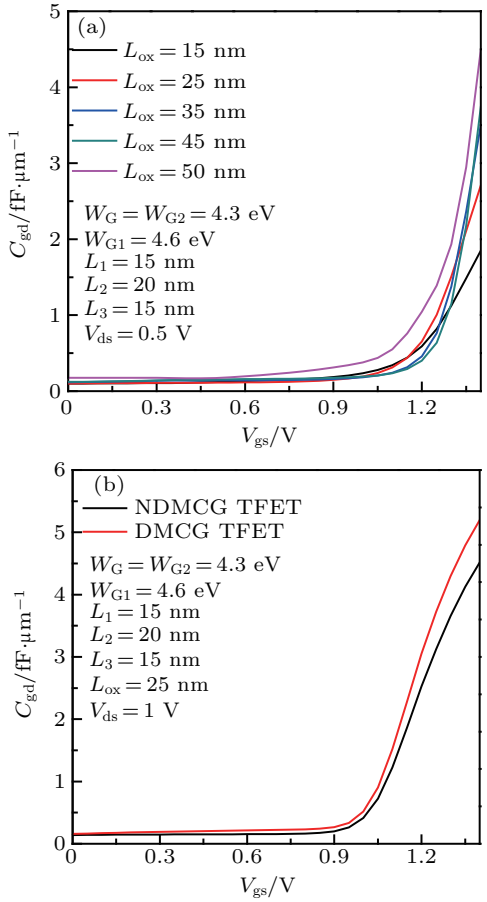


Fig. 8. (a) C_{gd}–V_{gs} curves for NDMCG TFET with different values of L_{ox}, and (b) comparison of C_{gd}–V_{gs} curve between NDMCG TFET and DMCG TFET.

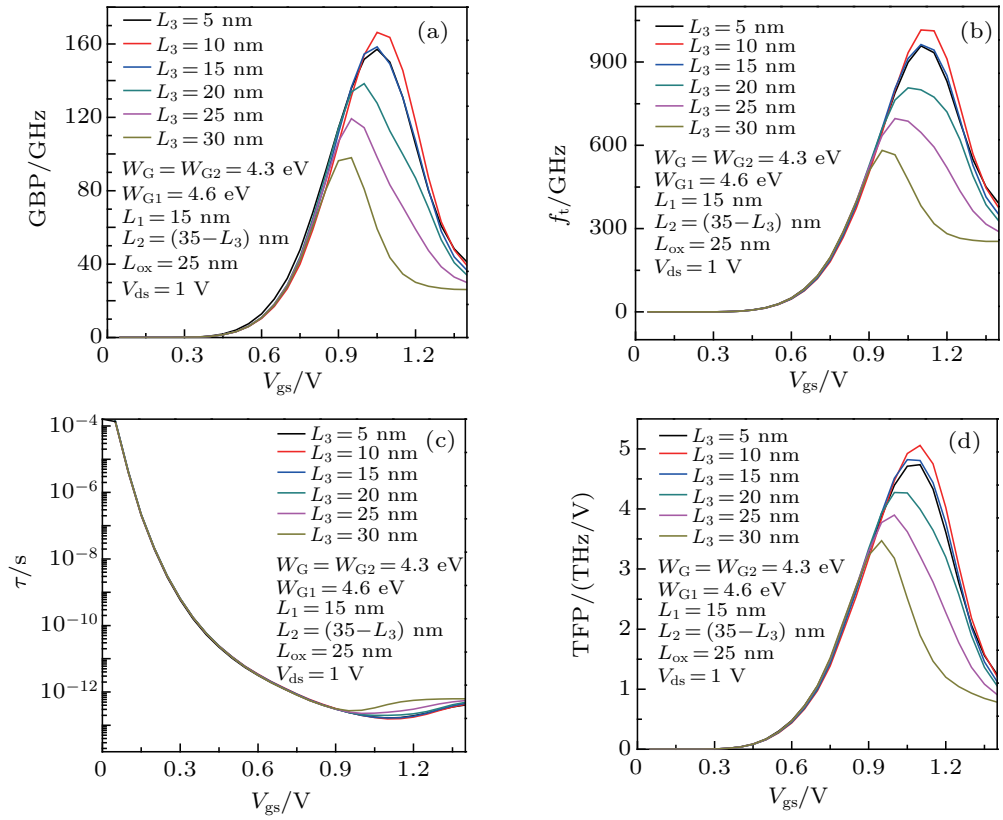


Fig. 9. Curves of (a) GBP, (b) f_t, (c) τ, and (d) TFP *versus* V_{gs} of NDMCG TFET for different values of L_3.

Figure 8(a) shows the variation of C_{gd} with V_{gs} for NDMCG TFET with L_1, L_2, and L_3 being 15, 20, and 15 nm, respectively. It can be found that C_{gd} increases with L_{ox} increasing, which is due to the fact that the gate–oxide thickness near the drain region is varied. This effect indicates the importance of the design of non-uniform gate–oxide layer. Moreover, non-uniform gate–oxide layer can reduce the coupling between the gate and the drain regions, thereby reducing C_{gd}. The C_{gd} of NDMCG TFET is less than that of DMCG TFET under all the same conditions as shown in Fig. 8(b). Therefore, The NDMCG TFET can better control the gate over the channel region.

Further, RF parameters of gain bandwidth product (GBP), cut-off frequency (f_t), transit time (τ), and transconductance frequency product (TFP) are analyzed. The GBP determines the maximum working frequency for a direct current gain of 10, and the formula of GBP is $g_m/\left(20\pi C_{gd}\right)$,[15,22] where g_m is the transconductance. f_t is the frequency at which the short-circuit current gain is unity, a criterion that is important for the quantification of the TFET performance in high-speed digital applications. The f_t is defined as $g_m/\left[2\pi\left(C_{gd}+C_{gs}\right)\right]$,[15,22] where C_{gs} is the gate–source capacitance. Figures 9(a) and 9(b) show that the NDMCG TFET with 10 nm of L_3 exhibits high GBP and f_t due to the reduced parasitic capacitance and enhanced transconductance. Similarly, the NDMCG TFET with 15 nm of L_1 exhibits high GBP and f_t as shown in Figs. 10(a) and 10(b).

Transit time (τ) is defined as the time taken for carriers to flow from source to drain region, and it is also another important parameter to confirm the NDMCG TFET for high-frequency operation, which is expressed as $\left(C_{gd}+C_{gs}\right)/g_m$. The comparison of τ between NDMCG TFETs with different values of L_3 (Fig. 9(c)) and L_1 (Fig. 10(c)) explains that the values of τ for NDMCG TFET under the lengths of L_1, L_2, L_3 being respectively 15, 25, 10 nm and 15, 20, 15 nm are less than those in the other cases over the entire range of V_{gs}. Therefore, better response and high operational speed can be obtained in both cases. Transconductance frequency product (TFP) is another important parameter to obtain the device characteristics for high-speed designs, and it is defined as $g_{m*}f_t/I_{ds}$, where I_{ds} is the drain–source current. The comparative results of the TFP for the proposed device are shown in Figs. 9(d) and 10(d), respectively. It can be found that the TFP of the proposed device reaches a peak value. However, the value begins to decrease as V_{gs} increases due to mobility degradation. Combining the analysis results of suppression in I_{amb} and large on-off current ratio, the optimized dual-material control-gate lengths of L_1, L_2, and L_3 are obtained to be 15, 20, 15 nm, respectively.

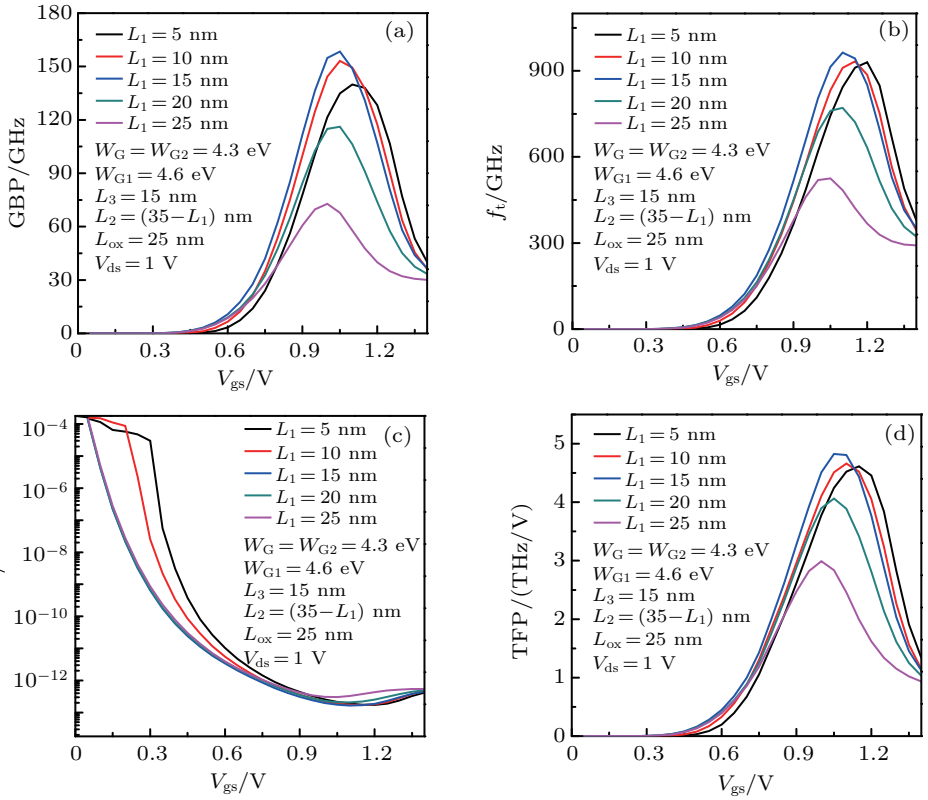


Fig. 10. Curves of (a) GBP, (b) f_t, (c) τ, and (d) TFP *versus* V_{gs} for NDMCG TFET with different values of L_1.

Figure 11 shows the influences of variation in L_{ox} on GBP, f_t, τ, and TFP for NDMCG TFET, with L_1, L_2, and L_3 fixed at 15, 20, and 15 nm, respectively. It can be found that the maximum values of GBP, f_t, and TFP increase with the value of L_{ox} increasing, but the values of three parameters described above decrease when the length of L_{ox} is 50 nm. It should be noted that the length of L_{ox} is 50 nm, which represents the uniform HfO_2 case ($t_1 = t_2 = 1$ nm). The proposed device embodies

the advantages of non-uniform hetero-gate-dielectric in terms of three parameters, and an optimum value ($L_{ox} = 45$ nm) exists at which the parameters are maximum. It is worth noting that there is little difference among the three parameters when L_{ox} is 45 nm and 35 nm, separately. By combining with the analysis results of Fig. 6, the optimum value of L_{ox} is obtained to be 35 nm. But the difference in transit time is not obvious in the above cases.

Figure 12 shows comparison of curves of GBP, f_t, τ, and TFP *versus* V_{gs} between NDMCG TFET and DMCG TFET, with L_{ox}, L_1, L_2, and L_3 fixed at 35, 15, 20, and 15 nm, respectively. The results show that the NDMCG TFET has a better RF performance than the conventional DMCG TFET. High GBP implies larger gain as well as bandwidth, the increase in f_t results in small switching delay. All these results demonstrate that the proposed device has a better prospect of high-speed and high-frequency applications in the advanced integrated circuits.

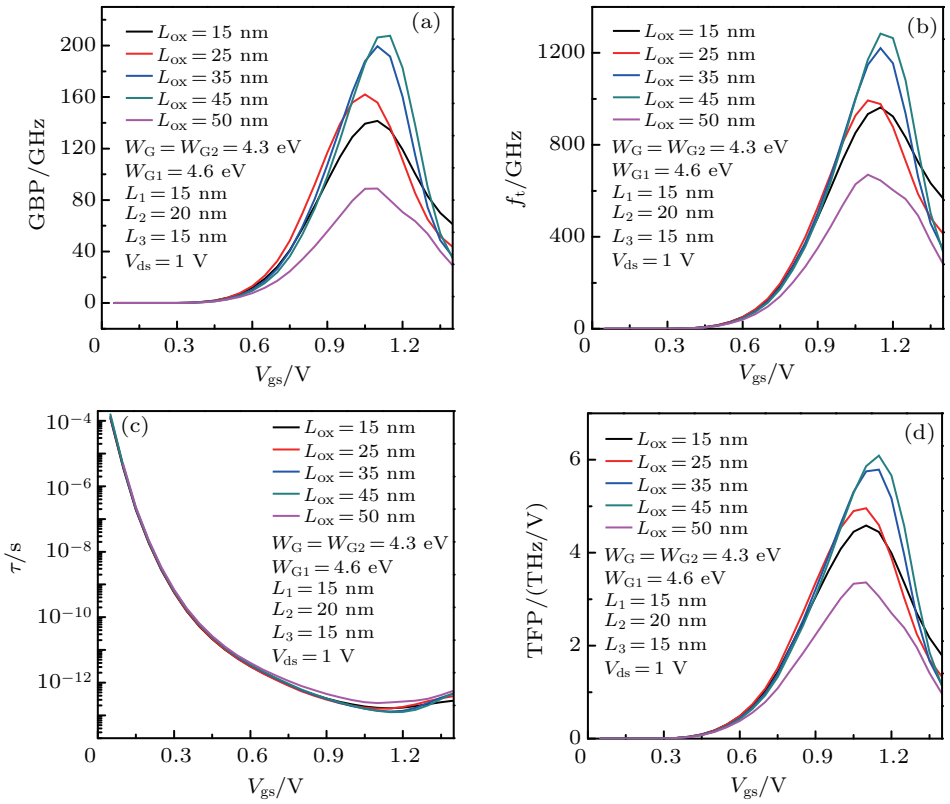


Fig. 11. Curves of (a) GBP, (b) f_t, (c) τ, and (d) TFP *versus* V_{gs} for NDMCG TFET with different values of L_{ox}.

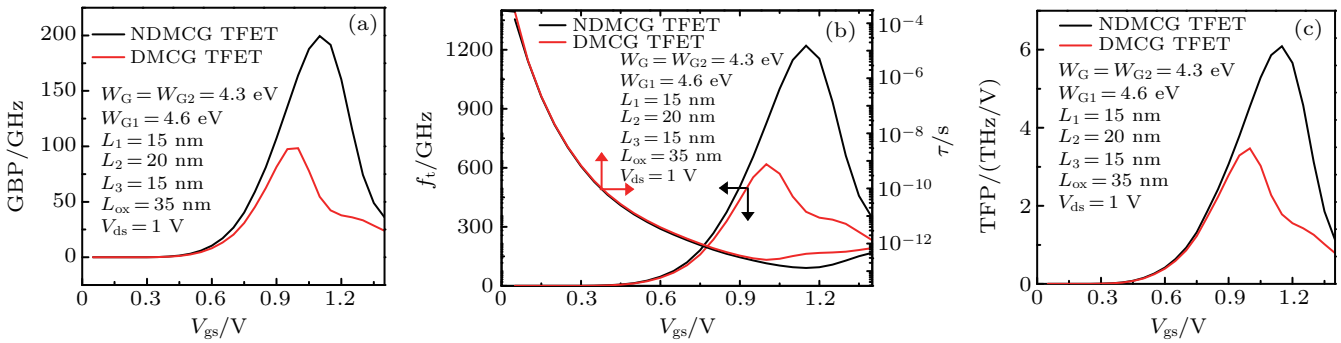


Fig. 12. Comparison of curves of (a) GBP, (b) f_t, τ, and (c) TFP *versus* V_{gs} between NDMCG TFET and DMCG TFET, with V_{ds} fixed at 1 V.

The above-mentioned parasitic capacitance and RF parameters for TFETs are analyzed when V_{ds} is 1 V, and the maximum values for GBP, f_t, and TFP are achieved when V_{gs} is nearly 1.1 V. However, according to the projection of International Technology Roadmap for Semiconductor (ITRS), the TFET has a great potential for low-power applications. In this case, V_{ds} is lower than 1 V. Therefore, the device optimization is also analyzed when V_{ds} is fixed at 0.5 V as indicated in Fig. 13, from which we can infer that the NDMCG TFET enhances the RF parameters compared with the conventional DMCG TFET under lower power supply voltage. Moreover, the maximum values for GBP, f_t, and TFP are achieved when V_{gs} is nearly 0.7 V. Therefore, the proposed device is also suitable for power supply voltage applications.

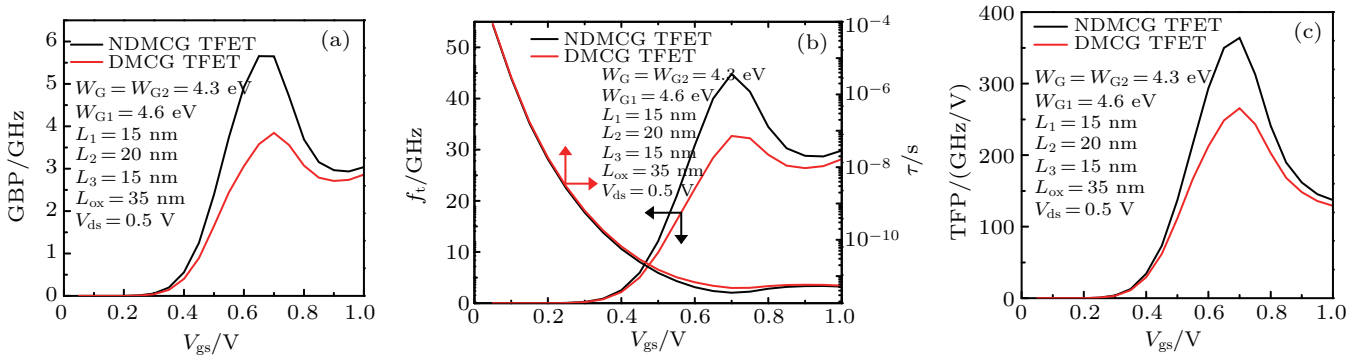


Fig. 13. Comparison of curves of (a) GBP, (b) f_t, τ, and (c) TFP *versus* V_{gs} between NDMCG TFET and DMCG TFET, with V_{ds} fixed at 0.5 V.

4. Conclusions

The performances of NDMCG TFET are studied based on TCAD simulations. We demonstrate that the increase of L_{ox} affects I_{amb}, but has little effect on I_{on} and I_{off}. The results show that the design of a non-uniform gate–oxide layer with L_{ox} being 35 nm and the dual-material control-gate lengths L_1, L_2, and L_3 being respectively 15, 20, 15 nm can realize high I_{on}/I_{off} and RF parameters with relatively low value of I_{amb}. When the drain–source voltage is fixed at 1 V for the optimized device, the RF parameters GBP, f_t, and TFP are investigated, of which the maximum values are 199 GHz, 1.2 THz, and 6.1 THz, respectively. Moreover, the RF parameters of the NDMCG TFET are enhanced compared with those of the conventional DMCG TFET under lower power supply voltage. The results indicate that the NDMCG TFET has the great potential applications in high-performance RF component, which should be the superiority in future high-frequency, and high-switching-speed electronics applications.

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