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Performance improvement of 4H-SiC PIN ultraviolet avalanche photodiodes with different intrinsic layer thicknesses*

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Four 4H-SiC p–i–n ultraviolet (UV) avalanche photodiode (APD) samples PIN-0.1, PIN-0.35, PIN-0.5, and PIN-1.0 with different intrinsic layer thicknesses (0.1 μm, 0.35 μm, 0.5 μm, and 1.0 μm, respectively) are designed and fabricated. Single photon detection efficiency (SPDE) performance becomes better as the intrinsic layer thickness increases, which is attributed to the inhibitation of tunneling. Dark count origin is also investigated, an activation energy as small as 0.22 eV of the dark count rate (DCR) confirms that the trap-assisted tunneling (TAT) process is the main source of DCR. The temperature coefficient ranges from −2.6 mV/°C to 18.3 mV/°C, demonstrating that the TAT process is dominant in APDs with thinner intrinsic layers. Additionally, the room temperature maximum quantum efficiency at 280 nm differs from 48% to 65% for PIN-0.35, PIN-0.5, and PIN-1.0 under 0 V bias, and UV/visible rejection ratios higher than 10^4 are obtained.

Keywords: 4H-SiC, avalanche photodiode, single photon detection efficiency, tunneling

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1. Introduction

Extremely weak ultraviolet (UV) light sensitive and visible blind detectors are required in numerous applications, such as medical treatment, flame detection, and volcano observation. Among all the UV light sensitive semiconductor materials, 4H-SiC has a wide bandgap (∼ 3.26 eV) and enjoys the advantages of high intrinsic visible blindness, good quantum efficiency, low operation voltage, ruggedness, and more mature process technology.[1,2] Recently, Zhou *et al.* reported SiN_x passivated large-area (600 μm diameter) 4H-SiC avalanche photodiodes (APDs) with a high multiplication gain of 6.5×10^5 and a low dark current density of 0.88 $\mu A/cm^2$ at the gain of 1000.[3] Su *et al.* studied the degree of avalanche uniformity across device mesa of 4H-SiC APDs via imaging the hot carrier luminescence pattern of the devices in the avalanche regime.[4] Chong *et al.* reported the effect of the beveled mesa angle on the leakage performance of 4H-SiC APDs, the results demonstrated that a small-slope beveled mesa APD means more uniform dark current level in the linear region.[5]

Although many 4H-SiC APDs have been fabricated and investigated, systematic study on the relation between device performance and certain parameters is rarely seen recently. As far as we know, few reports about the influence of the intrinsic layer (i-layer) thickness on SiC APDs performance are presented. According to the work of Campbell *et al.*,[6] APD with thicker i-layer inhibits tunneling process better, hence the dark current level before avalanche breakdown is lower. Nevertheless, further study of the influence of the i-layer thickness is quite limited, especially on the temperature coefficient, quantum efficiency (QE), and single photon detection efficiency (SPDE). On the other hand, the origin of dark counts is a vital research direction since the dark count rate (DCR) plays an important role in the overall performance of SiC APDs. A better understanding of DCR mechanism helps for the improvement of APD devices. The commonly considered origins include diffusion from quasi-neutral regions, generation recombination in the depletion layer, tunneling, and surface generation recombination.[1] The temperature dependences of these DCR origins are quite distinctive, but it has been seldom used to investigate the DCR origins of 4H-SiC APDs.

In this work, 4H-SiC p–i–n APDs with four different i-layer thicknesses are designed and fabricated. The relationships between the i-layer thickness and device performance, such as dark current level, temperature coefficient, QE, and SPDE are analyzed. The origin of DCR is also discussed.

2. Experimental details

The cross-sectional schematic diagram of the 4H-SiC p–i–n APD under investigation is shown in Fig. 1(a). The APD has a typical mesa side of 120×60 μm, as shown in Fig. 1(b). The epi-structure from top to bottom consists of

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a contact layer, a transition layer, an intrinsic layer, another contact layer, and an n-type 4H-SiC substrate. Please note that the main distinction between the four APDs is the thickness of layer 3 (i-layer), detailed information is given in Table 1. According to numerous experiment data, two APD samples with the same epi-layer thickness and the opposite doping types have very similar overall performance, so the doping type difference of PIN-0.35 should be ignored. The fabrication procedure begins with mesa etching, which is conducted in an inductively coupled plasma etching system with CF_4/O_2 as the etching gas. By using a photoresist reflow technique, the SiC mesa inherits the shape of the photoresist. A positive beveled mesa with a small slope angle of $\sim 3.6^\circ$ is obtained. The device surface is then passivated by thermal oxidation at 1050 °C in O_2 atmosphere followed by 1 μm SiO_2 layer deposited by plasma-enhanced chemical vapor deposition at 350 °C. After opening the contact windows by wet etching, n and p metal contacts both using Ni/Ti/Al/Au (35 nm/50 nm/200 nm/100 nm) metal stack are deposited by e-beam evaporation, which are finally annealed by rapid thermal annealing at 850 °C for 3 min in N_2 ambient.

The SPDE and DCR characteristics of the fabricated APDs are investigated via a passive-quenching mode circuit. In the passive quenching circuit, the APD is serially connected with a Keithley 2636 source meter, a quenching resistor, and a sampling resistor, which is further parallel connected to a Tektronix 4032 oscilloscope. Detailed information can be found in Ref. [7].

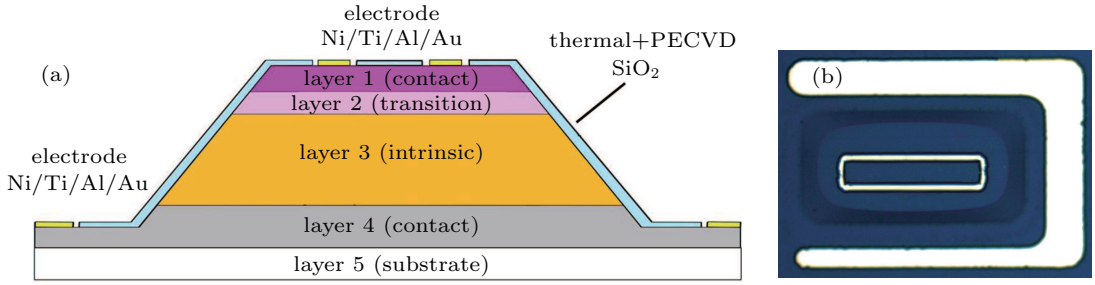


Fig. 1. (a) Cross-sectional schematic diagram of the 4H-SiC p–i–n APD. (b) The top view image of one fabricated SiC APD.

Table 1. Detailed epitaxial information of the APDs under test.

	PIN-0.1	PIN-0.35	PIN-0.5	PIN-1.0
Layer 1	0.2 μm (n^+) 2×10^{19} cm^{-3}	0.1 μm (p^+) 2×10^{19} cm^{-3}	0.2 μm (n^+) 2×10^{19} cm^{-3}	0.2 μm (n^+) 2×10^{19} cm^{-3}
Layer 2	0.2 μm (n) 2×10^{18} cm^{-3}	0.2 μm (p) 2×10^{18} cm^{-3}	0.2 μm (n) 2×10^{18} cm^{-3}	0.2 μm (n) 2×10^{18} cm^{-3}
Layer 3	0.1 μm (n^-) 2×10^{16} cm^{-3}	0.35 μm (p^-) 2×10^{16} cm^{-3}	0.5 μm (n^-) 2×10^{16} cm^{-3}	1.0 μm (n^-) 2×10^{16} cm^{-3}
Layer 4	5.0 μm (p^+) 3×10^{18} cm^{-3}	2.0 μm (n) 3×10^{18} cm^{-3}	5.0 μm (p^+) 3×10^{18} cm^{-3}	5.0 μm (p^+) 3×10^{18} cm^{-3}
Layer 5	Sub (n^+)	Sub (n^+)	Sub (n^+)	Sub (n^+)

3. Results and discussion

The room-temperature (RT) current–voltage (I–V) and the gain–voltage characteristics of PIN-0.5 (the i-layer thickness is 0.5 μm) are shown in Fig. 2(a). The dark current remains below 10^{-13} A level before the dark current sharply rises. Under an over bias of 2 V, the avalanche gain of PIN-0.5 can reach 4×10^5. The dark current as a function of the reverse voltage normalized to the breakdown voltage (V_{br}) of the four APDs is shown in Fig. 2(b). The dark current of PIN-0.1 and PIN-0.35 increases as the voltage increases and ends in 2–3 orders of magnitude higher than that of PIN-0.5 and PIN-1.0 near breakdown. According to Bai's work,[8] the suppression of the trap-assisted tunneling (TAT) becomes weaker as the i-layer becomes thinner, so the dark current increase should be caused by the TAT enhancement. Since there is an internal current gain caused by the impact ionization at high reverse voltage, it is hard to estimate the tunneling current level. Assuming that the avalanche multiplication which the tunneling current goes through is similar to the photocurrent, the primary multiplied dark current can be obtained by dividing the dark current by the corresponding gain,[6] as shown in the inset of Fig. 2(b). From PIN-1.0 with 1.0-μm i-layer to PIN-0.1 with 0.1-μm i-layer, more than four orders of magnitude of the primary dark current reduction near breakdown (e.g., near the over bias 0 V) is observed, indicating a clear tunneling current reduction with the increase of the i-layer thickness.

The SPDE/DCR characteristics of PIN-0.35, PIN-0.5, and PIN-1.0 are investigated under different over biases, as shown in Fig. 3(a). The SPDE of APDs with thicker i-layer grows faster under the same DCR increase. At an over bias of 1% V_{br}, the SPDE/DCR of PIN-1.0 is 0.4%/kHz, while that of PIN-0.35 is 0.15%/kHz. The better SPDE is typical for APDs with thicker i-layer, owing to the increase in higher-order impact ionization events and the chance of a carrier to initiate a self-sustaining avalanche.[9] On the other hand, the critical electric field (E_c) of 4H-SiC is not fixed at a certain value, but slightly decreases as the i-layer thickness increases.[10] For APDs with thicker i-layer, the avalanche could sustain itself under a lower electric field, while the energy band does not bend enough to induce considerable DCR. Therefore, the

SPDE of PIN-1.0 rises faster while the DCR hardly increases before the over bias of 0.6% V_{br}. As the over bias further increases, the DCR sharply rises as the energy band bending increases and thus the slope of SPDE/DCR becomes gentle.

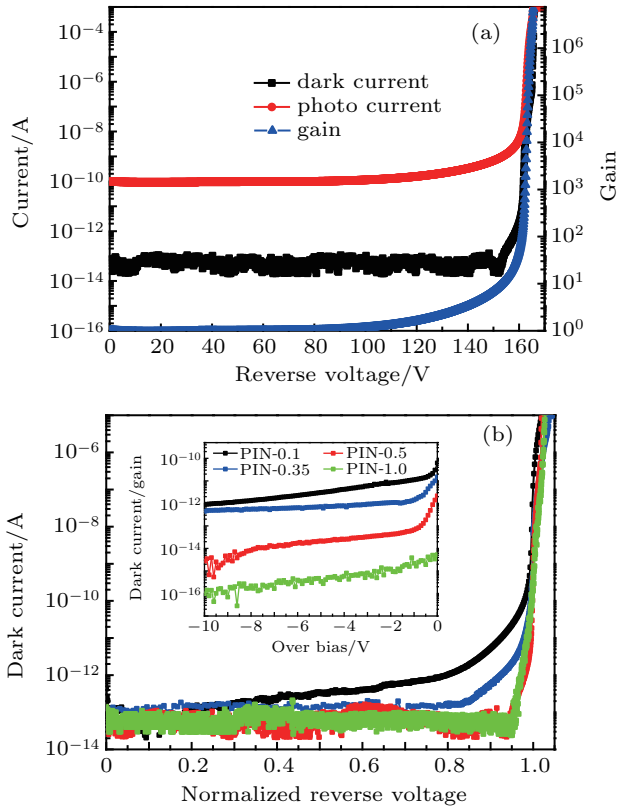


Fig. 2. (a) RT reverse *I*–*V* and gain–voltage characteristics of PIN-0.5. (b) The reverse dark current as a function of normalized reverse voltage for the four APDs. The inset shows the reverse dark current (normalized to gain) as a function of over bias before breakdown.

In order to verify the origin of DCR, the DCR–overbias characteristics of PIN-0.5 are investigated at RT, as shown in Fig. 3(b). The DCR exhibits a quasi-exponential dependence of over bias, which corresponds to TAT rather than to thermal generation. As we know, the thermal generation presents a quadratic dependence of over bias, as its main effect relies on the enlargement of the depletion zones. On the contrary, TAT is expected to present an exponential dependence of over bias.[6,11] To further confirm the origin of DCR, the activation energy (E_a) is extracted from the temperature dependence, as shown in the inset of Fig. 3(b). The E_a of DCR can be extracted by fitting $\ln(\mathrm{DCR}/T^2)$ versus $1/K_BT$, where K_B is the Boltzmann constant and T is the temperature.[12] An E_a of 0.22–0.11 eV is obtained for the over bias ranging from 0.5 V to 1.5 V, far smaller than half of the band gap of 4H-SiC ($\sim$ 1.63 eV), indicating that TAT instead of thermal generation dominates the dark counts in that temperature range.[1] The E_a of PIN-0.35 and PIN-1.0 exhibit similar results, which are not shown here. Though the tunneling process includes TAT and band-to-band tunneling (BBT), the latter hardly appears in a indirect and wide bandgap semiconductor like 4H-SiC. Hence, TAT is considered to be the main origin of DCR.

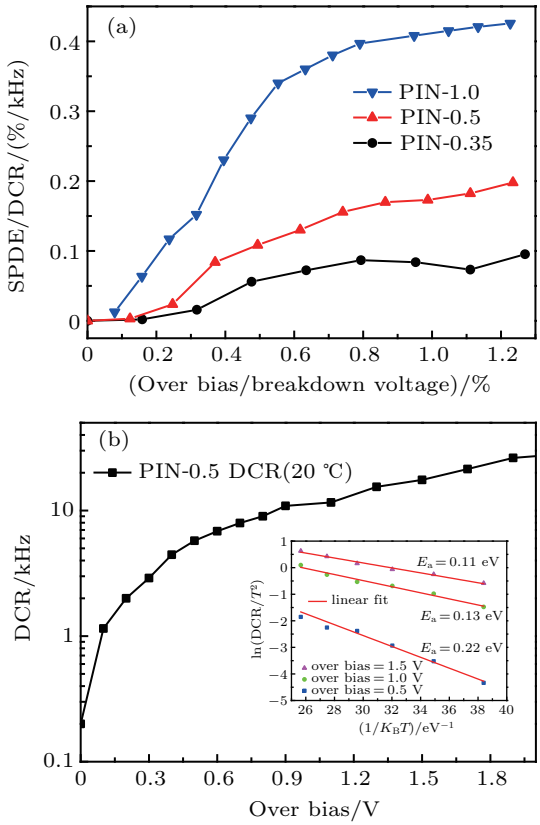


Fig. 3. (a) The SPDE/DCR characteristics measured as a function of over bias. (b) DCR–overbias characteristics of PIN-0.5 at RT. The inset shows the natural logarithm of DCR/T^2 versus $1/K_BT$ under different over biases.

The dark current characteristics of the APDs are also measured as a function of temperature ranging from RT to 140 °C. As shown in Fig. 4(a), the dark current of PIN-0.5 hardly increases as the temperature rises, demonstrating good thermal stability and quality of surface passivation. The other APDs exhibit similar dark characteristics in that temperature range, which are not shown here.

The V_{br} of the four APDs varies almost linearly as the temperature increases, and the calculated temperature coefficient increases as the i-layer thickness increases, as shown in Fig. 4(b). The V_{br} of 4H-SiC APD is regularly considered to be the voltage where an avalanche gain of 1000 is achieved. However, the gain characteristics differ from device to device, the gain-definition is not accurate enough in the analysis of device performance, especially in the calculation of the temperature coefficient. Here, V_{br} is defined as the voltage where a 10-mA dark current first appears. The DCR-definition applied here is more accurate to describe the essence of avalanche process. The temperature coefficient ranges from −2.6 mV/°C of PIN-0.1 to 18.3 mV/°C of PIN-1.0, indicating that the TAT component has been gradually replaced by the avalanche component as the i-layer thickness increases. The positive temperature coefficient of V_{br} is owing to the decrease of the mean free path of

carriers once the SiC lattice is heated, while the negative temperature coefficient is due to the thermally-induced bandgap narrowing effect which facilities the TAT process.[13] Hence, the temperature coefficient may be an effective parameter to evaluate the 4H-SiC APD TAT component.

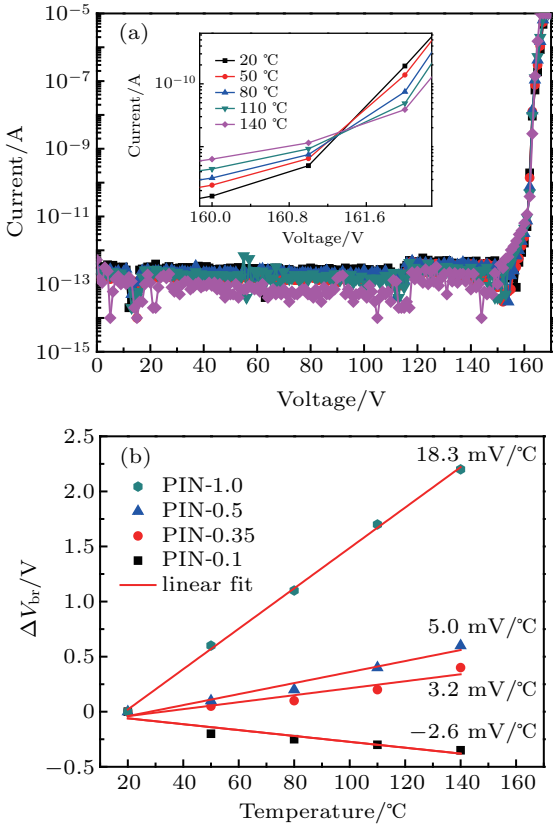


Fig. 4. (a) Dark current of PIN-0.5 measured as a function of temperature ranging from RT to 140 °C, The inset shows the dark current measured at different temperatures near the avalanche region. (b) The V_{br} variation measured as a function of temperature and the calculated temperature coefficient of the four APDs.

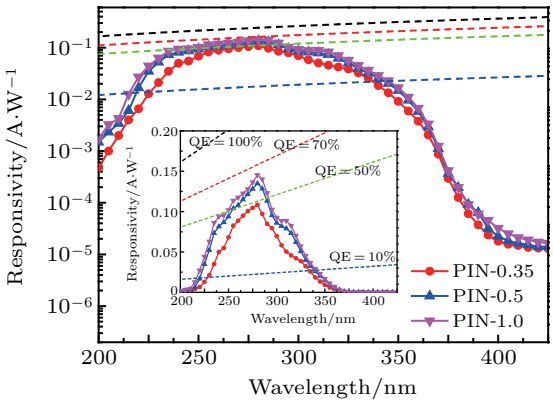


Fig. 5. The RT spectral response characteristics of PIN-0.35, PIN-0.5, and PIN-1.0 measured at 0 V. The inset shows the spectral response characteristics plotted in linear scale.

The photo-response characteristics of PIN-0.35, PIN-0.5, and PIN-1.0 are measured at 0 V, as shown in Fig. 5. The peak responsivity at 280 nm is 0.108 A/W, 0.135 A/W, and 0.145 A/W for PIN-0.35, PIN-0.5, and PIN-1.0, corresponding to a maximum external quantum efficiency (EQE) of 48%, 59%, and 65%, respectively. A high UV/visible (280 nm/400 nm) rejection ratio of more than 10^4 is obtained for the three APDs. The EQE increase from PIN-0.35 to PIN-1.0 should be caused by the thickness increase of the i-layer, which acts as an absorption region.

Although the device performance (dark current level, SPDE, and QE) improves as the intrinsic layer thickness increases, the breakdown voltage uniformity decreases. The breakdown voltage uniformity plays a vital role in industrial applications, in which the devices are utilized as linear arrays. In order to balance the overall performance of the APD devices, 0.5 μm is considered as the optimized i-layer thickness.

4. Conclusion

In this work, in order to investigate the relationship between device performance and i-layer thickness, four APDs with different i-layers are designed and fabricated. The APD with thicker i-layer is confirmed to has lower primary dark current, larger positive temperature coefficient, and higher EQE. The E_a of DCR is far small than the half of the band gap of 4H-SiC ($\sim$ 1.63 eV), indicating that the tunneling is the responsible origin of DCR. The thick i-layer could suppress the tunneling component effectively, thus bringing all the benefits to the APD performance improvement. Further optimization of device design, fabrication, and measurement will be carried out to reduce the tunneling component and analyze the origin of DCR in SiC APDs. In order to balance the overall performance of the APD devices, 0.5 μm is considered as the optimized i-layer thickness.

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