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Thermal resistance matrix representation of thermal effects and thermal design of microwave power HBTs with two-dimensional array layout*

Rui Chen(陈蕊), Dong-Yue Jin(金冬月)†, Wan-Rong Zhang(张万荣), Li-Fan Wang(王利凡), Bin Guo(郭斌), Hu Chen(陈虎), Ling-Han Yin(殷凌寒), and Xiao-Xue Jia(贾晓雪)

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Based on the thermal network of the two-dimensional heterojunction bipolar transistors (HBTs) array, the thermal resistance matrix is presented, including the self-heating thermal resistance and thermal coupling resistance to describe the self-heating and thermal coupling effects, respectively. For HBT cells along the emitter length direction, the thermal coupling resistance is far smaller than the self-heating thermal resistance, and the peak junction temperature is mainly determined by the self-heating thermal resistance. However, the thermal coupling resistance is in the same order with the self-heating thermal resistance for HBT cells along the emitter width direction. Furthermore, the dependence of the thermal resistance matrix on cell spacing along the emitter length direction and cell spacing along the emitter width direction is also investigated, respectively. It is shown that the moderate increase of cell spacings along the emitter length direction and the emitter width direction could effectively lower the self-heating thermal resistance and thermal coupling resistance, and hence the peak junction temperature is decreased, which sheds light on adopting a two-dimensional non-uniform cell spacing layout to improve the uneven temperature distribution. By taking a 2×6 HBTs array for example, a two-dimensional non-uniform cell spacing layout is designed, which can effectively lower the peak junction temperature and reduce the non-uniformity of the dissipated power. For the HBTs array with optimized layout, the high power-handling capability and thermal dissipation capability are kept when the bias voltage increases.

Keywords: heterojunction bipolar transistors (HBTs) array, thermal effects, thermal resistance matrix, thermal design

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1. Introduction

In recent years, heterojunction bipolar transistors (HBTs) array with parallel HBT cells layout has been used widely for microwave power applications[1–4] due to its high current handling capability.[5–7] However, the self-heating effect caused by the power dissipation of each HBT cell and the thermal coupling effect among the adjacent HBT cells result in an uneven temperature profile in the HBTs array. Because of the positive temperature coefficient of the emitter current, the central HBT cells with higher temperature will conduct more current and consequently generate more heat, which aggravates the thermal effects and leads to thermal breakdown or thermal runaway.[8,9]

In order to obtain more uniform temperature distribution and tackle these thermal issues, one-dimensional (along emitter width direction) layout design technologies including variation of emitter length in HBT cells[10,11] (in Fig. 1(a)) and variation of emitter spacing between HBT cells[12–15] (in Fig. 1(b)) are used widely, which could decrease the temperature difference along the emitter width direction. However, there is still a higher temperature in the center of each emitter. At the same time, the non-uniformity of the temperature profile along the emitter length direction is not reduced. In recent research, the technology of multi-emitter array (in Fig. 1(c)) is proposed to decrease the temperature difference along the emitter length direction effectively,[16,17] which shows the superior thermal properties of the HBTs array with two-dimensional parallel HBT cells layout (2-D HBTs array). However, the layout design methodology of 2-D HBTs array has not been studied.

It is known that the thermal resistance matrix ($[R_{ij}]$) could be used to represent the thermal effects of a one-dimensional HBT array,[18,19] which is helpful to design the layout of the device. However, the prior $[R_{ij}]$ representation is not applicable for the 2-D HBTs array.

In this paper, with the aid of the thermal network of a 2-D HBTs array, a new thermal resistance matrix ($[R_{ijkl}]$) is proposed, including self-heating thermal resistance (R_{ijij}) in the (i, j) HBT cell and thermal coupling resistance ($R_{ijkl(ij\neq kl)}$)

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to represent the self-heating and thermal coupling effects, respectively. The dependence of $[R_{ijkl}]$ on cell spacing along the emitter length direction (S_x) and cell spacing along the emitter width direction (S_y) is also studied respectively. Furthermore, with the aid of $[R_{ijkl}]$, the HBTs array with a novel 2-D non-uniform cell spacing layout (including non-uniform S_x and non-uniform S_y) is designed to lower the peak junction temperature, reduce the non-uniformity of the temperature profile, and hence alleviate the thermal issues of the HBTs array.

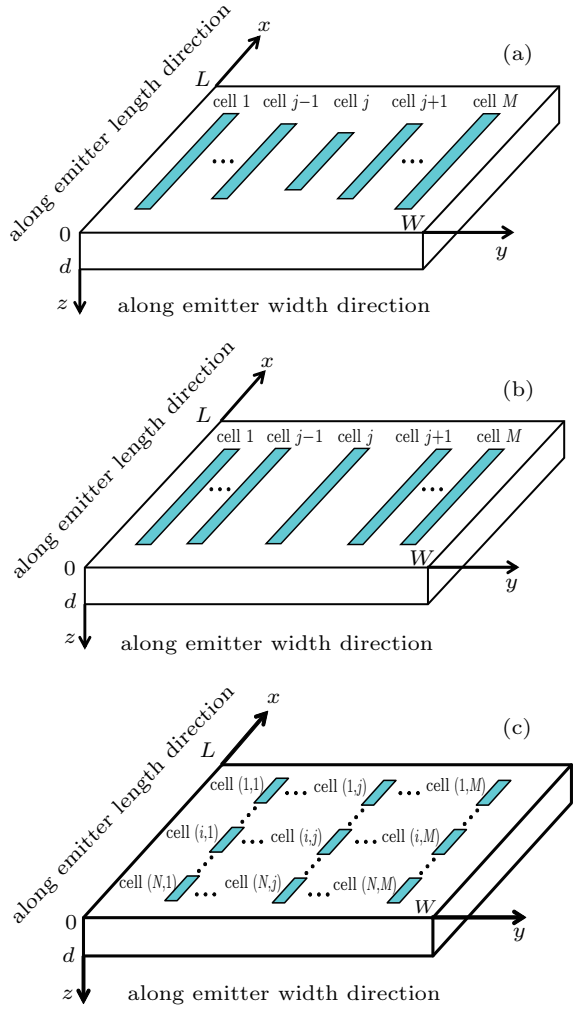


Fig. 1. Three-dimensional schematic structures of HBTs arrays with different layout designs: (a) variation of emitter length in one-dimensional layout design (M HBT cells), (b) variation of emitter spacing in one-dimensional layout design (M HBT cells), (c) two-dimensional parallel layout design ($N \times M$ HBT cells).

2. Thermal-electrical model

To account for the self-heating and the thermal coupling effects, a thermal network of 2-D HBTs array ($N \times M$ HBT cells) with a ground-referenced thermal voltage is shown in Fig. 2, where each HBT cell is assigned with a constant temperature (e.g., its average temperature).

For the (i, j) HBT cell in the thermal network, the self-heating effect can be represented as a parallel combination of R_{iji} and dissipated power (P_{ij}). The self-heating temperature rise of the (i, j) HBT cell (T_{Sij}) is obtained as $T_{Sij} = R_{iji} \times P_{ij}$. Meanwhile, the thermal coupling effect can be represented as a series thermal coupling voltage, which is a combination of the temperature rise caused by the rest HBT cells. The thermal coupling temperature rise of the (i, j) HBT cell (T_{Cij}) is obtained as

$$T_{Cij} = \sum_{k=1}^{N} \sum_{l=1}^{M} R_{ijkl} P_{kl} - R_{iji} P_{ij}, \tag{1}$$

where R_{ijkl} represents the contribution of the (k, l) HBT cell to the temperature rise of the (i, j) HBT cell, P_{kl} represents the dissipated power of the (k, l) HBT cell ($P_{kl} = I_{Ckl} V_{CE}$), I_{Ckl} is the collector current of the (k, l) HBT cell, and V_{CE} is the collector–emitter voltage.

Therefore, the peak junction temperature of the (i, j) HBT cell (T_{ij}) including the self-heating temperature rise and the total thermal coupling temperature rise is obtained as

$$T_{ij} = T_{Sij} + T_{Cij} + T_0 = \sum_{k=1}^{N} \sum_{l=1}^{M} R_{ijkl} P_{kl} + T_0. \tag{2}$$

For the 2-D HBTs array with $N \times M$ HBT cells, $[R_{ijkl}]$ is expressed as

$$[R_{ijkl}] = \left[\begin{array}{ccc|c|ccc} R_{1111} & \cdots & R_{1M11} & & R_{111M} & \cdots & R_{1M1M} \\ \vdots & \ddots & \vdots & \cdots & \vdots & \ddots & \vdots \\ R_{N111} & \cdots & R_{NM11} & & R_{N11M} & \cdots & R_{NM1M} \\ \hline & \vdots & & \ddots & & \vdots & \\ \hline R_{11N1} & \cdots & R_{1MN1} & & R_{11NM} & \cdots & R_{1MNM} \\ \vdots & \ddots & \vdots & \cdots & \vdots & \ddots & \vdots \\ R_{N1N1} & \cdots & R_{NMN1} & & R_{N1NM} & \cdots & R_{\mathrm{NMNM}} \end{array}\right]. \tag{3}$$

It is noted that there are $N \times M$ sub-thermal resistance matrices in $[R_{ijkl}]$, including $[R_{ij11}]$, …, $[R_{ij1M}]$, $[R_{ij21}]$, …, $[R_{ij2M}]$, …, $[R_{ijN1}]$, …, $[R_{ijNM}]$, where $[R_{ij11}]$ can be expressed as

$$[R_{ij11}] = \begin{pmatrix} R_{1111} & \cdots & R_{1M11} \\ \vdots & \ddots & \vdots \\ R_{N111} & \cdots & R_{NM11} \end{pmatrix}. \tag{4}$$

In this paper, the thermal model of the strained Si/SiGe HBTs array is established with ANSYS. The electrical model is established with MATLAB, which has considered the positive temperature coefficient of the collector current in each HBT cell

$$I_{Cij} = I_{C0} \exp\left\{\frac{q}{kT_0}\left[V_{BE} - \phi\left(T_{ij} - T_0\right)\right]\right\}, \tag{5}$$

where I_{Cij} is the collector current of the (i, j) HBT cell, I_{C0} is the saturation current, k is Boltzmann's constant, q is the charge of electron, V_{BE} is the base–emitter voltage, and ϕ is the negative temperature coefficient of V_{BE}.

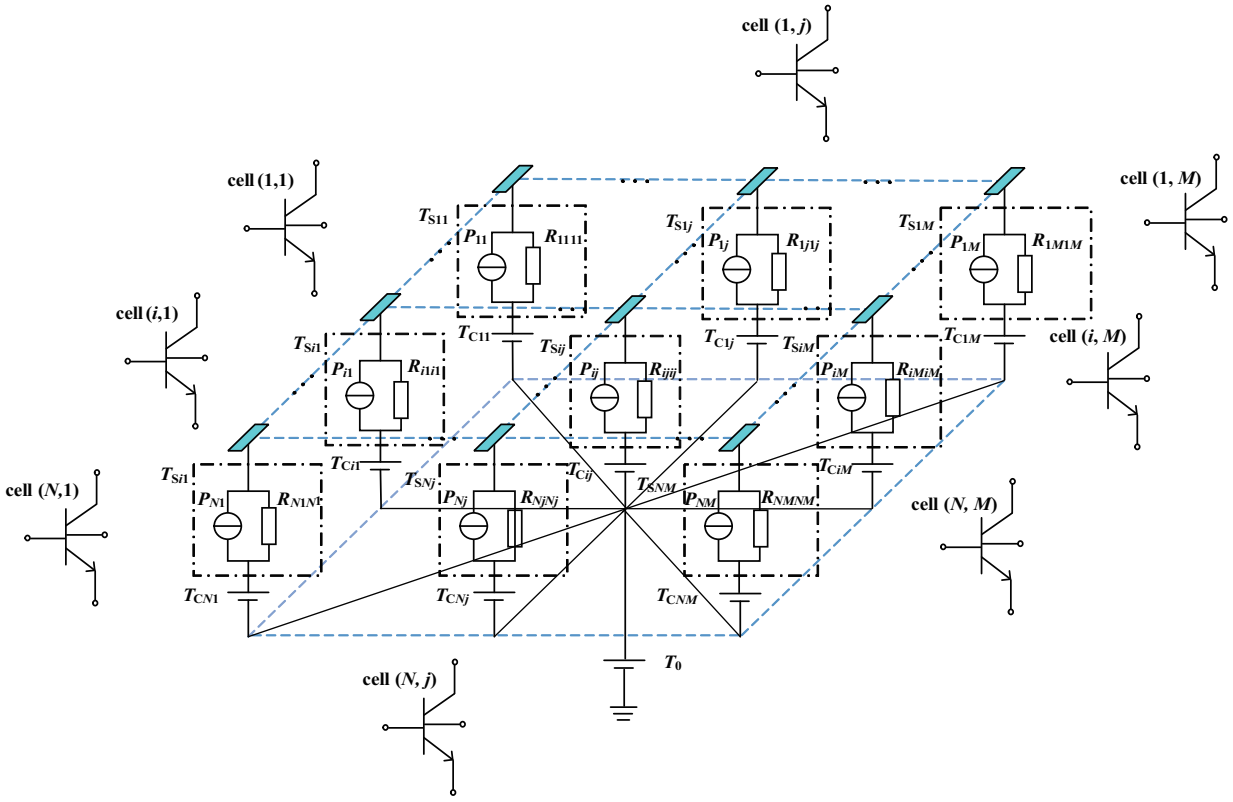


Fig. 2. Thermal network of a two-dimensional HBTs array with $N \times M$ HBT cells by taking into account the self-heating and thermal coupling effects.

As a result, the thermal-electrical model is established based on the iterative solution between ANSYS and MATLAB, and the temperature of the HBTs array (with $N \times M$ HBT cells) is first calculated under the same power level. By increasing the power of the (k, l) HBT cell (ΔP_{kl}), a new temperature distribution is calculated. Therefore, $[R_{ijkl}]$ including R_{ijij} and $R_{ijkl(ij\neq kl)}$ is obtained by using the temperature rise of the (i, j) HBT cell (ΔT_{ij}) as

$$R_{ijkl} = \Delta T_{ij}/\Delta P_{kl}. \tag{6}$$

2.1. Impact of cell spacing along emitter length direction

Take a 2×1 HBTs array for example, $[R_{ijkl}]$ is calculated, and the impact of cell spacing along the emitter length direction (S_x) on the thermal characteristics of the HBTs array is studied. The layout of the 2×1 HBTs array is shown in Fig. 3, where both the chip width (W) and the chip length (L) is 10 μm, the width (w) and the length (l) of each HBT cell is 0.12 μm and 3 μm, respectively.

The impact of S_x on R_{ijij} and $R_{ijkl(ij\neq kl)}$ is shown in Figs. 4 and 5, respectively. It can be seen that R_{ijij} decreases as S_x increases from 0.1 μm to 0.25 μm due to the increase of the heat dissipation path. However, R_{ijij} increases exponentially when S_x increases beyond 0.25 μm. It is because both the front-edge and back-edge surfaces of the chip along the emitter length direction are adiabatic, which restrict the lateral spread of the heat flow spread from the heat source to the outside. Different from R_{ijij}, $R_{ijkl(ij\neq kl)}$ keeps decreasing as S_x increases, and the trend of $R_{ijkl(ij\neq kl)}$ can be approximated by an exponential function, indicating that the effective thermal coupling exists when two cells are very close to each other.

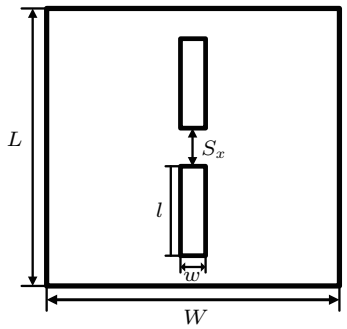


Fig. 3. The layout of a 2×1 HBTs array.

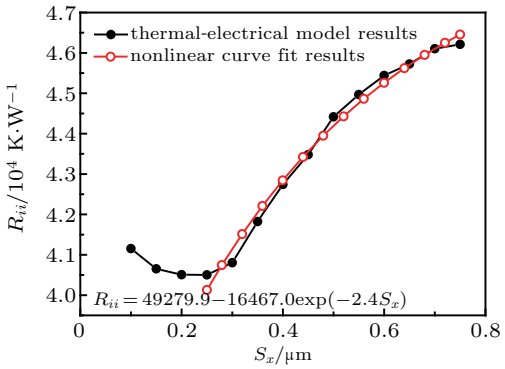


Fig. 4. The self-heating thermal resistance versus cell spacing along emitter length direction in the 2×1 HBTs array.

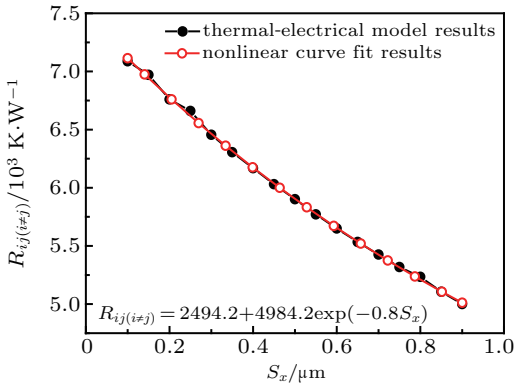


Fig. 5. The thermal coupling resistance versus cell spacing along emitter length direction in the 2×1 HBTs array.

The impact of S_x on the peak junction temperature (T_{ij}) at I_C of 0.4 mA and V_{CE} of 5 V is shown in Fig. 6, where the trend of T_{ij} is almost the same as that of R_{ijij}. It is because $R_{ijkl(ij\neq kl)}$ is far less than R_{ijij} in the $[R_{ijkl}]$ of the given 2×1 HBTs array and the trend of T_{ij} is mainly determined by R_{ijij}.

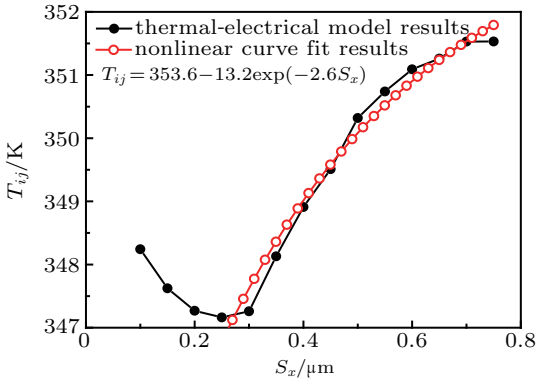


Fig. 6. The peak junction temperature versus cell spacing along emitter length direction in the 2×1 HBTs array.

2.2. Impact of cell spacing along emitter width direction

Take a 1×2 HBTs array for example, $[R_{ijkl}]$ is calculated, and the impact of cell spacing along the emitter width direction (S_y) on the thermal characteristics of the HBTs array is studied. The layout of the 1×2 HBTs array is shown in Fig. 7, where both the chip size and the size of each HBT cell is the same as those of the 2×1 HBTs array. S_y is the cell spacing along the emitter width direction.

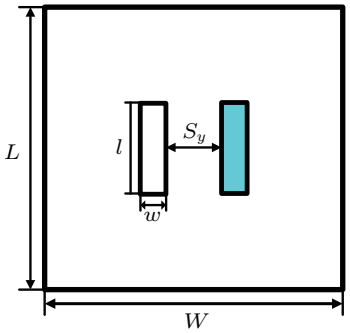


Fig. 7. The layout of a 1×2 HBTs array.

The impact of S_y on R_{ijij} and $R_{ijkl(ij\neq kl)}$ is shown in Figs. 8 and 9, respectively. It can be seen that R_{ijij} decreases linearly as S_y increases from 0.5 μm to 1.1 μm, and increases exponentially when S_y increases beyond 1.1 μm. It is because the lateral spread of heat flow is restricted by the left and right edges of the chip and the spreading angle of the heat flow is decreased, which decrease the heat dissipation path and lead to the increase of R_{ijij}. At the same time, $R_{ijkl(ij\neq kl)}$ keeps decreasing exponentially as S_y increases.

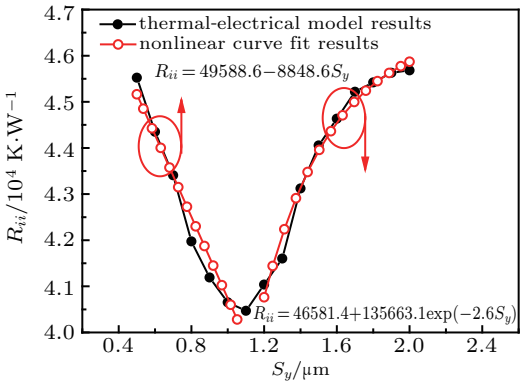


Fig. 8. The self-heating thermal resistance versus cell spacing along emitter width direction in the 1×2 HBTs array.

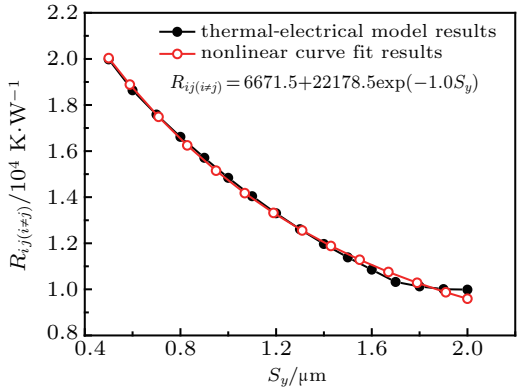


Fig. 9. The thermal coupling resistance versus cell spacing along emitter width direction in the 1×2 HBTs array.

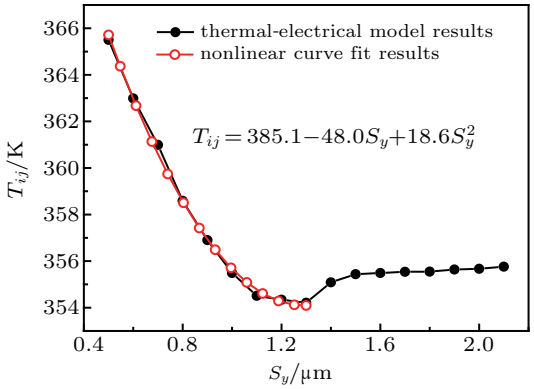


Fig. 10. The peak junction temperature versus cell spacing along emitter width direction in the 1×2 HBTs array.

Figure 10 shows the impact of S_y on T_{ij} at I_C of 0.4 mA and V_{CE} of 5 V, where T_{ij} decreases with a parabola distribution as S_y increases from 0.5 μm to 1.3 μm, and remains approximately constant when S_y increases beyond 1.3 μm. It is because $R_{ijkl(ij\neq kl)}$ is in the same order with R_{ijij}, and hence both $R_{ijkl(ij\neq kl)}$ and R_{ijij} will affect the thermal characteristics of the HBTs array.

From this analysis, it can be concluded that both S_x and S_y should be designed carefully to effectively decrease R_{ijij} and $R_{ijkl(ij\neq kl)}$. The decrease of R_{ijij} and $R_{ijkl(ij\neq kl)}$ is helpful for lowering the peak junction temperature of HBTs array, which sheds light on adopting a 2-D non-uniform cell spacing layout to improve the thermal characteristics of HBTs array.

3. Thermal-electrical model verification

Take a HBTs array with 1×20 HBT cells for example, both the simulated temperature profile along the central line across the HBT cells and the measured temperature profile reported in Ref. [15] are shown in Fig. 11. The simulated temperature profile matches well with the measured data, verifying the thermal-electrical model used in the simulations.

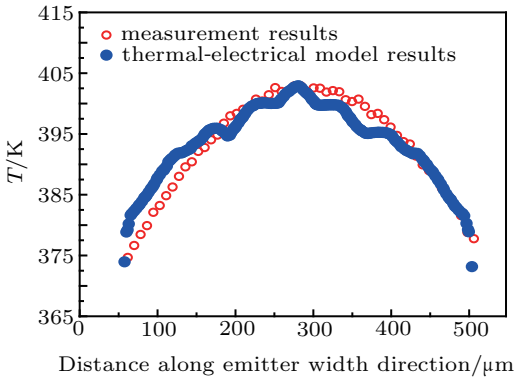


Fig. 11. Comparison of measured and simulated temperature profiles of a HBTs array with 1×20 HBT cells at $I_C = 0.6$ A and $V_{CE} = 6$ V.

4. Layout design

With the aid of the thermal-electrical model, $[R_{ijkl}]$ of a 2×6 HBTs array (array-1) with uniform cell spacings of 0.25 μm along the emitter length direction and 1.3 μm along the emitter width direction is calculated at I_C of 2.4 mA and V_{CE} of 5 V

$$[R_{ijkl}] = \left[\begin{array}{cccccc|c|cccccc} 44721 & 10711 & 5088 & 2739 & 1574 & 1021 & \cdots & 1030 & 1581 & 2739 & 5087 & 10771 & 44716 \\ 7688 & 5558 & 3756 & 2129 & 1295 & 826 & \cdots & 830 & 1261 & 2193 & 3602 & 5594 & 7693 \\ \hline 7627 & 5423 & 3702 & 2129 & 1295 & 826 & \cdots & 824 & 1241 & 2128 & 3602 & 5594 & 7693 \\ 44611 & 10673 & 4980 & 2739 & 1574 & 1021 & \cdots & 1025 & 1598 & 2693 & 5087 & 10770 & 44720 \end{array}\right]. \quad (7)$$

The detail profile of $[R_{ijkl}]$ in array-1 is shown in Fig. 12.

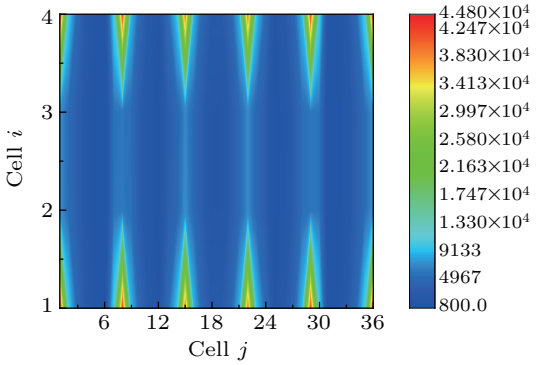


Fig. 12. Profile of thermal resistance matrix $[R_{ijkl}]$ (K/W) in the 2×6 HBTs array with uniform cell spacing (array-1) at I_C of 2.4 mA and V_{CE} of 5 V.

At the same time, iterations are used to calculate T_{ij} and P_{kl} of array-1. First, it is assumed that there is an even collector current distribution across all HBT cells. Due to the thermal effects, the temperature of each HBT cell can be calculated with a temperature rise different from the others'. Because of the positive temperature coefficient of I_{Cij} in Eq. (5), the collector current (I_{Cij}) as well as the dissipated power (P_{kl}) of each HBT cell is redistributed and leads to a new distribution of T_{ij}. The above steps are iterated until the final steady-state solutions are achieved. The steady-state results of P_{kl} in array-1 are shown in Fig. 13. The temperature profile of array-1 is shown in Fig. 14.

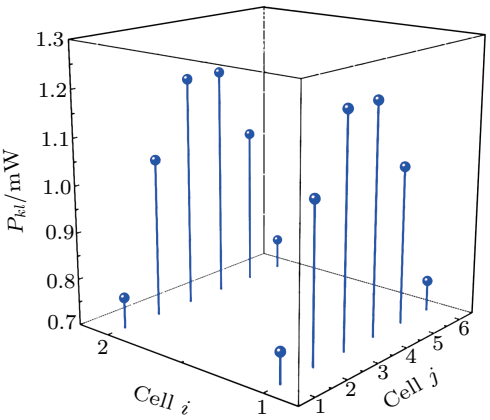


Fig. 13. The distribution of the dissipated power (P_{kl}) in the 2×6 HBTs array with uniform cell spacing (array-1) at I_C of 2.4 mA and V_{CE} of 5 V.

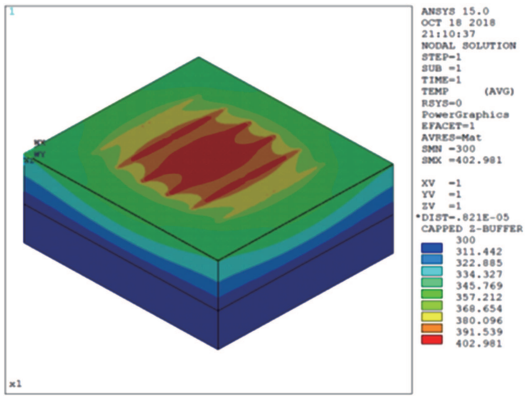


Fig. 14. Temperature profile of the 2×6 HBTs array with uniform cell spacing (array-1) at I_C of 2.4 mA and V_{CE} of 5 V.

In order to improve the uniformity of the P_{kl} distribution and lower the temperature of the central HBT cells, both of cell spacing along the emitter length direction (S_x) and cell spacing along the emitter width direction (S_y) are designed carefully. For S_x, the spacings between the central cells should be increased significantly to lower R_{ijij}, because $R_{ijkl(ij\neq kl)}$ is far less than R_{ijij} for the cells along the emitter length direction and the temperature difference is mainly determined by R_{ijij}. For S_y, the spacings between the central cells are increased moderately to lower both R_{ijij} and $R_{ijkl(ij\neq kl)}$. It is because $R_{ijkl(ij\neq kl)}$ is in the same order with R_{ijij} for the cells along the emitter width direction and the temperature difference is determined by both R_{ijij} and $R_{ijkl(ij\neq kl)}$. Moreover, the temperature difference will remain approximately constant as S_y increase to a certain distance. At the same time, considering that the outside cells are more convenient to spread heat, both S_x and S_y of the outside cells can be decreased to keep the total cell spacing unchanged. A 2×6 HBTs array (array-2) with non-uniform S_x and non-uniform S_y is designed under the same power density of array-1. The detail values of S_x and S_y of the two types of HBTs arrays are presented in Tables 1 and 2, respectively. The layouts of the two types of HBTs arrays are also presented in Fig. 15. Array-2 also has an identical vertical structure, total emitter area, and total cell spacing to those of array-1. The detail profile of $[R_{ijkl}]$ in array-2 is shown in Fig. 16. For array-2, not only R_{ijij} of each HBT cell but also $R_{ijkl(ij\neq kl)}$ in the central HBT cells decrease obviously, when compared with those of array-1. Take the central (1, 3) HBT cell for example, $[R_{ij13}]$ of the two types of HBTs arrays is respectively given by

$$[R_{ij13}]_{\text{array}-1} = \begin{pmatrix} 5349 & 9826 & 40992 & 9202 & 4634 & 2828 \\ 3667 & 4907 & 7590 & 5153 & 3239 & 2005 \end{pmatrix}, \quad (8)$$

$$[R_{ij13}]_{\text{array}-2} = \begin{pmatrix} 5780 & 10203 & 35516 & 7779 & 4120 & 2589 \\ 3146 & 3901 & 4270 & 3244 & 2317 & 1709 \end{pmatrix}. \quad (9)$$

It is shown that R_{1313} is lowered by 5476 K/W with an improvement of 13.4% and $R_{ij13(ij\neq 13)}$ is also improved from 8.5% to 43.7%.

Table 1. Cell spacing along emitter length direction of the two types of HBTs arrays.

	S_{x1}/μm	S_{x2}/μm	S_{x3}/μm	S_{x4}/μm	S_{x5}/μm	S_{x6}/μm
Array-1	0.25	0.25	0.25	0.25	0.25	0.25
Array-2	0.1	0.25	0.4	0.4	0.25	0.1

Table 2. Cell spacing along emitter width direction of the two types of HBTs arrays.

	S_{y1}/μm	S_{y2}/μm	S_{y3}/μm	S_{y4}/μm	S_{y5}/μm
Array-1	1.3	1.3	1.3	1.3	1.3
Array-2	1.1	1.3	1.7	1.3	1.1

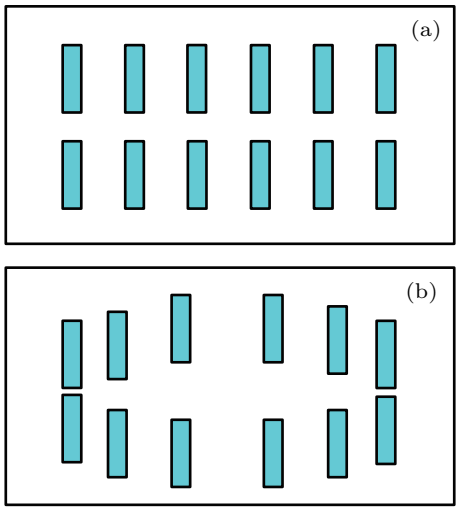


Fig. 15. Layouts of 2×6 HBTs arrays (a) with uniform S_x and uniform S_y (array-1), (b) with non-uniform S_x and non-uniform S_y (array-2).

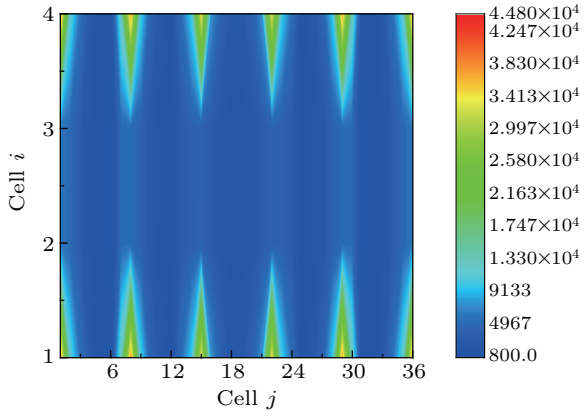


Fig. 16. Profile of thermal resistance matrix $[R_{ijkl}]$ (K/W) in the 2×6 HBTs array with non-uniform S_x and non-uniform S_y (array-2) at I_C of 2.4 mA and V_{CE} of 5 V.

The correlated P_{kl} and the temperature profile of array-2 are shown in Figs. 17 and 18, respectively. For array-2, the maximum power level difference of the HBT cells is decreased by 38.7% when compared with that of array-1. As a result,

array-2 has a lower peak junction temperature of 407.7 K, which is lowered by 4.2% and the uniformity of the cell temperature is improved by 46.9%.

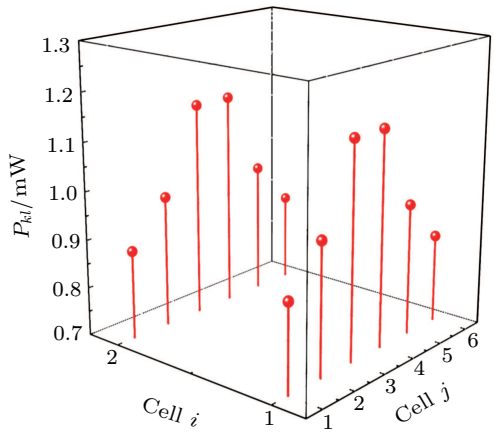


Fig. 17. The distribution of the dissipated power (P_{kl}) in the 2×6 HBTs array with non-uniform cell spacing (array-2) at I_C of 2.4 mA and V_{CE} of 5 V.

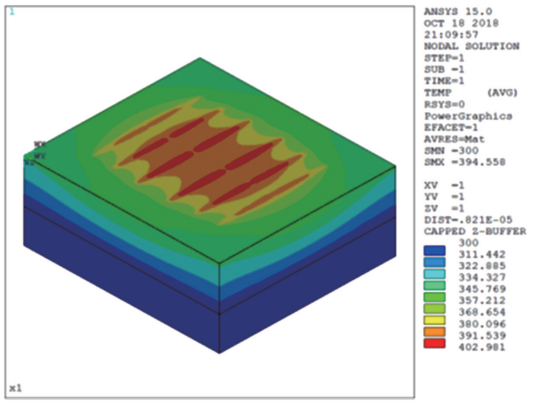


Fig. 18. Temperature profile of the 2×6 HBTs array with non-uniform cell spacing (array-2) at I_C of 2.4 mA and V_{CE} of 5 V.

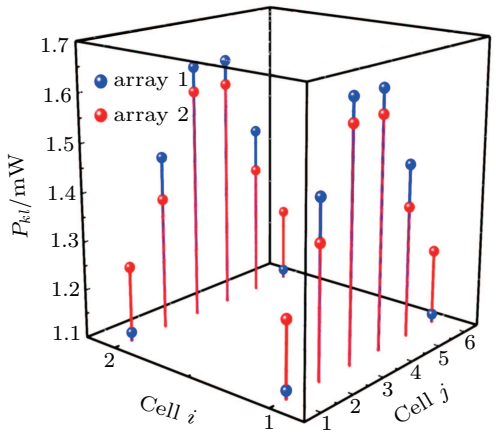


Fig. 19. Power levels at $V_{CE} = 7$ V for HBTs array with uniform cell spacing (array-1) and HBTs array with varying cell spacing (array-2).

As the collector–emitter voltage V_{CE} is increased to 7 V, the calculated correlated P_{kl} and T_{ij} of the HBT cells in the two arrays are shown in Figs. 19 and 20, respectively. For array-2, the maximum power level difference is decreased by 36.5%, the peak junction temperature is lowered by 20.2 K, and the uniformity of the cell temperature is improved by 52.7%, when compared with those of array-1. It indicates that, for the HBTs array with designed non-uniform cell spacing, the high power-handling capability and thermal dissipation capability are kept when V_{CE} increases.

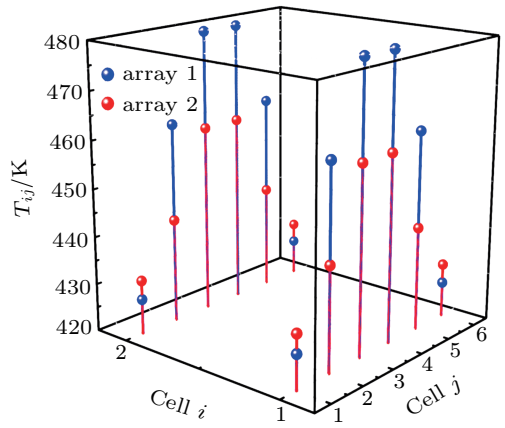


Fig. 20. The peak junction temperature profiles at heat source surface of HBTs array with uniform cell spacing (array-1) and HBTs array with varying cell spacing (array-2) at $V_{CE} = 7$ V.

5. Conclusion

To represent the self-heating effect and thermal coupling effect of the HBTs array with $N \times M$ HBT cells, $[R_{ijkl}]$ including R_{ijij} and $R_{ijkl(ij\neq kl)}$ is presented in this paper. With the aid of a thermal network, the thermal-electrical model is established based on the iterative solution between ANSYS and MATLAB, and $[R_{ijkl}]$ of the HBTs array are calculated. The dependence of $[R_{ijkl}]$ and peak junction temperature T_{ij} on cell spacing (S_x and S_y) is also investigated. For HBT cells along the emitter length direction, T_{ij} decreases as S_x increases from 0.1 μm to 0.25 μm, and T_{ij} increases exponentially when S_x increases beyond 0.25 μm. The trend of T_{ij} versus S_x is mainly determined by the variation of R_{ijij}. However, for HBT cells along the emitter width direction, T_{ij} decreases as S_y increases from 0.5 μm to 1.3 μm, and T_{ij} remains approximately constant when S_y increases beyond 1.3 μm, where the trend of T_{ij} versus S_y is determined by both R_{ijij} and $R_{ijkl(ij\neq kl)}$. As a result, the moderate increase of S_x and S_y could effectively lower R_{ijij} and $R_{ijkl(ij\neq kl)}$ as well as T_{ij}. Furthermore, by taking a 2×6 HBTs array for example, the 2-D non-uniform cell spacing layout (including non-uniform S_x and non-uniform S_y) is designed. For the optimized HBTs array, the peak junction temperature is lowered by 4.2%, the uniformity of the cell temperature is improved by 46.9%, and the maximum power level difference of the HBT cells is decreased by 38.7%, when compared with those of the uniform device. At the same time, the high power-handling capability and thermal dissipation capability are kept as V_{CE} increases from 5 V to 7 V, indicating that

the 2-D non-uniform cell spacing layout is a useful method to design power HBTs arrays for high thermal stability.

References

[1] Hadi R A, Grzyb J, Heinemann B and Pfeiffer R 2013 *IEEE J. Solid-state Circuits* **48** 2002

[2] Metzger A G, D'Alessandro V, Rinaldi N and Zampardi P J 2013 *Microelectron. Reliab.* **53** 1471

[3] Hettrich H and Möller M 2016 *IEEE J. Solid-state Circuits* **51** 2006

[4] Vincenzo D A, Antonio P C, Lorenzo C, Brian M and Peter J Z 2018 *Proceedings of EuroSimE, Toulouse*, France, p. 1

[5] Sun Y B, Fu J, Wang Y D, Zhou W, Zhang W and Liu Z H 2016 *Chin. Phys. B* **25** 048501

[6] Fu Q, Zhang W R, Jin D Y, Zhao Y X and Wang X 2016 *Chin. Phys. B* **25** 124401

[7] Sun Y B, Li X J, Zhang J Z and Shi Y L 2017 *Chin. Phys. B* **26** 098502

[8] Liou L L, Bayraktaroglu B and Huang C I 1996 *Solid-State Electron.* **39** 165

[9] Sevimli O, Parker A E, Fattorini A P and Mahon S J 2013 *IEEE Trans. Electron. Devices* **60** 1632

[10] Koenig E, Seiler U, Schneider J, Erben U and Schumacher H 1995 *Solid-State Electron.* **38** 775

[11] Jin D Y, Zhang W R, Shen P, Xie H Y, Li J, Gan J N, Huang L, Hu N and Huang Y W 2008 *2008 International Conference on Microwave and Millimeter Wave Technology*, April 21–24, 2008 Nanjing, China, p. 166

[12] McAlister S P, McKinnon W R, Kovacic S J and Lafontaine H 2004 *Solid-State Electron.* **48** 2001

[13] Jin D Y, Zhang W R, Xie H Y, Chen L, Shen P and Hu N 2009 *Microelectron. Reliab.* **49** 382

[14] Chen L, Zhang W R, Jin D Y, Shen P, Xie H Y, Ding C B, Xiao Y, Sun B T and Wang R Q 2011 *Chin. Phys. B* **20** 018501

[15] Chen L, Zhang W R, Jin D Y, Xie H Y, Xiao Y, Wang R Q and Ding C B 2011 *Acta Phys. Sin.* **60** 078501 (in Chinese)

[16] Marano I, D'Alessandro V and Rinaldi N 2009 *Solid-State Electron.* **53** 297

[17] Zhao X Y, Jin D Y, Zhang W R, Wang X, Guo Y L and Wang D 2016 *5th International Symposium on Next-Generation Electronics*, May 4–6, 2016 Taiwan, China, p. 1

[18] Jin D Y, Zhang W R, Chen L, Fu Q, Xiao Y, Wang R Q and Zhao X 2011 *Chin. Phys. B* **20** 064401

[19] Lehmann S, Zimmermann Y, Pawlak A and Schröter M 2014 *IEEE Trans. Electron. Devices* **61** 3676