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Citation: Chin. Phys. B . 2019, 28(8): 088502. **doi:** 10.1088/1674-1056/28/8/088502
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Negative gate bias stress effects on conduction and low frequency noise characteristics in p-type poly-Si thin-film transistors*

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(Received 24 January 2019; revised manuscript received 17 May 2019; published online 9 July 2019)

The instability of p-channel low-temperature polycrystalline silicon thin film transistors (poly-Si TFTs) is investigated under negative gate bias stress (NBS) in this work. Firstly, a series of negative bias stress experiments is performed, the significant degradation behaviors in current–voltage characteristics are observed. As the stress voltage decreases from −25 V to −37 V, the threshold voltage and the sub-threshold swing each show a continuous shift, which is induced by gate oxide trapped charges or interface state. Furthermore, low frequency noise (LFN) values in poly-Si TFTs are measured before and after negative bias stress. The flat-band voltage spectral density is extracted, and the trap concentration located near the Si/SiO_2 interface is also calculated. Finally, the degradation mechanism is discussed based on the current–voltage and LFN results in poly-Si TFTs under NBS, finding out that Si–OH bonds may be broken and form Si^* and negative charge OH^- under negative bias stress, which is demonstrated by the proposed negative charge generation model.

Keywords: polycrystalline silicon, thin film transistor, negative bias stress, low frequency noise

PACS: 85.30.Tv, 73.40.Qv, 85.40.Qx **DOI:** 10.1088/1674-1056/28/8/088502

1. Introduction

As switching elements and peripheral circuits, low-temperature polysilicon thin film transistors (poly-Si TFTs) have been widely used in high-performance active matrix liquid crystal displays (AMLCD) and active matrix organic light emitting diodes (AMOLED).[1,2] During its application in the display field, poly-Si TFTs may be exposed to various environments, such as temperature, bias stress, *etc*.,[3–6] thereby changing the characteristics of poly-Si TFTs and further affecting the performance of peripheral circuits.[7] Therefore, its reliability is the key issue for circuit application of TFT.

As previously reported,[8–15] the reliability of poly-Si under negative bias stress has been studied, and the degradation of the transfer characteristics in poly-Si TFT is explained by different mechanisms as being carrier trapping/de-trapping. However, there are few papers about distinguishing between the contribution of stress-induced oxide trapped charges and the contribution of interface states to the threshold voltage shift in poly-Si TFT. Besides, the dominant mechanism of the poly-Si TFT under a gate bias stress has not been fully discussed.

As a non-destructive reliability characterization method, the low frequency noise (LFN) measurement has been widely used to evaluate and select semiconductor devices.[16,17] Based on the LFN results, the density of traps located near the Si/SiO_2 interface can be extracted, which is useful in analyzing the degradation mechanism in poly-Si TFT.

In this paper, a series of experiments is carried out to study the instability of poly-Si TFTs under NBS. The dependence of degradation characteristics on the bias voltage is analyzed. In addition, the contributions of stress-induced oxide trapped charges and interface states to the threshold voltage shift are distinguished. Moreover, the values of the LFN are extracted before and after NBS. The density of traps located near the Si/SiO_2 interface is extracted, and the spatial distribution of trapped charges in gate oxide is also calculated.

2. Device structure and experimental details

2.1. Device structure

The devices under test are p-channel LTPS-TFTs with a top-gate structure. Firstly, the amorphous silicon thin film was shaped into a polysilicon thin film by the ELA process. Then, the poly-Si layer was patterned into active islands by use of wet etch, followed by a 50-nm-thick SiO_2 deposition using the LPCVD. The low-temperature oxide (LTO) was used as the gate dielectric. Subsequently, a 300-nm-thick Al was sputtered and patterned into gate electrodes. Boron at a dose of 4×10^{15} cm^2 was implanted into the source and drain by

*Project supported by the National Natural Science Foundation of China (Grant No. 61574048), the Pearl River Science and Technology Nova Program of Guangzhou City, China (Grant No. 201710010172), the International Science and Technology Cooperation Program of Guangzhou City (Grant No. 201807010006), the International Cooperation Program of Guangdong Province, China (Grant No. 2018A050506044), and the Opening Fund of Key Laboratory of Silicon Device Technology, China (Grant No. KLSDTJJ2018-6).

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self-aligned technology. Before defining the contact holes, a passivation layer was formed by the LPCVD depositing 500-nm SiO_2. The 700-nm thick Al-1% Si was used as the metal leads. Finally, the devices were sintered in a synthesis gas at 420 °C for 30 min. In this experiment, the device channel width and length are 12 μm and 10 μm respectively, and the measured unit area gate oxide capacitance (C_{ox}) is about 6.91×10^{-8} F/cm^2.

2.2. *I–V* characteristic and extracted parameters

In this work, the transfer characteristics were measured by using Agilent B1500, and the low frequency noise values were measured using Keysight E4727A.[18,19]

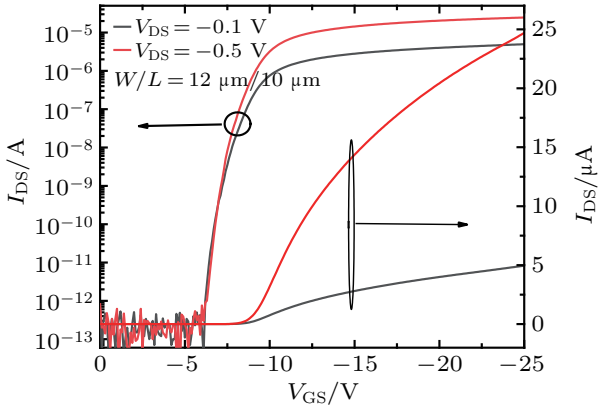


Fig. 1. Transfer characteristics of poly-Si TFT.

The transfer characteristics of poly-Si TFTs are shown in Fig. 1, which were measured at $V_{DS} = -0.1$ V. The extracted threshold voltage (V_{th}) was measured to be about −8.79 V using the linear extrapolation method. The field effect mobility (μ_{FE}) was about 45 cm^2·V^{-1}·s^{-1}. Moreover, the extracted sub-threshold swing (SS) was −0.34 V/decade, which was defined as the reciprocal of the slope of the log(I_{DS})–V_{GS} curve in the sub-threshold region.

3. Influences of NBS on *I–V* and low frequency noise characteristics

3.1. Influence on *I–V* characteristics

Figure 2 shows the measured transfer characteristics of poly-Si TFTs under NBS when V_{GS} is −37 V, which shows that the threshold voltage continuously shifts with the stress time increasing, and the sub-threshold slope also slightly increases. By using the linear extrapolation method, V_{TH} was extracted from −8.32 V to −11.02 V after the negative bias stress had been applied for 5000 s.

Four different bias stress experiments were carried out with the same stress time, and the values of negative bias stress voltage (V_{GS}) were −25 V, −29 V, −33 V, and −37 V, respectively. Figure 3 shows a linear relationship between ΔV_{TH} and stress time in the log-log coordinate system, which indicates that the degradation behaviors have a strong correlation with the stress time and stress voltage. It is consistent with previous investigations in Refs. [12], [20], and [21]. Like NBS degradation of MOSFETs, the shift of V_{TH} can be modeled as[14,20]

$$-\Delta V_{th} \propto t^n \exp\left(-\frac{E_a}{KT}\right) \exp\left(\frac{qaE_{ox}}{KT}\right), \tag{1}$$

where t is the stress time, n is the time exponent, E_a is the activation energy, $E_{ox} \approx V_{GS}/t_{ox}$ (t_{ox} is the gate oxide thickness), and a is the acceleration distance of electron ($a \approx 3.8$ Å).[22] As shown in Fig. 3, ΔV_{th} follows a power-law dependence on the stress time. The time exponent varies from 0.26 to 0.32 with the increasing of bias voltage, which is extracted from the slope of the fitted line. The results were consistent with previous reports about bulk MOSFETs[12] and poly-Si TFT,[21] where the typical value of n is between 1/4 and 1/3.[23]

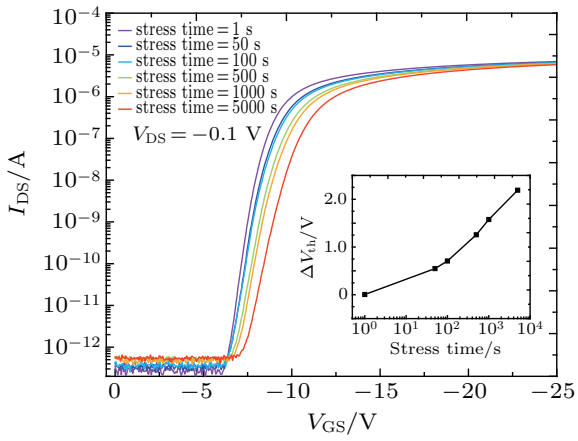


Fig. 2. Transfer characteristics of poly-Si TFT measured under different stress times.

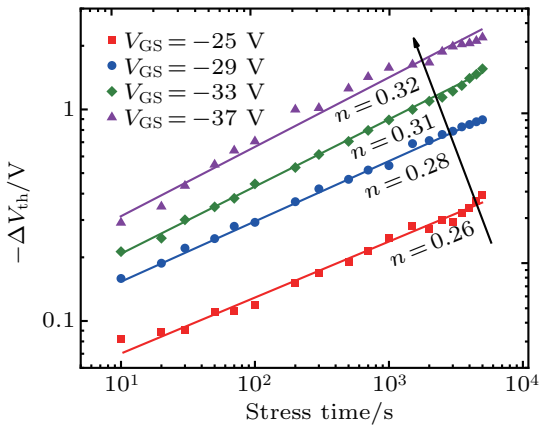


Fig. 3. Log–log plot of ΔV_{th} *versus* stress time in poly-Si TFTs with different bias stress voltages.

Meanwhile, the normalized μ_{FE} decreases and SS increases with stress time increasing as shown in Fig. 4, which is attributable to the carrier trap in the gate oxide and the generation of interface states near the Si/SiO_2 interface.[24] The result indicates that more interface states may be induced in the channel, which leads the sub-threshold swing to increase.

The relationship between the SS and the interface state density (D_{it}) can be expressed as[25]

$$\Delta SS = 2.3\frac{KT}{q}\frac{q\Delta D_{it}}{C_{ox}}, \tag{2}$$

where $\Delta D_{it} = \Delta N_{it}/\Phi_f$ (Φ_f is about 0.35 eV in this work).

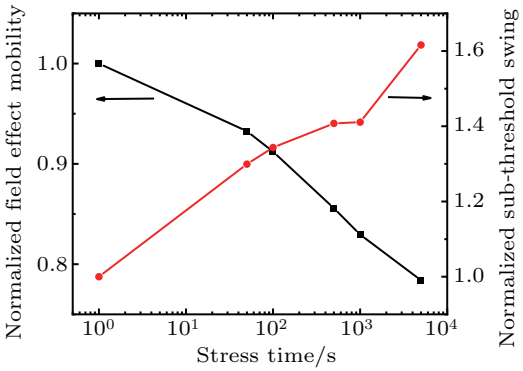


Fig. 4. Variations of normalized hole field effect mobility and normalized sub-threshold swing in the poly-Si TFTs when stress voltage is −37 V.

Besides, as the stress time increases, the interface state traps cause the average free time of carriers to decrease and further to result in the decline of carrier field effect mobility. The variation of the field effect mobility can be calculated from[25]

$$\mu_{FE} = \frac{\mu_0}{1+\eta\Delta N_{it}}, \tag{3}$$

where μ_0 is the hole field effect mobility before stress and η is a fitting parameter. According to Eq. (3), the variation of interface states has a considerable influence on carrier mobility.

According to the above description about the device fabrication process, the low-temperature oxide (LTO) was used as the gate dielectric of DUT, which may be sensitive to moisture exposure. As reported in Ref. [26], molecular H_2O may sink into the gate oxide layer at an opportune state, which may be induced ≡ SiOH groups as expressed by the simplified equation[13]

$$H_2O + \equiv SiOSi \equiv \leftrightarrow \equiv Si - OH + OH - Si \equiv . \tag{4}$$

In this paper, an assumption was made that a lot of ≡ SiOH groups are induced in the gate oxide or near the channel interface. Under the negative bias stress, carriers leaped over the surface barrier, and then broke the Si–OH bonds with disassociation energy of above 1.2 eV, resulting in the generation of Si* and negative charge OH^-. The Si* groups formed into interface states, and the partial OH^- groups were captured by oxide traps, thus forming into the fixed negative charges in the gate oxide layer. A negative charge generation model is presented to expound the process[11] as shown in Fig. 5.

In addition, as previously reported,[11,27] the impact ionization phenomenon is more accessibly induced under higher negative bias stress, which further resulted in localized states in the gate oxide or near the channel interface. Therefore, the degradation behaviors becomes more evident as the gate voltage increases as shown in Figs. 2–4.

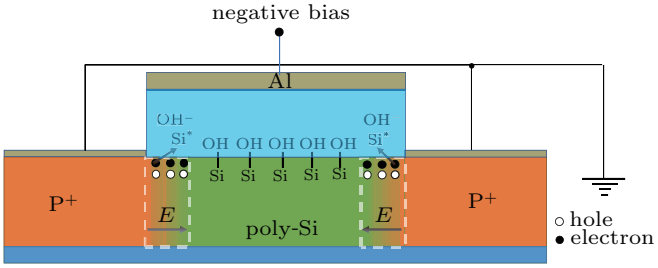


Fig. 5. Schematic illustration of negative charge generation model in poly-Si TFT.

As reported in Refs. [8]–[15] in the NBS degradation of poly-TFTs, the shift of the threshold voltage may be affected by both fixed charges in gate oxide and interface states, and it can be expressed as[28,29]

$$-\Delta V_{th} = \Delta V_{it} + \Delta V_{ox} = q\Delta N_{it}/C_{ox} - q\Delta N_{ox}/C_{ox} \tag{5}$$

and

$$N_{it} = [(SS/\ln 10)(q/KT) - 1](C_{ox}/q). \tag{6}$$

According to Eq. (5), the contributions of stress-induced charges OH^- (ΔV_{ox}) and interface states (ΔV_{it}) to V_{TH} can be divided. Based on Eq. (6), the ΔN_{ox} and ΔN_{it} can be calculated, and the results are plotted in Fig. 6. The results indicate that stress-induced interface states have more contributions to the threshold voltage shift than the stress-induced oxide trapped charges. It is determined that the variations of V_{TH} are dominated by the stress-induced Si* groups in the Si/SiO_2 interface.

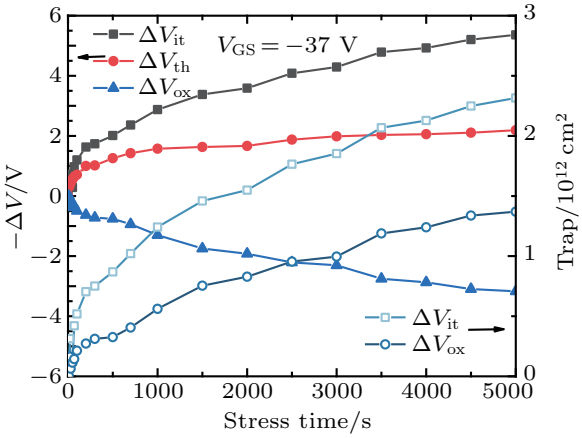


Fig. 6. Plots of separation of stress-induced oxide trapped charges and interface states versus time.

The variations of N_{it} and N_{ox} are presented in Fig. 7, under different stress voltages. ΔN is the difference between ΔN_{it} and ΔN_{ox}, which increases with stress increasing voltage. It further shows that N_{it} dominates the degradation of poly-Si TFTs more at a higher stress voltage.

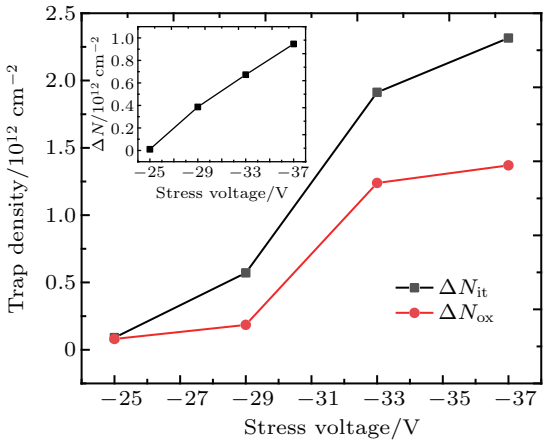


Fig. 7. Variations of trap density *versus* stress voltage ($\Delta N = \Delta N_{\rm it} - \Delta N_{\rm ox}$).

3.2. Low frequency noise characters

As reported in Refs. [30]–[32] several theories can be used to explain the origin of $1/f$ noise: the carrier number fluctuation (ΔN) model, the mobility fluctuation ($\Delta\mu$) model and carrier number with correlated mobility fluctuation (ΔN–$\Delta\mu$) model. As proposed by Ghibaudo *et al.*,[32] in the ΔN–$\Delta\mu$ model the variation of mobility induced by the fluctuation of interfacial charges is considered. Therefore, it provides a general description of LFN in various actual cases.

The above models have considered the noise related to carrier number fluctuations due to the trapping process in oxide traps. As reported by Dimitriadis[33] and Wang,[34] the measured noise under higher drain current intensity can be well described by the use of ΔN–$\Delta\mu$ model. However, the measured excess noise under low drain current intensity may be dominated by the trapping process in the grain boundary.[33,34] Therefore, it should be modeled by considering the grain boundary effect.[34]

As reported in Refs. [8]–[15], the variation of grain boundary trap is less related to NBS effect. In order to simplify the following calculations, the classical ΔN–$\Delta\mu$ model is used in this paper.

To further investigate the low frequency noise in these poly-Si TFTs, the curves of drain current power spectral densities *versus* the drain current are plotted in Fig. 8. According to the classical ΔN–$\Delta\mu$ model, the normalized drain current spectral density ($S_{\rm ID}/I_{\rm DS}$) can be given by[33,35–37]

$$\frac{S_{\rm ID}}{I_{\rm DS}} = \left(1 \pm \alpha_{\rm c}\mu_{\rm eff}C_{\rm ox}\frac{I_{\rm DS}}{g_{\rm m}}\right)\frac{g_{\rm m}^2}{I_{\rm DS}^2}S_{\rm Vfb}, \tag{7}$$

where $\alpha_{\rm c}$ is the fitting parameter which may be related to the Coulomb scattering, $g_{\rm m}$ is the transconductance, and $S_{\rm Vfb}$ is the flat band voltage spectral density. Due to uniformly distributed traps in the oxide, $S_{\rm Vfb}$ can be expressed by[33,38]

$$S_{\rm Vfb} = \frac{q^2KT\lambda N_{\rm t}}{WLC_{\rm ox}^2 f}, \tag{8}$$

where $N_{\rm t}$ is the trap state density near the Si/SiO2 interface (in units $\rm cm^{-3}{\cdot}eV^{-1}$), which includes oxide traps, interface states and border traps, and λ is the tunnel attenuation distance (about 0.1 nm in DUT). Based on Eq. (7), $S_{\rm Vfb}$ can be extracted from Fig. 8. Furthermore, based on Eq. (8), the normalized $N_{\rm t}$ is plotted in Fig. 9. Those increases further reveal that more localized states and trapped charges are induced after NBS.

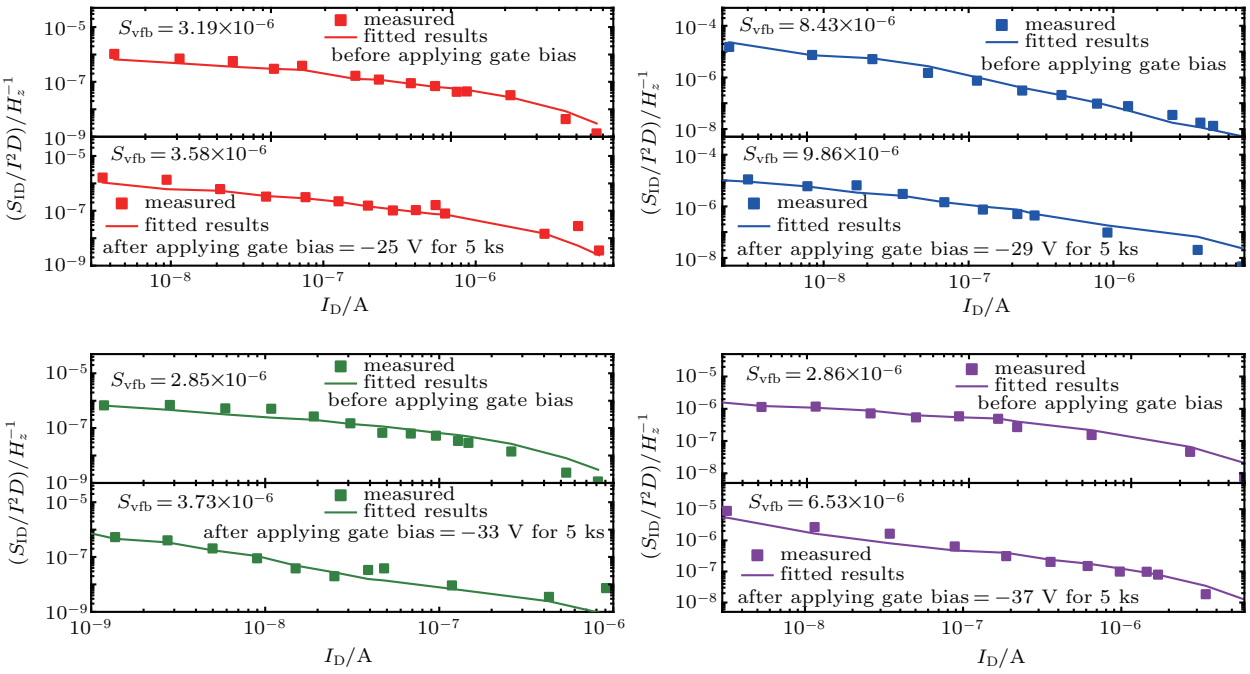


Fig. 8. Curves of normalized noise *versus* drain current power spectral density before and after NBS ($V_{\rm DS} = -0.5$ V).

Note that here in Eq. (7) the effect of the grain boundary trap on the low frequency noise is not taken into consideration. Therefore, the excess noise observed in the low drain current of poly-Si TFT cannot be well described by using Eq. (7).[33,34] In addition, the grain boundary trap related degradation phenomenon cannot be evaluated by using Eq. (7).[33,34] More accurate noise models should be adopted, which were proposed by Dimitriadis[33] and Wang.[34] The trapping and de-trapping of carriers tunneling from the inversion layer to the oxide traps near the interface cause $1/f$ noise. Therefore, based on the charge tunneling principle, the tunneling distance is affected by the time constant ($\tau = 1/2\pi f$).[36] In order to have a qualitative spatial distribution of traps in the gate oxide, the relationship between frequency and tunneling distance can be expressed as follows:[36,38]

$$\frac{1}{2\pi f} = \tau_0 \exp(\alpha_t x), \tag{9}$$

where τ_0 (about 10^{-10} s) is the time constant, x is the tunneling distance, α_t is the tunneling attenuation coefficient (about 10^8 cm^{-1}). The plot of calculated density of trapped charges *versus* depth before and after stress experiment are graphed in Fig. 10, those results are in agreement with the previous discussion about the variations of the transfer characteristics.

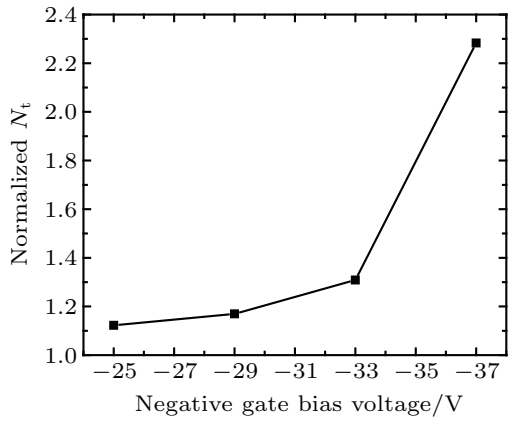


Fig. 9. Normalized N_t (defined as $N_{t_after}/N_{t_initial}$) *versus* negative gate bias voltage.

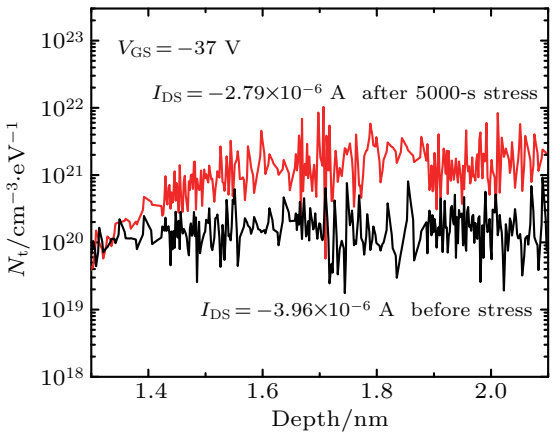


Fig. 10. Spatial distribution of oxide trapped charge density in gate oxide before and after stress.

4. Conclusions

The effects of negative bias stress on current–voltage curves and low frequency noise characteristics in p-type poly-Si TFTs are investigated in this paper. The variations of threshold voltage, field effect mobility and sub-threshold swing are extracted and analyzed, and more degradation is observed with bias stress increasing. The process of formation of Si^* and negative charge OH^- is clarified by a negative charge model. In addition, the contributions of stress-induced oxide trapped charges and interface states to the variation of threshold voltage are distinguished, and the shift of threshold voltage is dominated by stress-induced interface states under higher stress. Finally, the values of flat-band voltage spectral density and spatial distribution of trap charges are extracted and analyzed, and the results are consistent with the proposed experimental model.

References

[1] Maiolo L, Pecora A, Maita F, Minotti A, Zampetti E, Pantalei S, Macagnano A, Bearzotti A, Ricci D and Fortunato G 2013 *Sen. Actuators B* **179** 114
[2] Fortunato E, Barquinha P and Martins R 2012 *Adv. Mater.* **24** 2945
[3] Ho C, Panagopoulos G and Roy K 2013 *IEEE Trans. Electron. Dev.* **60** 288
[4] Yan B, Yang J, Xia Z, Liu X, Du G, Han R, Kang J, Liao C C, Gan Z, Liao M, Wang J P and Wong W 2008 *IEEE T. Nanotechnol.* **7** 418
[5] Zhou D, Wang M and Zhang S 2011 *IEEE Trans. Electron. Dev.* **58** 3422
[6] Tai Y H, Chiu H L and Chou L S 2013 *J. Disp. Technol.* **9** 613
[7] Chang G W, Chang T C, Jhu J C, Tsai T M, Chang K C, Syu Y E, Tai Y H, Jian F Y and Hung Y C 2014 *IEEE Trans. Electron. Dev.* **61** 2119
[8] Son K S, Kim H S, Maeng W J, Lee K H, Kim T S, Park J S, Kwon J Y, Koo B and Lee S Y 2011 *IEEE Electron. Dev. Lett.* **32** 164
[9] Mishra R, Mitra S and Gauthier R 2008 *IEEE Electron. Dev. Lett.* **29** 262
[10] Jo M, Chang M, Kim S, Jung S, Park J B, Lee J, Seong D J and Hwang H 2009 *IEEE Electron. Dev. Lett.* **30** 1194
[11] Zhou J, Wang M and Wong M 2011 *IEEE Trans. Electron. Dev.* **58** 3034
[12] Cho E N, Kang J H, Kim C E and Moon P 2011 *IEEE Trans. Dev. Mater. Reliab.* **11** 112
[13] Ma M W, Chen C Y, Wu W C, Su C J, Kao K H, Chao T S and Lei T F 2008 *IEEE Trans. Electron. Dev.* **55** 1153
[14] Wang R S, Huang R, He Y D, Wang Z H, Jia G S, Kim W D, Park D G and Wang Y Y 2008 *IEEE Electron. Dev. Lett.* **29** 242
[15] Xiong N, Xiao P, Li M, Xu H, Yao R H, Wen S S and Peng J B 2013 *Appl. Phys. Lett.* **102** 242102
[16] Hu H H, Jheng Y R, Wu Y C, Hung M F and Huang G W 2012 *IEEE Electron. Dev. Lett.* **33** 1276
[17] Pichon L, Boukhenoufa A, Cordier C and Cretu B 2007 *IEEE Electron. Dev. Lett.* **28** 716
[18] Liu Y, He H Y, Chen R S, En Y F, Li B and Chen Y Q 2018 *IEEE J. Electron Dev. Soc.* **6** 271
[19] Liu Y, He H Y, Chen Y Y, Chen R, Wang L and Cai S T 2019 *IEEE Trans. Electron Dev.* **66** 2192
[20] Hu C F, Wang M X, Zhang B and Wong M 2009 *IEEE Trans. Electron. Dev.* **56** 587
[21] Chen C Y, Lee J W, Wang S D, Shieh, M S, Lee P H, Chen W C, Lin H Y, Yeh K L and Lei T F 2006 *IEEE Trans. Electron. Dev.* **53** 2993
[22] Maeda S, Maegawa S, Ipposhi T, Nishimura H, Ichiki T, Mitsuhashi J, Ashida M, Muragishi T, Inou, Y and Nishimura T 1994 *J. Appl. Phys.* **76** 8160

[23] Gleskova H and Wagner S 2001 *IEEE Trans. Electron. Dev.* **48** 1667
[24] Schwank J R, Shaneyfelt M R, Fleetwood D M, Felix J A, Dodd P E and Paillet P 2008 *IEEE Trans. Nucl. Sci.* **55** 1833
[25] Liu Y, Chen H B, Liu Y R, Wang X, En Y F, Li B and Lu Y D 2015 *Chin. Phys. B* **24** 088503
[26] Doremus R H 1976 *J. Phys. Chem.* **80** 1773
[27] Yamamoto T, Uwasawa K and Mogami T 1999 *IEEE Trans. Electron. Dev.* **46** 921
[28] Ristić G S, Pejović M M and Jakšić A B 2000 *J. Appl. Phys.* **87** 3468
[29] Wang L, Liu Y, Geng K W, Chen Y Y and En Y F 2018 *Chin. Phys. B* **27** 068504
[30] Hooge F N 1994 *IEEE Trans. Electron. Dev.* **41** 1926
[31] McWhorter A L, Meyer J W and Strum P D 1957 *Phys. Rev.* **108** 1642
[32] Ghibaudo G, Roux O 1991 *Phys. Status Solidi A* **124** 571
[33] Dimitriadis C A, Kamarinos G and Brini J 2001 *IEEE Electron. Dev. Lett.* **22** 381
[34] Wang M X and Wang M 2014 *IEEE Trans. Electron Dev.* **61** 3258
[35] Jomaah J and Balestra F 2004 *Proc. Inst. Elect. Eng.—Circuits Devices Syst.* **151** 111
[36] Ioannidis E G, Tsormpatzoglou A, Tassis D H, Dimitriadis C A, Templier F and Kamarinos G 2010 *J. Appl. Phys.* **108** 106103
[37] Liu Y, Cai S T, Han C Y, Chen Y Y, Wang L, Xiong X M and Chen R S 2019 *IEEE J. Electron. Dev. Soc.* **7** 203
[38] Liu Y, Chen R S, Li B, En Y F and Chen Y Q 2018 *IEEE Trans. Electron. Dev.* **65** 356