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Effects of active layer thickness on performance and stability of dual-active-layer amorphous InGaZnO thin-film transistors*

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Dual-active-layer (DAL) amorphous InGaZnO (IGZO) thin-film transistors (TFTs) are fabricated at low temperature without post-annealing. A bottom low-resistance (low-*R*) IGZO layer and a top high-resistance (high-*R*) IGZO layer constitute the DAL homojunction with smooth and high-quality interface by *in situ* modulation of oxygen composition. The performance of the DAL TFT is significantly improved when compared to that of a single-active-layer TFT. A detailed investigation was carried out regarding the effects of the thickness of both layers on the electrical properties and gate bias stress stabilities. It is found that the low-*R* layer improves the mobility, ON/OFF ratio, threshold voltage and hysteresis voltage by passivating the defects and providing a smooth interface. The high-*R* IGZO layer has a great impact on the hysteresis, which changes from clockwise to counterclockwise. The best TFT shows a mobility of 5.41 $cm^2/V{\cdot}s$, a sub-threshold swing of 95.0 mV/dec, an ON/OFF ratio of 6.70×10^7, a threshold voltage of 0.24 V, and a hysteresis voltage of 0.13 V. The value of threshold voltage shifts under positive gate bias stress decreases when increasing the thickness of both layers.

Keywords: thin film transistor, InGaZnO, dual-active-layer

PACS: 73.61.Ga, 77.55.hf, 85.30.–z, 85.30.Tv **DOI:** 10.1088/1674-1056/28/8/087302

1. Introduction

Amorphous oxide semiconductor-based thin-film transistors (TFTs) are considered as the most prominent candidate for next-generation flexible display systems[1–3] and many other applications.[4] The TFT parameters of field-effect mobility (μ_{FE}), ON/OFF ratio, sub-threshold swing (*SS*), and threshold voltage (V_{th}) are critical for the practical applications. These parameters are strongly influenced by the oxygen vacancies in the active layer. A high-temperature (> 300 °C) post-annealing process is required to control the concentration of oxygen vacancies to optimize the electrical characteristics.[5–7] However, such high processing temperature is generally incompatible with many common polymer substrates. In addition, μ_{FE} and V_{th} show opposite dependence on the carrier concentration: a high carrier concentration of the active layer leads to a large μ_{FE} but a negative and poor-controllable V_{th}, while a lower carrier concentration results in a positive V_{th} but a much lower μ_{FE}.[8]

Many groups have adopted the dual-active-layer (DAL) architecture to solve this contradiction and achieve high mobility and suitable V_{th} simultaneously. The DAL normally contains a bottom layer with high electron concentration and a top layer with low defect density. The former is close to the channel and the latter close to the contacts. Kim *et al.* reported a DAL TFT with indium–zinc oxide (IZO) or indium–tin oxide (ITO) bottom layer and InGaZnO (IGZO) top layer.[8] The thin IZO or ITO layer is for the high mobility and the IGZO layer for the suitable V_{th}. Kim *et al.* proposed solution-processed AlInZnO (AIZO)/InZnO (IZO) DAL TFTs and came to a similar conclusion.[9] Marrs *et al.* fabricated IGZO/IZO DAL TFTs on flexible plastic substrates and demonstrated that a high saturation mobility and good gate bias stress stability could be achieved without the necessity of high-temperature annealing.[10] Many other groups studied the influence of the components of the two layers, or the thickness of the bottom layer with high carrier concentration, on the performance and stability of the devices.[11–18]

Compared with the above-mentioned hetero-DAL structures, the homo-DAL structure has a simple fabrication process. Nag *et al.* proposed the single-source dual-layer concept and applied it to the display and circuits.[19] Tian *et al.* fabricated fully transparent DAL IGZO TFTs with different oxygen compositions in two layers.[20] Park *et al.* studied the influence of oxygen vacancy concentrations in both IGZO layers

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on the device stabilities.[21] In the present study, we fabricate DAL IGZO TFTs by simply adjusting the O_2/Ar gas ratio during the sputtering at 100 ℃ without post-annealing, and investigate the effect of the thickness of both the bottom layer (low-resistance layer) and the top layer (high-resistance layer) on the TFT parameters. The dependence of positive gate bias stress stabilities and hysteresis phenomena on the thickness of each layer is explored and analyzed as well. The role of the IGZO homojunction interface was revealed based on the morphological characterization of the bottom layer and its influence on the device performance.

2. Experiment

The structure of the DAL IGZO TFTs is illustrated in Fig. 1(a). First, a 35-nm-thick Cr gate layer is deposited on quartz glass by radio frequency (RF) magnetron sputtering and patterned by UV-lithography followed by wet etching (JET-929, Changsha Jinxin Electronic Materials Co. Ltd). Then a 30-nm-thick Al_2O_3 gate dielectric layer is deposited by atomic layer deposition (ALD) and patterned by UV-lithography and wet etching (hot dilute AZ 300MIF developer). The low-resistance (low-R) IGZO layer is prepared by RF-magnetron sputtering at 100 ℃ with pure Ar atmosphere, followed by *in situ* deposition of a high-resistance (high-R) IGZO layer at 100 ℃ with a mixed sputtering gas of $Ar/O_2 = 10:4$. The DAL channel is patterned by the third-step UV-lithography and wet etching (dilute hydrochloric acid). Lastly, a 100-nm-thick ITO source/drain electrode is deposited by RF-magnetron sputtering and patterned by a lift-off method. No post-annealing treatment was conducted on the as-fabricated TFTs.

To investigate the effect of active layer thickness on the TFT performance, we first vary the growth time of low-R IGZO from 0 min to 5 min while keeping a constant 30 min growth of the high-R IGZO layer. The low-R IGZO growth time was optimized as 4 min in this case, then the high-R IGZO growth time was adjusted from 15 min to 60 min. The samples are labeled as (growth time of low-R)+(growth time of high-R). For instance, $3+30$ means that the growth time of the low-R layer is 3 min and the high-R layer 30 min.

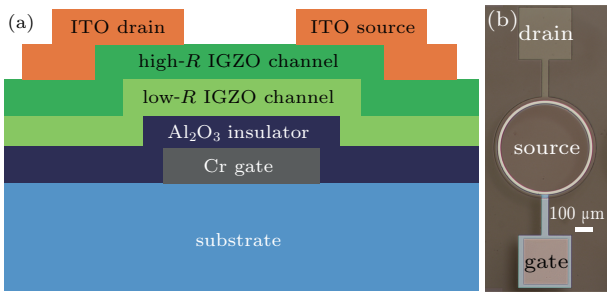


Fig. 1. Schematic diagram of DAL IGZO TFT. (a) Structure from the cross-section view. (b) Micrograph from the top view. The scale bar represents 100 μm.

The film thickness is measured by a surface profiler (KLA-Tencor P-6). The electrical properties are revealed using the Van der Pauw method (HMS-3000, Ecopia). The surface morphology and roughness are evaluated by atomic force microscopy (AFM; Dimension Edge, Bruker). I–V characteristic measurements are performed in the dark using a Keithley 4200 semiconductor characterization system.

The circular Corbino TFT structure can be seen in Fig. 1(b). The inner cycle with the radius R_1 of 252 μm is the source and the outer ring with the radius R_2 of 268 μm the drain. The channel length (L) is given by $R_2 - R_1$, whereas the effective channel width (W) is $\pi(R_1 + R_2)$. The μ_{FE} and SS are derived from the forward sweep of transfer characteristics with a drain voltage (V_{DS}) of 0.1 V using the following equations:[3]

$$\mu_{FE} = \frac{L}{W \cdot C_{ox} \cdot V_{DS}} \cdot \frac{dI_{DS}}{dV_{GS}},$$
$$SS = \left(\frac{dV_{GS}}{d\log_{10}(I_{DS})} \bigg|_{max} \right),$$

where C_{ox} is the specific capacitance of the gate dielectric per unit area, I_{DS} the drain current, and V_{GS} the gate voltage. The ON/OFF ratio is defined as the absolute value of the ratio of I_{DS} at $V_{GS} = 10$ V to that at $V_{GS} = -10$ V for comparison. The V_{th} is defined as the value of V_{GS} when $I_{DS} = W/L * 1$ nA in the linear region. The hysteresis voltage (V_H) is defined as the difference in V_{th} extracted from V_{GS} sweeps between off-to-on and on-to-off. All TFT parameters except for V_H are obtained from three independent devices where each test is repeated three times.

3. Results and discussion

The dependence of the total active layer thickness on the low-R IGZO growth time and high-R IGZO growth time is demonstrated in Fig. 2(a) and Fig. 2(b), respectively. The growth rates are extracted from the linear fitting, which are 2.99 nm/min for low-R IGZO and 0.85 nm/min for high-R IGZO. In fact, the IGZO grows much slower under oxygen-rich conditions.[22]

Figure 3 shows the surface morphology of low-R IGZO films. For the growth time of 1 min, the surface is island-like and the root mean square (RMS) roughness is 1.60 nm, as shown in Fig. 3(a). When the growth time increases to 2 min, the islands coalesce into a smooth film with a low RMS roughness of 0.304 nm [Fig. 3(b)]. Figure 3(c) indicates that the 4 min low-R IGZO film becomes even smoother, where the RMS roughness is 0.140 nm. The smooth surface of low-R IGZO facilitates the formation of an abrupt homo-interface with high-R IGZO, which is of great importance for the electron transport.[17]

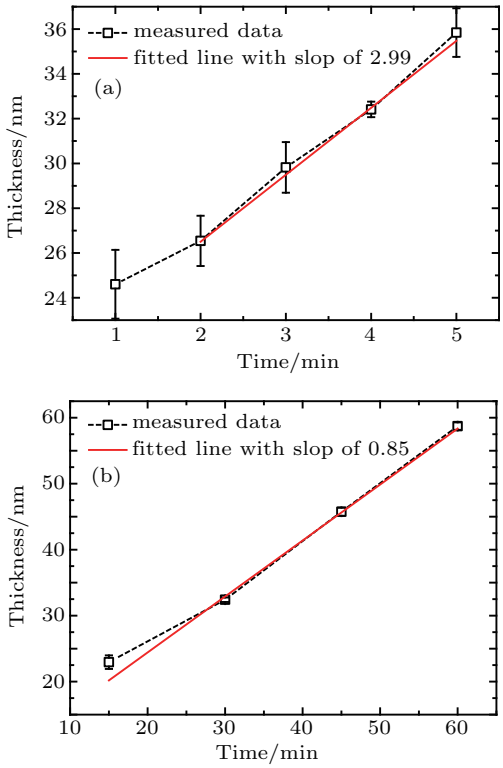


Fig. 2. The dependence of total channel layer thickness on the growth time of (a) the low-*R* IGZO layer (with 30 min high-*R* IGZO layer) and (b) the high-*R* IGZO layer (with 4 min low-*R* IGZO layer).

The low-*R* IGZO film sputtered under oxygen-deficient conditions contains a large number of oxygen vacancies, which leads to a high electron concentration of 1.52×10^{19} cm^{-3}. Such a high concentration of electrons could passivate the trap states at the interface between the channel and dielectric layers effectively.[14,23] The Hall mobility of low-*R* IGZO is 10.4 cm^2/V· s and the resistivity 3.97×10^{-2} Ω· cm. The resistance of high-*R* IGZO film is higher than 200 MΩ and cannot be measured in the HMS-3000 Hall system.

Figure 4 shows the transfer characteristics for the IGZO TFTs with different thicknesses of low-*R* layers. The TFT parameters are summarized in Table 1. The 0+30 sample, *i.e.* the sample only containing a high-*R* IGZO single active layer, exhibits a very low ON/OFF ratio of about 200 and very large $V_{\rm H}$ above 9 V at $V_{\rm DS} = 0.1$ V, where the on-state $I_{\rm DS}$ even decreases with elevated $V_{\rm GS}$, as shown in Fig. 4(a). The transfer curve with $V_{\rm DS} = 5$ V presents $V_{\rm th} > 9$ V and degraded $I_{\rm DS}$ with respect to that of $V_{\rm DS} = 1$ V. Defects are generated at the dielectric interface during the sputtering of IGZO, which traps the electron during the $V_{\rm GS}$ sweeping and leads to the low on-state $I_{\rm DS}$, large clockwise $V_{\rm H}$ and non-equilibrium, non-steady-state TFT operation.[24] The ON/OFF ratio increases by two orders of magnitude after inserting a 1 min low-*R* IGZO layer, but the $V_{\rm H}$ is still very large, as shown in Fig. 4(b). The AFM image in Fig. 3(a) demonstrates that the 1 min low-*R* IGZO is discontinuous so that the current flows partly though the low-*R* IGZO and partly through the high-*R* IGZO. A large number of defects remain at the interface between the dielectric and high-*R* IGZO layers, which will still trap the electrons and lead to the non-equilibrium, non-steady-state TFT operation. The 2-min low-*R* IGZO layer turns into continuous film, benefitting the passivation of the interface defects by the large number of electrons. The ON/OFF ratio is $\sim 10^7$, even reaching 10^{10} when the minimum and maximum currents at $V_{\rm DS} = 5$ V are chosen. The $V_{\rm H}$ is smaller than 0.3 V [Fig. 4(c)]. Note that the $V_{\rm th}$ shifts in the negative direction with thicker low-*R* IGZO layer due to the increasing total number of electrons [Figs. 4(c)–4(f)]. The best TFT performance belongs to the 4+30 sample, where the $\mu_{\rm FE}$ is 5.41 ± 0.05 cm^2/V·s, *SS* 95.0 ± 6.9 mV/dec, ON/OFF ratio $6.70\pm0.95\times10^7$, $V_{\rm th}0.24\pm0.12$ V, and $V_{\rm H}$ 0.13 V.

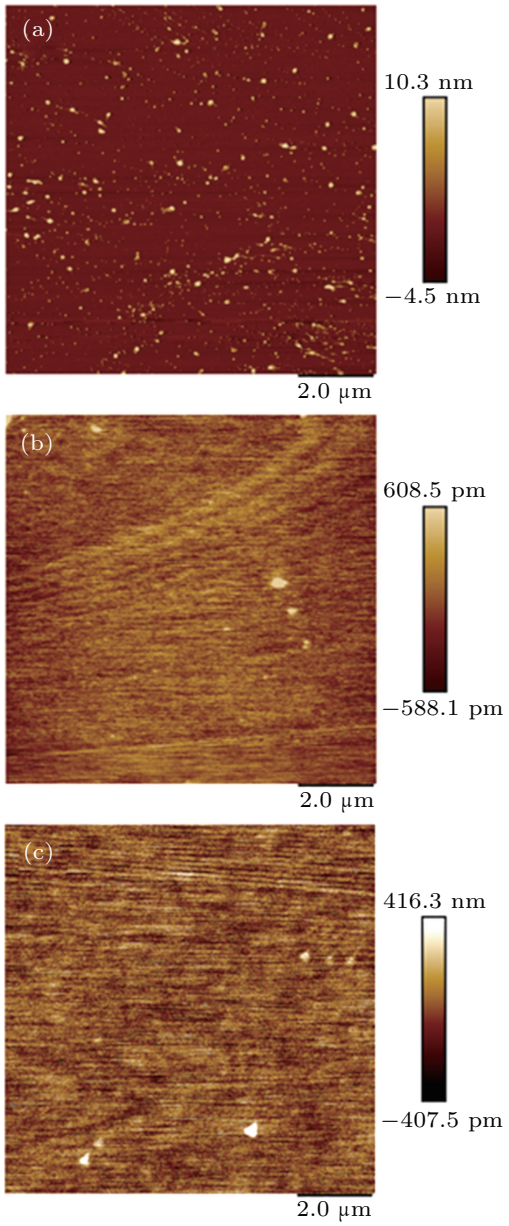


Fig. 3. AFM image of low-*R* IGZO film with the growth time of (a) 1 min, (b) 2 min, and (c) 4 min.

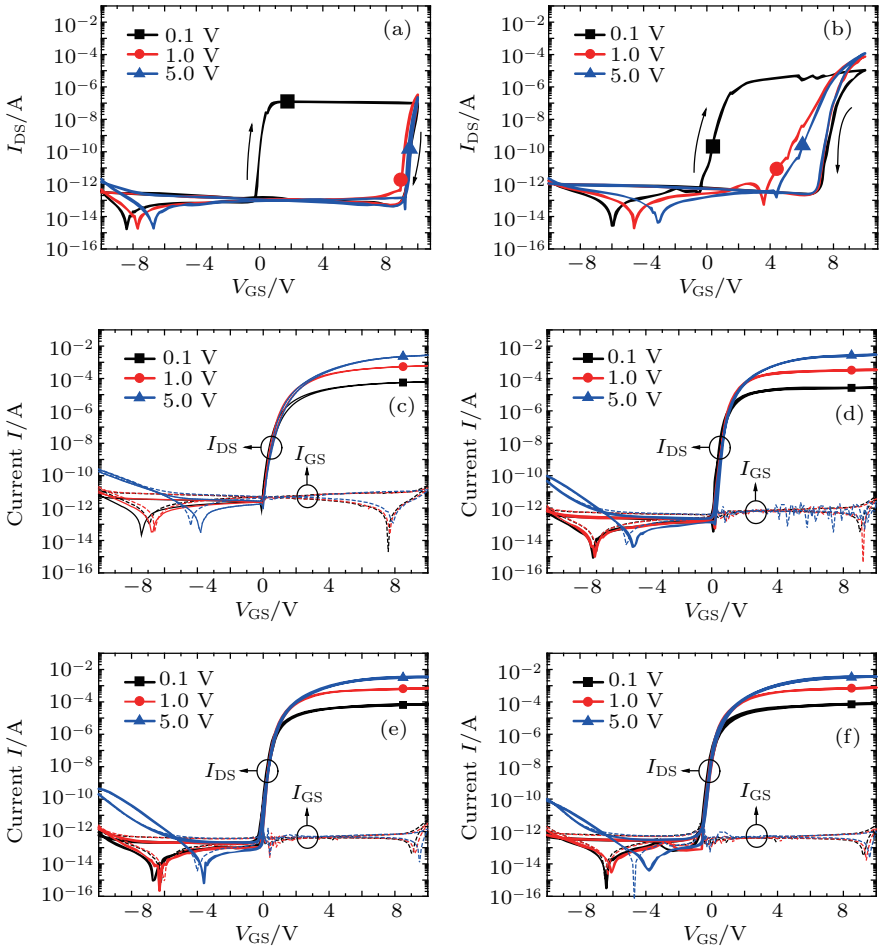


Fig. 4. Transfer characteristics for IGZO TFTs with different thicknesses of low-*R* layers: (a) 0+30, (b) 1+30, (c) 2+30, (d) 3+30, (e) 4+30, and (f) 5+30.

Figure 5 manifests the output characteristics of the IGZO TFTs with various thicknesses of low-*R* layers. The curves do not show much difference except for the current values. The excellent saturation demonstrates the small contact resistances.

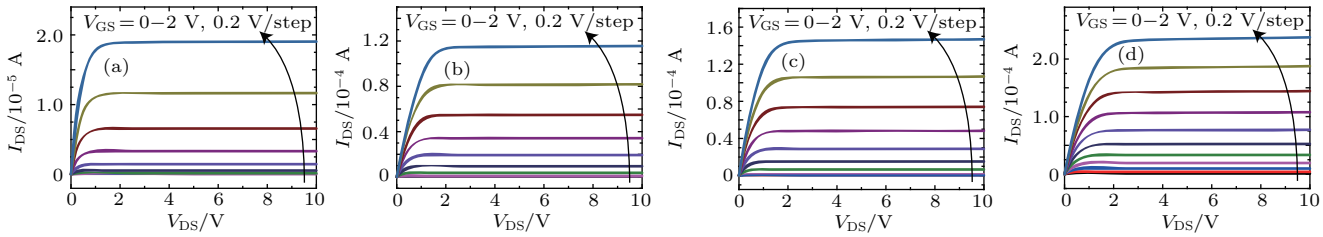


Fig. 5. Output characteristics of IGZO TFTs with different thicknesses of low-*R* layers: (a) 2+30, (b) 3+30, (c) 4+30, and (d) 5+30.

Table 1. Summary of TFT parameters for low-*R* IGZO layer with different thicknesses.

Samples	Thickness/nm	μ_{FE}/(cm^2/V·s)	*SS*/(mV/dec)	ON/OFF ratio	V_{th}/V	V_H/V
0+30	18.87 ± 0.50	–	–	1.93×10^2	–	> 9
1+30	24.60 ± 1.54	–	–	7.25×10^4	–	4.87
2+30	26.54 ± 1.12	4.63 ± 0.19	180 ± 33	$7.29 \pm 2.54 \times 10^6$	0.51 ± 0.10	0.22
3+30	29.82 ± 1.13	4.43 ± 0.36	80.2 ± 4.2	$6.35 \pm 1.49 \times 10^7$	0.35 ± 0.03	0.12
4+30	32.41 ± 0.35	5.41 ± 0.05	95.0 ± 6.9	$6.70 \pm 0.95 \times 10^7$	0.24 ± 0.12	0.13
5+30	35.84 ± 1.09	5.14 ± 0.09	120 ± 3.5	$5.00 \pm 0.66 \times 10^7$	−0.26 ± 0.05	0.14

The transfer characteristics for the IGZO TFTs with various thicknesses of high-*R* IGZO layers are shown in Fig. 6. The 4+15 sample exhibits large clockwise hysteresis, which is reduced to smaller than 0.2 V for the 4+30 sample. Intriguingly, the hysteresis changes its direction from clockwise to counterclockwise for the 4+45 sample, and the counterclockwise hysteresis becomes bigger when the thickness of the high-*R* IGZO layer further increases. The TFT parame-

ters are summarized in Table 2. The hysteresis voltage V_H gradually changes from 1.47 V to −1.41 V as the thickness of the high-*R* IGZO increases. Generally, the counterclockwise hysteresis phenomenon is attributed to several mechanisms: (i) acceptor-like defects in the dielectric or at the channel/dielectric interface,[25,26] (ii) slow polarization in the dielectric layer,[27–29] (iii) mobile charges,[30,31] (iv) charges injected from the gate electrode,[32–34] and (v) negative capacitance by ferroelectric dielectric,[35,36] but none of them can explain the transition trends with the thickness change of the high-*R* IGZO. In this case, the interface between the dielectric and channel is the same for all these samples, while the only difference is the high-*R* IGZO layer. The counterclockwise hysteresis has also been reported in bilayer InGaO TFTs with a 10-nm-thick front channel layer and 40-nm-thick back channel layer,[37] where the thickness of both layers is close to that of the 4+60 sample. ZnO/ZnMgO field-effect transistors with two-dimensional electron gas in the ZnO channel also exhibit counterclockwise hysteresis.[38] The existence of a large amount of carriers in the channel might be the origin of the hysteresis phenomenon. The mechanism needs to be further investigated.

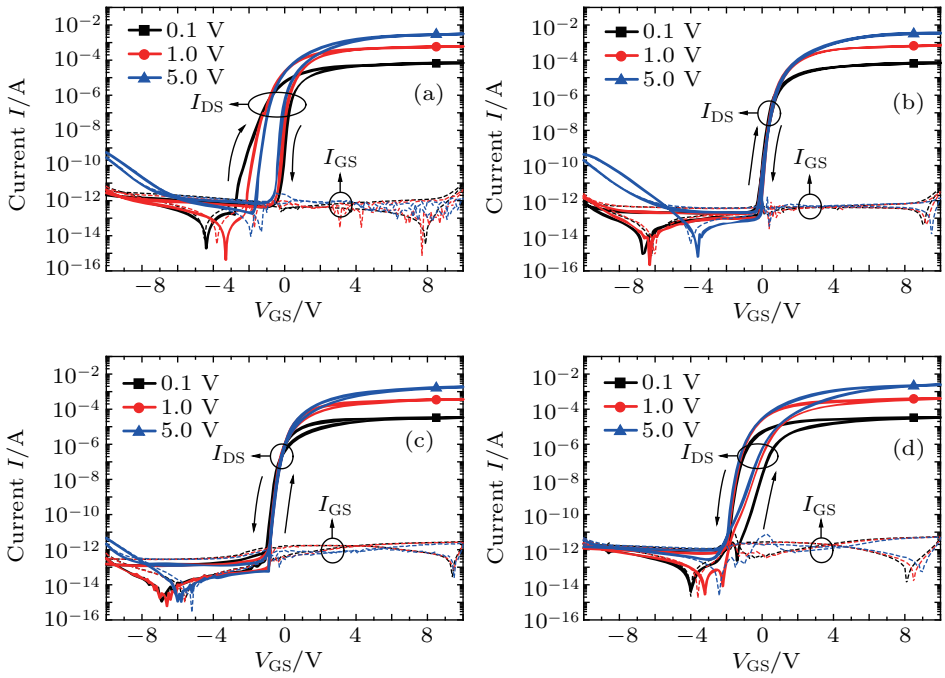


Fig. 6. Transfer characteristics for IGZO TFTs with different thicknesses of high-*R* layers: (a) 4+15, (b) 4+30, (c) 4+45, and (d) 4+60.

The μ_{FE} and ON/OFF ratio significantly decrease when the growth time of high-*R* IGZO is larger than 45 min. The off-state I_{DS} at $V_{DS} = 5$ V also decreases as the thickness of high-*R* IGZO increases. The slight degradation of saturation current in Fig. 7(a) can also be seen from the transfer curves in Fig. 6(a), and it is different from the oversaturation hump phenomena.[20,39–41] The mechanism also needs to be further investigated. The degraded saturation current is recovered when the growth time of high-*R* IGZO increases to 30 min [Fig. 7(b)]. On the other hand, the thick high-*R* IGZO acts as a large resistor that connects in series with the channel, resulting in the reduction of μ_{FE} and off-state I_{DS} as well as the contact resistance. The large contact resistance leads to the increase of pinch-off voltage, as shown in the output characteristics for the IGZO TFTs in Fig. 7(c) and Fig. 7(d).

The 4+30 sample presents the best TFT performance of all these samples. It is found that the thickness of low-*R* IGZO exerts little influence over the device performance as long as it forms a continuous and smooth film. However, the thickness of high-*R* IGZO has a huge impact on μ_{FE}, V_{th}, and V_H. It was reported that the thick back channel layer (high-*R* layer in this work) controls the charge conductance, resulting in a suitable threshold voltage.[9] Here, we demonstrate that this layer also has a great effect on the hysteresis.

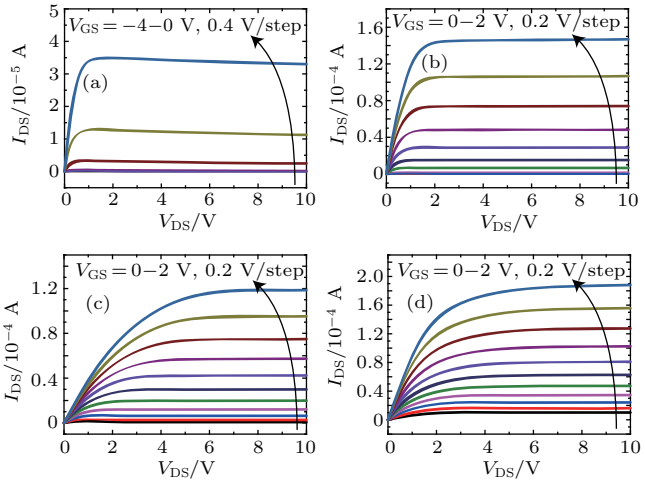


Fig. 7. Output characteristics for IGZO TFTs with different thicknesses of high-*R* layers: (a) 4+15, (b) 4+30, (c) 4+45, and (d) 4+60.

Table 2. Summary of TFT parameters for high-*R* IGZO layer with different thicknesses.

Samples	Thickness/nm	$\mu_{FE}/(cm^2/V\cdot s)$	*SS*/(mV/dec)	ON/OFF ratio	V_{th}/V	V_H/V
4+15	22.95 ± 1.02	4.86 ± 0.30	191 ± 16	$1.82\pm0.17\times10^7$	-1.85 ± 0.07	1.47
4+30	32.41 ± 0.35	5.41 ± 0.05	95.0 ± 6.9	$6.70\pm0.95\times10^7$	0.24 ± 0.12	0.13
4+45	45.75 ± 0.61	1.62 ± 0.25	115 ± 4.3	$5.80\pm2.69\times10^7$	-0.07 ± 0.15	-0.05
4+60	58.72 ± 0.56	1.60 ± 0.14	243 ± 17	$1.73\pm1.47\times10^7$	0.16 ± 0.03	-1.41

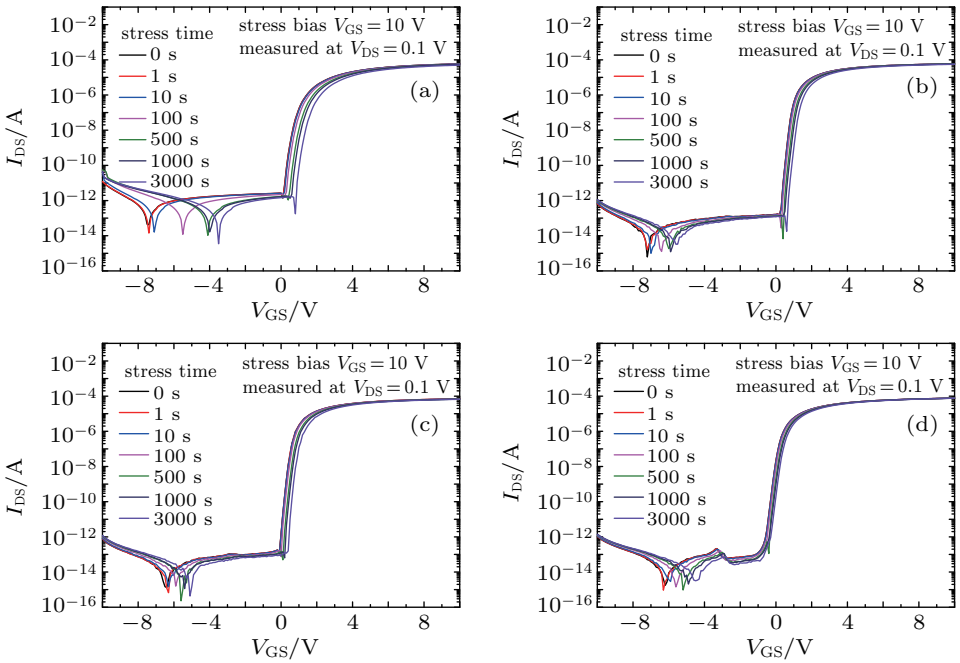


Fig. 8. Evolution of the transfer characteristics of IGZO TFTs for (a) 2+30, (b) 3+30, (c) 4+30, and (d) 5+30.

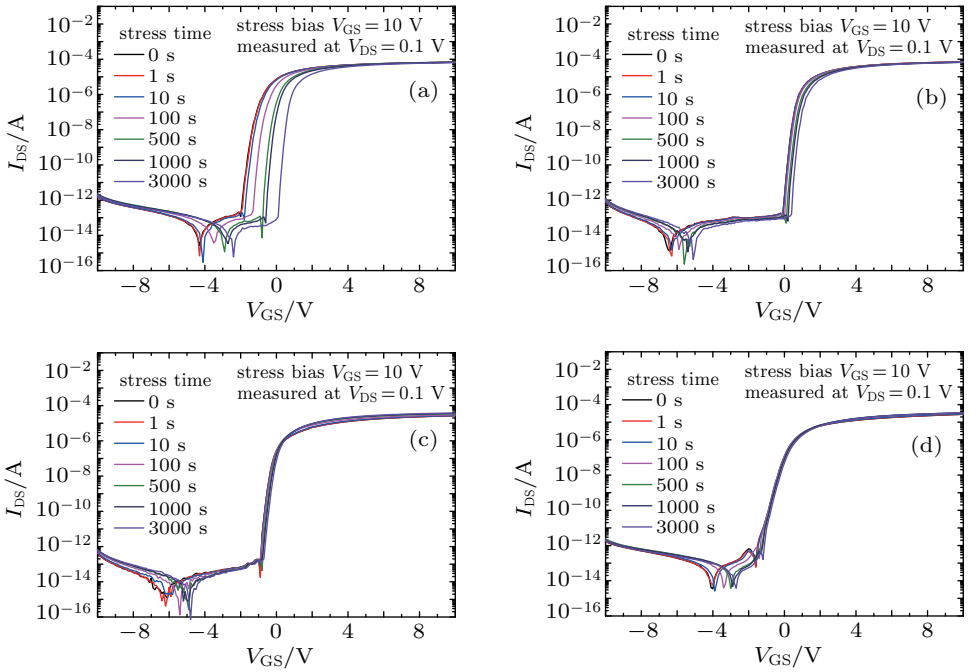


Fig. 9. Evolution of the transfer characteristics of IGZO TFTs for (a) 4+15, (b) 4+30, (c) 4+45, and (d) 4+60.

The positive gate bias stress (PBS) characteristics of the IGZO TFTs with different thicknesses of low-*R* IGZO layers are shown in Fig. 8, and with different high-*R* IGZO layers in Fig. 9. The transfer characteristics were measured at $V_{DS}=0.1$ V under a gate bias stress of $V_{GS}=10$ V at set intervals. The PBS results in a positive V_{th} shift (ΔV_{th}) for all

samples. The value of *SS* is basically unchanged for all TFTs (not shown here). Therefore, the V_{th} shifts are dominated by the charge trapping in the gate dielectric or at the channel–dielectric interface rather than on defect creation.[42–44] The threshold voltage shifts *versus* stress time are shown in Fig. 10. The value of ΔV_{th} decreases with thicker low-*R* IGZO, as shown in Fig. 10(a). This can be attributed to the increase in the total amount of electrons, which passivates the trap states. The value of ΔV_{th} also decreases with thicker high-*R* IGZO, as shown in Fig. 10(b). The dynamic interaction between the ambient atmosphere and the exposed back channel affects the V_{th} stability. Although there is no extra passivation layer to protect the back channel, the high-*R* IGZO layer serves as a passivation for the TFTs and inhibits the back channel formation.[5,44]

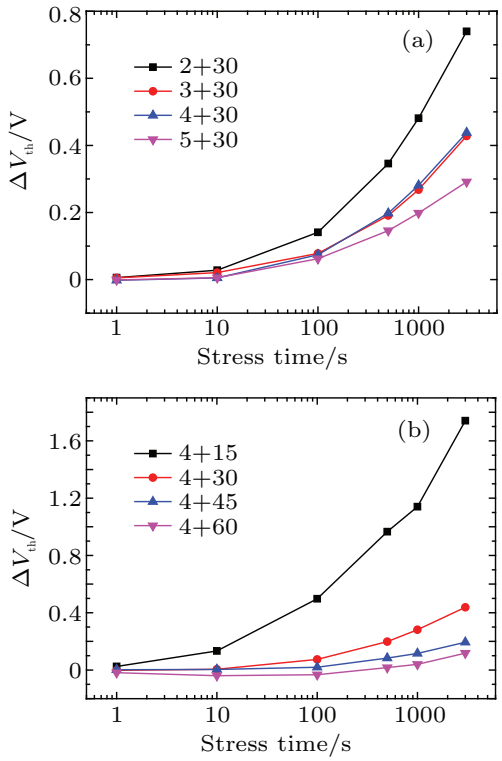


Fig. 10. The threshold voltage shifts *versus* stress time with different growth times of (a) low-*R* IGZO layer and (b) high-*R* layer.

4. Conclusion

In summary, DAL IGZO TFTs with various thicknesses of both layers have been fabricated, and their effects on TFT performance and stability have been investigated. When a continuous and smooth low-*R* layer forms, the μ_{FE}, ON/OFF ratio, V_{th}, and V_H are significantly improved due to the passivation of defects and the high-quality homojunction interface. The influence becomes weak after the thickness of the low-*R* layer increases beyond about 10 nm. The high-*R* layer not only affects the value of μ_{FE} and V_{th}, but also has a huge impact on V_H. The hysteresis gradually changes from clockwise to counterclockwise with the increasing thickness of the high-*R* layer. The V_{th} shifts decrease with both a thicker low-*R* and high-*R* layer. The excellent stability of DAL IGZO TFTs facilitates their application in active-matrix liquid-crystal displays and active matrix organic light-emitting diodes.

References

[1] Kamiya T, Nomura K and Hosono H 2010 *Sci. Technol. Adv. Mater.* **11** 044305
[2] Fortunato E, Barquinha P and Martins R 2012 *Adv. Mater.* **24** 2945
[3] Petti L, Münzenrieder N, Vogt C, Faber H, Büthe L, Cantarella G, Bottacchi F, Anthopoulos T D and Tröster G 2016 *Appl. Phys. Rev.* **3** 021303
[4] Wang K 2017 *SID Symp. Dig. Tech. Pap.* **48** 497
[5] Chen W T, Lo S Y, Kao S C, Zan H W, Tsai C C, Lin J H, Fang C H and Lee C C 2011 *IEEE Electron Device Lett.* **32** 1552
[6] Ye Z, Xu H, Liu T, Liu N, Wang Y, Zhang N and Liu Y 2017 *IEEE Trans. Electron. Devices* **64** 4114
[7] Huo W, Mei Z, Zhao M, Sui Y, Zhao B, Zhang Y, Wang T, Cui S, Liang H, Jia H and Du X 2018 *IEEE Trans. Electron. Devices* **65** 3791
[8] Kim S I, Kim C J, Park J C, Song I, Kim S W, Huaxiang Yin, Eunha Lee, Jae Chul Lee and Youngsoo Park 2008 *2008 IEEE International Electron Devices Meeting* 2008 IEEE International Electron Devices Meeting (IEDM) (San Francisco, CA, USA: IEEE) pp. 1–4
[9] Kim K M, Jeong W H, Kim D L, Rim Y S, Choi Y, Ryu M K, Park K B and Kim H J 2011 *IEEE Electron Dev. Lett.* **32** 1242
[10] Marrs M A, Moyer C D, Bawolek E J, Cordova R J, Trujillo J, Raupp G B and Vogt B D 2011 *IEEE Trans. Electron. Dev.* **58** 3428
[11] Jeong W H, Kim K M, Kim D L, Rim Y S and Kim H J 2012 *IEEE Trans. Electron. Dev.* **59** 2149
[12] Seo J S and Bae B S 2014 *ACS Appl. Mater. Interfaces* **6** 15335
[13] Lee S H and Choi W S 2015 *J. Disp. Technol.* **11** 698
[14] Abliz A, Huang C W, Wang J, Xu L, Liao L, Xiao X, Wu W W, Fan Z, Jiang C, Li J, Guo S, Liu C and Guo T 2016 *ACS Appl. Mater. Interfaces* **8** 7862
[15] Choi J H, Yang J, Nam S, Pi J, Kim H, Kwon O, Park E, Hwang C and Cho S H 2016 *IEEE Electron Dev. Lett.* **37** 1295
[16] Liu Y R, Zhao G W, Lai P T and Yao R H 2016 *Chin. Phys. B* **25** 088503
[17] Faber H, Das S, Lin Y H, Pliatsikas N, Zhao K, Kehagias T, Dimitrakopulos G, Amassian A, Patsalas P A and Anthopoulos T D 2017 *Sci. Adv.* **3** e1602640
[18] Stewart K A, Gouliouk V, McGlone J M and Wager J F 2017 *IEEE Trans. Electron. Dev.* **64** 4131
[19] Nag M, Chasin A, Rockele M, Steudel S, Myny K, Bhoolokam A, Tripathi A, van der Putten B, Kumar A, van der Steen J L, Genoe J, Li F, Maas J, van Veenendaal E, Gelinck G and Heremans P 2013 *J. Soc. Inf. Disp.* **21** 129
[20] Tian Y, Han D, Zhang S, Huang F, Shan D, Cong Y, Cai J, Wang L, Zhang S, Zhang X and Wang Y 2014 *Jpn. J. Appl. Phys.* **53** 04EF07
[21] Park J H, Kim Y, Yoon S, Hong S and Kim H J 2014 *ACS Appl. Mater. Interfaces* **6** 21363
[22] Yang D G, Do Kim H, Kim J H, Lee S W, Park J, Kim Y J and Kim H S 2017 *Thin Solid Films* **638** 361
[23] Xu H, Xu M, Chen Z, Li M, Zou J, Tao H, Wang L and Peng J 2016 *IEEE Electron Dev. Lett.* **37** 57
[24] Wager J F 2010 *J. Soc. Inf. Disp.* **18** 749
[25] Qian L X and Lai P T 2014 *IEEE Trans. Device Mater. Reliab.* **14** 177
[26] Yue L, Meng F and Chen J 2018 *Semicond. Sci. Technol.* **33** 015012
[27] Yang W, Song K, Jung Y, Jeong S and Moon J 2013 *J. Mater. Chem. C* **1** 4275
[28] Banger K, Warwick C, Lang J, Broch K, Halpert J E, Socratous J, Brown A, Leedham T and Sirringhaus H 2016 *Chem. Sci.* **7** 6337
[29] Ye Z, Yuan Y, Xu H, Liu Y, Luo J and Wong M 2017 *IEEE Trans. Electron. Dev.* **64** 438
[30] Liu Y, Guan P, Zhang B, Falk M L and Katz H E 2013 *Chem. Mater.* **25** 3788
[31] Jo J W, Kim K H, Kim J, Ban S G, Kim Y H and Park S K 2018 *ACS Appl. Mater. Interfaces* **10** 2679

[32] Lee C A, Park D W, Jin S H, Park I H, Lee J D and Park B G 2006 *Appl. Phys. Lett.* **88** 252102
[33] Daunis T B, Tran J M H and Hsu J W P 2018 *ACS Appl. Mater. Interfaces* **10** 39435
[34] Wang X, Gao Y, Liu Z, Luo J and Wan Q 2019 *IEEE Electron Dev. Lett.* **40** 224
[35] Petti L, Münzenrieder N, Salvatore G A, Zysset C, Kinkeldei T, Büthe L and Tröster G 2014 *IEEE Trans. Electron. Dev.* **61** 1085
[36] Li Y, Liang R, Wang J, Jiang C, Xiong B, Liu H, Wang Z, Wang X, Pang Y, Tian H, Yang Y and Ren T 2019 *IEEE Electron Dev. Lett.* **40** 826
[37] Yang C P, Chang S J, Chang T H, Wei C Y, Juan Y M, Chiu C J and Weng W Y 2017 *IEEE Electron Dev. Lett.* **38** 572
[38] Sasa S, Ozaki M, Koike K, Yano M and Inoue M 2006 *Appl. Phys. Lett.* **89** 053502
[39] Oh M S, Lee K, Song J H, Lee B H, Sung M M, Hwang D K and Im S 2008 *J. Electrochem. Soc.* **155** H1009
[40] Han D, Zhang S, Zhao F, Dong J, Cong Y, Zhang S, Zhang X and Wang Y 2015 *Thin Solid Films* **594** Part B 266
[41] Jian L Y, Lee H Y, Lin Y H and Lee C T 2018 *J. Electron. Mater.* **47** 1467
[42] Cross R B M and De Souza M M 2006 *Appl. Phys. Lett.* **89** 263513
[43] Suresh A and Muth J F 2008 *Appl. Phys. Lett.* **92** 033502
[44] Jeong J K, Won Yang H, Jeong J H, Mo Y G and Kim H D 2008 *Appl. Phys. Lett.* **93** 123508