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Thermal conductivity characterization of ultra-thin silicon film using the ultra-fast transient hot strip method*

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Thermal conductivity is an important material parameter of silicon when studying the performance and reliability of devices or for guiding circuit design when considering heat dissipation, especially when the self-heating effect becomes prominent in ultra-scaled MOSFETs. The cross-plane thermal conductivity of a thin silicon film is lacking due to the difficulty in sensing high thermal conductivity in the vertical direction. In this paper, a feasible method that utilizes an ultra-fast electrical pulse within 20 μs combined with the hot strip technique is adopted. To the best of our knowledge, this is the first work that shows how to extract the cross-plane thermal conductivity of sub-50 nm (30 nm, 17 nm, and 10 nm) silicon films on buried oxide. The ratio of the extracted cross-plane thermal conductivity of the silicon films over the bulk value is only about 6.9%, 4.3%, and 3.8% at 300 K, respectively. As the thickness of the films is smaller than the phonon mean free path, the classical heat transport theory fails to predict the heat dissipation in nanoscale transistors. Thus, in this study, a ballistic model, derived from the heat transport equation based on extended-irreversible-hydrodynamics (EIT), is used for further investigation, and the simulation results exhibit good consistence with the experimental data. The extracted effective thermal data could provide a good reference for precise device simulations and thermoelectric applications.

Keywords: cross-plane thermal conductivity, ultra-fast transient hot strip method

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1. Introduction

To further improve device performance and the integration density of chips in the post-Moore era, novel structured transistors like FinFETs and ultra-thin body and buried oxide (UTBB) FETs have been adopted.[1,2] However, due to the high drive current and the low thermal conductivity, the severe self-heating effects of these new structure transistors may lead to reliability problems.[3,4] The thermal characterization of thin silicon films is of great importance for studying self-heating effects in high performance transistors. The accurate extraction of thermal parameters for these thin Si films, which is quite different from that for bulk silicon, is necessary for the heat modeling and estimation in high performance circuits.[5,6] In general, measurements of cross-plane thermal conductivity are much more difficult than those in the in-plane direction of silicon films, due to the small thermal resistance R_F induced by the high thermal conductivity film. Therefore, few research studies about the cross-plane thermal conductivity of silicon films have been reported. So far, cross-plane thermal conductivity has been measured in holey silicon structures, and the thermal conductivity of the porous film is much lower than that of the simulated whole silicon film.[7,8] The extra boundaries introduced increase the phonon boundary scattering and reduce the cross-plane thermal conductivity, which is significant for thermoelectric applications. Lots of models have been established to calculate the cross-plane thermal conductivity.[9–11] According to the simulation results given in Ref. [11], the cross-plane thermal conductivity decreases as the silicon film thickness diminishes and is lower than the in-plane thermal conductivity. The lower thermal conductivity in the vertical direction may result in a higher channel operating temperature and further degrade the performance of the devices. What is more, the heat transport mechanism in the vertical direction is different from that in the lateral orientation as the thickness of the silicon film decreases. With the film thickness reduced below 1 μm, diffusive heat transport in-plane is dominated by various scattering mechanisms, such as Umklapp scattering, phonon boundary scattering, and imperfection scattering.[12,13] However, with the thickness reduction, heat transport in the cross-plane transfers to ballistic phonon transport, which means that the phonon mean free path is shorter than the length scale in the temperature gradient direction and phonons can travel without the internal scattering. Therefore, it is important and necessary to investigate the cross-plane thermal conductivity of thin silicon films, whether

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for figuring out the operation principles of phonon transport in the vertical direction or for understanding the self-heating effect in transistors.

The transient hot strip method (THS) was first proposed by Gustafsson to extract the thermal conductivity and thermal diffusivity of solids and fluids,[14] and was later also applied to measure the thermal conductivity of metallic materials by inserting an insulation layer between the metal heater and the tested film.[15] The THS method is a feasible technique for thermal conductivity measurements. Traditionally, THS measurements are carried out in a millisecond or second time scale.[16] In this paper, we proposed an ultra-fast transient hot strip method to determine the cross-plane thermal conductivity of thin silicon films. The ultra-short pulse took place from nanosecond to microsecond time scales for film thickness ranging from 10 nm to tens of μm depending on the thermal diffusivity of the materials. The pulse width of the electrical voltage was selected from 200 ns to 20 μs, which is a compromise between our experimental setup and the requirement of measurement accuracy. The cross-plane thermal conductivity data for silicon films with different thicknesses (from 30 nm to 10 nm) at different temperatures (from 75 K to 400 K) were successfully extracted from the time dependent temperature response after the ultra-short electrical pulse. The positive temperature dependence indicates that phonon boundary scattering dominates in the studied temperature region. Adopting a novel analysis model derived from the heat transport equation based on extended irreversible hydrodynamics (EIT), good consistency was achieved between the experimental data and the simulations, experimentally verifying the ballistic phonon transport heat conduction in the cross plane of thin silicon films.

2. Experimental setup

The process flow for fabricating the test structures is shown in Fig. 1. After pre-cleaning the silicon-on-insulator (SOI) substrate with a thick Si layer, the silicon film was thinned to 30 nm, 17 nm, 10 nm, and 0 nm (control sample) by a cyclic thermal oxidation and HF etching. Following that, 10 nm-thick Al_2O_3 was grown by atomic layer deposition (ALD) at 300 ℃ to isolate the silicon film from the heater metal. After the deposition of a 50 nm-thick Ni layer by thermal evaporation, the Ni electrodes were patterned by optical lithography and wet-etching in diluted HCl. The schematic in Fig. 1 on the right shows a three-dimensional view of such a fabricated test structure. The length of the test structures is 1000 μm, and the width is 10 μm. The ratio of length/width was designed to be far greater than 20 to minimize the effect of the finite strip length. The thickness of the buried oxide (BOX) layer is 3 μm and the substrate silicon has a thickness of 675 μm.

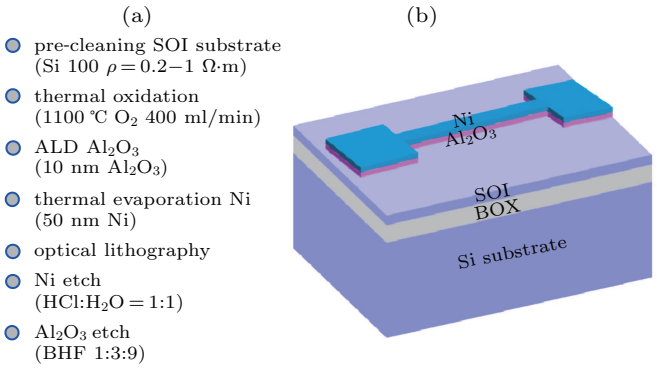


Fig. 1. (a) The process flow for fabricating the structure and (b) the schematic of the structure.

By applying an electrical pulse with a pulse time of 20 μs to the Ni electrode, the sample was heated by the Joule heating produced, and the temperature went up. In this structure, the Ni strip acted as both the heater and the sensor. The measurements were performed at an environmental temperature from 300 K to 400 K with steps of 10 K in a vacuum ambient of 2.7×10^{-7} mbar in order to minimize the effects of heat convection. The oven temperature was PID controlled, and the temperature accuracy was 0.001 K. The ambient temperature was sensed by a silicon diode placed close to the sample.

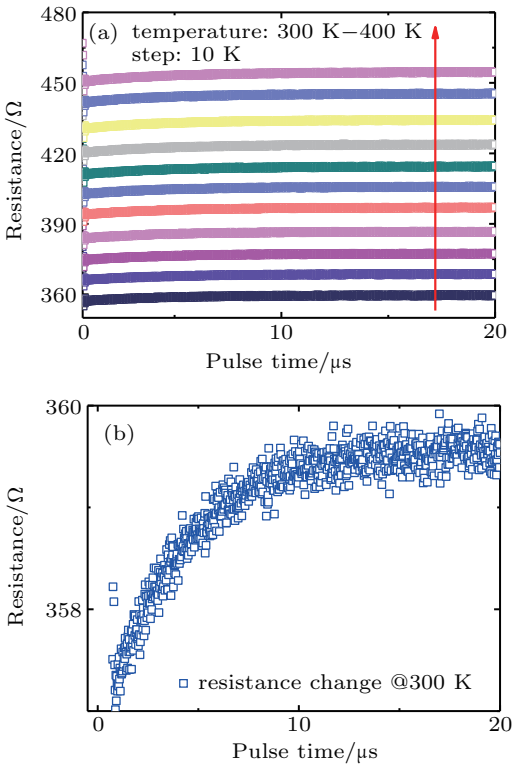


Fig. 2. (a) Resistance distribution at temperatures between 300 K and 400 K, varied as the pulse time increased, and (b) a zoomed-in schematic of the resistance distribution at temperature 300 K.

The resistance responses in the temperature range between 300 K and 400 K are shown in Fig. 2. Figure 2(a) shows that the linear resistance increased as the temperature increased, and the zoomed-in resistance response curve at

300 K after the voltage pulse is shown in Fig. 2(b). The resistance increased as the pulse time increased during the earlier 10 μs, and then tended to saturate during the latter 10 μs. According to the resistance response at a certain ambient temperature, the temperature rise can be calculated.

Considering the uncertainty induced by the measurement setup, we took the average resistance of the third hundred nanosecond as the initial resistance R_0. The temperature coefficient of resistance (TCR) was obtained by measuring the resistance R at different temperatures T and was calculated as

$$\alpha = \frac{1}{R}\frac{\mathrm{d}R}{\mathrm{d}T}. \tag{1}$$

The dependence of the initial resistance R_0 and the temperature coefficient α on temperature is summarized in Fig. 3. Figure 3(a) shows R at temperatures between 300 K and 400 K, and figure 3(b) shows the TCR of the Ni strip in the same temperature regime. It can be found that R increases linearly as the temperature increases, while the trend of TCR change is the reverse.

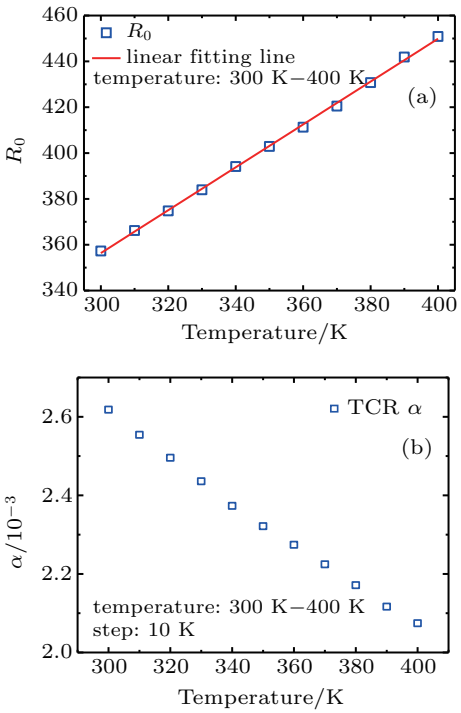


Fig. 3. (a) The initial resistances R_0 extracted from the resistance distribution varied as the pulse time increased, and R_0 was calculated by averaging the resistances at the third hundred nanosecond. (b) The temperature coefficient distribution at different environment temperatures ranging from 300 K to 400 K in steps of 10 K.

The temperature rise ΔT can be calculated using the following equation:

$$\Delta T = (R - R_0)/(\alpha R_0). \tag{2}$$

According to the THS model, the temperature in the metal strip can also be characterized as

$$\Delta T = [P_0/(\gamma\sqrt{\pi}\kappa)]f(\tau), \tag{3}$$

where P_0 is the heat generation power per unit length, γ is a geometrical parameter, h is the length of the heater, κ is the thermal conductivity, and t is the measurement time.[17] The γ parameter is related to the sample structure[18] and the optical values of γ with different structures are shown in Fig. 4. Here, it was set as 2 for the same structure in Fig. 4(c).

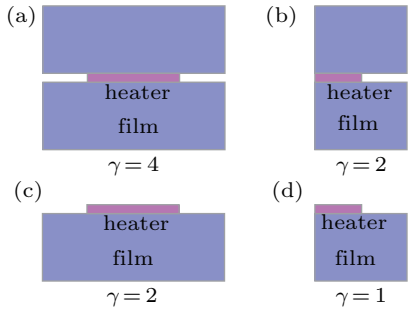


Fig. 4. Geometrical parameter γ is related to the measurement structure, and (a) $\gamma = 4$, (b) $\gamma = 2$, (c) $\gamma = 2$, (d) $\gamma = 1$ for the structures shown.

The thermal impedance R_{th} is defined as $\Delta T/P_0$, and therefore R_{th} can be expressed as

$$R_{\mathrm{th}} = \frac{1}{2\sqrt{\pi}\kappa}f(\tau). \tag{4}$$

When the width of the strip d is small, $f(\tau)$ is approximately proportional to $\ln t$ as given by

$$f(\tau) \approx \frac{1}{2\sqrt{\pi}}\ln\tau^2, \tag{5}$$

$$\tau = 2\sqrt{Dt}/d, \tag{6}$$

where D is the thermal diffusivity of the film, and τ is the characteristic time. Therefore, the thermal conductivity is related to the slope of R_{th} versus t in the log scale, and is given by

$$\kappa^{-1} = 4\pi\frac{\mathrm{d}R_{\mathrm{th}}}{\mathrm{d}\ln t}. \tag{7}$$

Figures 5(a) and 5(b) show the R_{th} distributions of the control sample and of the sample with $T_{\mathrm{SOI}} = 30$ nm in the same temperature region, respectively. Comparing the slope from different SOI thicknesses with that from the control sample in the same linear region, the thermal conductivity of different thin silicon films can be obtained.

As shown in Fig. 5(c), the film thermal conductivity $\kappa_{\mathrm{Si,film}}$ can be calculated as

$$\kappa_{\mathrm{Si,film}}^{-1} = 4\pi\left(\frac{\mathrm{d}R_{\mathrm{th,control+Si,film}}}{\mathrm{d}\ln t} - \frac{\mathrm{d}R_{\mathrm{th,control}}}{\mathrm{d}\ln t}\right), \tag{8}$$

where $R_{\mathrm{th,control}}$ is the thermal impedance of the control sample, shown by blue symbols, and $R_{\mathrm{th,control+Si,film}}$ is the thermal impedance of the $T_{\mathrm{SOI}} = 30$ nm sample, shown by yellow symbols.

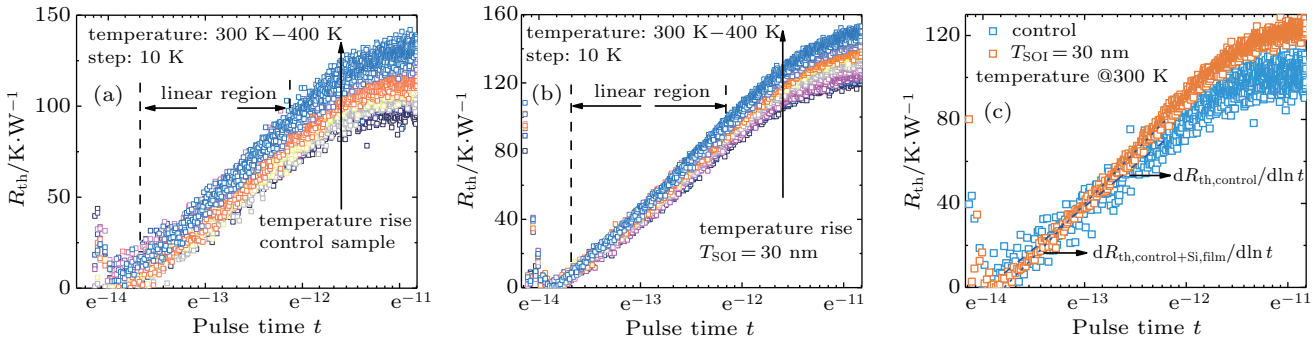


Fig. 5. The linear region in thermal resistance distribution versus pulse time in log scale. The thermal resistance increased as temperature increased. (a) The control sample without SOI, (b) the sample with SOI thickness of 30 nm, and (c) the schematic of $\kappa_{Si,film}$ extraction.

3. Results and discussion

The extracted thermal conductivities of the silicon films with different thicknesses are shown in Fig. 6(a). Black symbols represent the thermal conductivity of 30 nm SOI, red symbols are the thermal conductivity of 17 nm SOI, and the blue symbols are for 10 nm SOI. As the temperature increases, the conductivity does not decrease significantly, which is a similar trend to that in in-plane data.[19] This implies that internal scattering is not dominant in the present temperature regime since the Umklapp scattering has $1/T$ dependence on temperature.[20] The ratio of the thermal conductivity of 30 nm, 17 nm, and 10 nm SOI over the bulk value is only $\sim 6.9\%$, $\sim 4.3\%$, and $\sim 3.8\%$ at 300 K, respectively. This extremely low thermal dissipation in devices or circuits may result in hot spots, which interrupts smooth operation. Also, we measured the temperature response of films of the above three thicknesses in the low temperature region (75–285 K). The data are shown in Fig. 6(b). The values at a cryogenic temperature from 75 K to 210 K gradually increase as temperature rises. Beyond 210 K, the thermal conductivity goes up to a certain level. The positive temperature dependence indicates that the phonon-boundary scattering dominates in ultra-thin silicon films below 210 K.

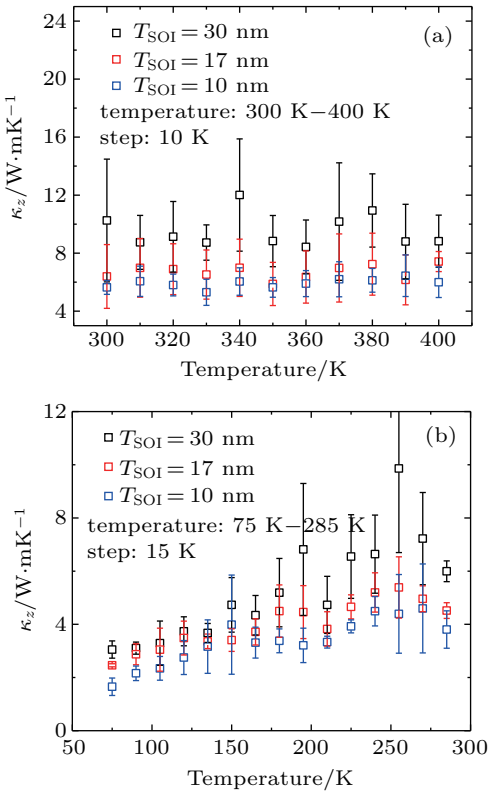


Fig. 6. The cross-plane thermal conductivity extracted at temperatures (a) from 300 K to 400 K, and (b) from 75 K to 285 K.

According to the work reported in Ref. [21], the average mean free path (MFP) in nanostructured silicon films is about 200 nm. As the film thickness in this work is much smaller than the MFP, phonons can carry heat without internal scattering. In Ref. [12], a ballistic heat transport model based on extended irreversible thermodynamics was used to calculate the cross-plane thermal conductivity. The EIT model was first proposed by Alvarez and Jou, and was very effective for predicting cross-plane thermal conductivity in silicon films.[10] The analysis form is given by

$$\kappa_{film,Si} = \frac{\kappa_{bulk} L^2}{2\pi^2 l^2}\left(\sqrt{1+4(\pi l/L)^2}-1\right), \tag{9}$$

where $\kappa_{film,Si}$ is the cross-plane thermal conductivity, κ_{bulk} refers to the silicon bulk thermal conductivity, L is the thickness of the thin film, and l is the phonon mean free path. When L is smaller than l, phonons can transport heat without internal scattering, and the above formalism can be simplified as

$$\kappa_{film,Si} = \frac{\kappa_{bulk}}{\pi}\frac{L}{l}. \tag{10}$$

Comparison of the calculated results from the EIT model and the experiment data is shown in Fig. 7(a). The bulk silicon thermal conductivity κ_{bulk} and the average mean free path l are cited from the references.[9,22] It can be found that a satisfactory match between the calculated and experimental results is achieved. This indicates that the ballistic phonon transport dominates in vertical heat conduction in ultra-thin silicon films below 50 nm. The underestimate of $T_{SOI} = 30$ nm in the low temperature region may be attributed to the poor interface quality between Al_2O_3 and SOI films, which could result in a large interface thermal resistance increase as the temperature decreases. The extracted thermal conductivities also

match well with the data simulated using the Landauer method as show in Fig. 7(b).[23] The consistency between the experiment data and the simulation values validates the feasibility of the ultrafast THS method for cross-plane thermal conductivity extraction.

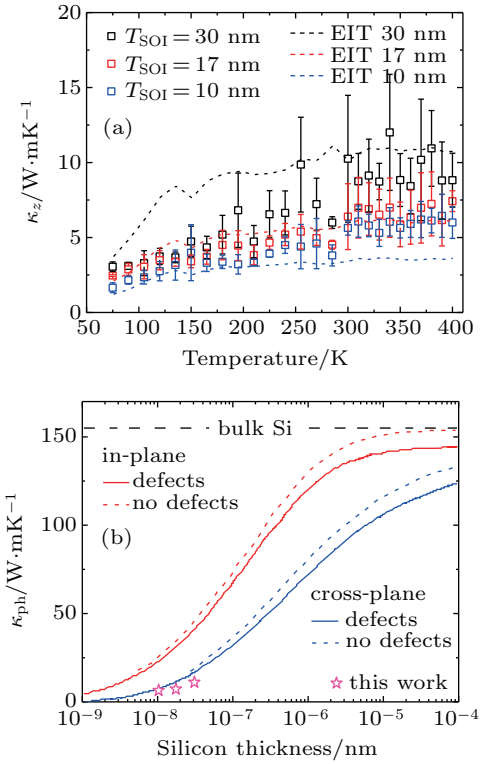


Fig. 7. The comparison of experimental data with the values calculated from (a) the EIT model from the low temperature region 75 K to high temperature 400 K, (b) the Landauer method in Ref. [23].

4. Conclusion

The sub-20 μs ultra-fast THS method has been implemented for measuring the cross-plane thermal conductivity of ultra-thin silicon films. The cross-plane thermal conductivities of 30 nm, 17 nm, and 10 nm thin silicon films were successfully extracted for the first time. The ratio of the thin film's thermal conductivity over the bulk value is only about 6.9%, 4.3%, and 3.8% at 300 K, respectively. The experimental data show a satisfactory agreement with the EIT model and the Landauer model, indicating ballistic phonon transport in the vertical temperature gradient direction of the silicon films. The measured thermal conductivities of silicon films provide important guidance in dealing with the self-heating related issues in advanced transistors. The results in this study also suggest possible thermoelectric applications for ultra-thin silicon films.

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