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Design, fabrication, and study of 10-kV silicon-carbide p-channel IGBTs with hexagonal cells and step space modulated junction termination extension

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Design and fabrication of 10-kV silicon–carbide p-channel IGBTs with hexagonal cells and step space modulated junction termination extension*

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10-kV 4H–SiC p-channel insulated gate bipolar transistors (IGBTs) are designed, fabricated, and characterized in this paper. The IGBTs have an active area of 2.25 mm^2 with a die size of 3 mm× 3 mm. A step space modulated junction termination extension (SSM-JTE) structure is introduced and fabricated to improve the blocking performance of the IGBTs. The SiC p-channel IGBTs with SSM-JTE termination exhibit a leakage current of only 50 nA at −10 kV. To improve the on-state characteristics of SiC IGBTs, the hexagonal cell (H-cell) structure is designed and compared with the conventional interdigital cell (I-cell) structure. At an on-state current of 50 A/cm^2, the voltage drops of I-cell IGBT and H-cell IGBT are 10.1 V and 8.3 V respectively. Meanwhile, on the assumption that the package power density is 300 W/cm^2, the maximum permissible current densities of the I-cell IGBT and H-cell IGBT are determined to be 34.2 A/cm^2 and 38.9 A/cm^2 with forward voltage drops of 8.8 V and 7.8 V, respectively. The differential specific on-resistance of I-cell structure and H-cell structure IGBT are 72.36 mΩ·cm^2 and 56.92 mΩ·cm^2, respectively. These results demonstrate that H-cell structure silicon carbide IGBT with SSM-JTE is a promising candidate for high power applications.

Keywords: silicon carbide, power device, insulated gate bipolar transistors (IGBTs), high voltage

PACS: 85.30.Tv, 85.30.Pq, 85.30.De **DOI:** 10.1088/1674-1056/28/6/068504

1. Introduction

Due to the excellent physical and electrical properties of silicon carbide (SiC) material, such as wide bandgap, high critical field and high electron saturation drift velocity nature, 4H–SiC devices have emerged as an attractive alternative to silicon devices for high voltage applications.[1–3] A thick epilayer[4] is needed to block the high voltage for high-voltage applications, such as high-voltage direct current (HVDC) transmission and smart grid. Several investigations have been conducted on SiC MOSFETs with blocking voltage over 10 kV.[5] However, these high-voltage unipolar devices suffer a high resistance of the thick drift layers. To solve this problem, the carrier modulation effect of bipolar device is introduced to reduce the resistance. Power IGBTs in 4H–SiC are very attractive to high power switching applications due to their low differential specific on-resistance and moderate switching loss. Significant progress has been made for both n-channel[6–9] and p-channel[10–13] SiC IGBTs in the past decade.

One of the main issues that limit the static characteristic of SiC devices is the poor channel mobility.[14] The acceptor-like and donor-like interface state near the band edge are detrimental to electron and hole mobility. The density of these donor-like interface states in SiC/SiO_2 interface is extremely high so that the channel mobility of p-channel IGBT is lower than that of Si IGBT. The hexagonal-cell[15] (H-cell) structure is adopted as a solution to the high channel resistance problem in p-channel SiC IGBT for the larger width-to-length ratio (W/L ratio). Another issue is that the relatively high leakage current in the termination region of IGBT device can strongly degrade the blocking performance of SiC IGBT. To reduce the leakage current, especially for ultra-high voltage device, compound terminal structures are generally used. In this paper, 10-kV p-channel SiC IGBTs with H-cell and I-cell layouts are designed, fabricated and characterized. On-state comparisons between H-cell and I-cell are comprehensively studied. Moreover, the leakage current depressing effects of different terminal structures are also presented and demonstrated for the improvement of the off-state performance of 10-kV 4H–SiC

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IGBTs.

2. Design and fabrication

A schematic cross-section of a single unit cell of the SiC IGBT is shown in Fig. 1. A planar gate structure was chosen because of its process simplicity and high gate oxide reliability. All the critical epitaxial layers were grown on a 350-μm-thick 4-inch (1 inch = 2.54 cm) 4° off-axis n-type 4H–SiC substance. The p-type buffer layer had a thickness of 2 μm and a doping concentration of 2×10^{17} cm^{-3}, and the p-drift layer possessed a thickness of 100 μm and a doping concentration of 2×10^{14} cm^{-3}. The carrier lifetime of the thick drift layer was measured to be 1.2 μs by microwave photoconductivity decay method. As is well known, the reliability of gate oxide[16] in SiC MOS-based device is a critical factor for the blocking performance. Generally, the narrow JFET region can shield the gate oxide from high electric field strength in the blocking mode. However, the narrow JFET region will also increase the JFET resistance strongly and reduce the carrier injection efficiency. To ensure the reliability of oxide layer and improve the on-state performance, the JFET length of the I-cell structure was adopted to be 10 μm and that of the H-cell structure was taken as 8 μm. Thus, the maximum electric fields in the gate oxide of both devices are reduced below 4.5 MV/cm at a 10-kV blocking voltage.

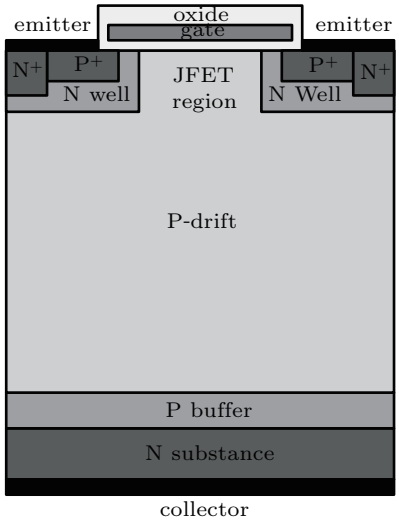


Fig. 1. (a) Schematic cross-section of a single unit cell of SiC IGBT.

Appropriate edge terminations were designed to relieve edge field crowding effect on the crowding electric field around the edges of the devices. To achieve a nearly ideal breakdown voltage, three junction termination extension structures (JTE) were designed, which are 200-μm wide double-zone JTE, 500-μm wide double zone JTE without and with field limiting rings at various depths called SSM-JTE structures as shown in Fig. 2. Like a common space modulated JTE (SM-JTE),[17] floating field rings are inserted close to each zone of double-zone JTE to obtain a laterally tapered distribution for an effective JTE dose in the SSM-JTE structure.[18] The depths of the double zones in SSM JTE feature different values, while the doping concentration of each implantation step is identical. It is intended to avoid the influence of activation rate on the doping concentration in the fabricated device. Thus, a wide tolerance interval is obtained for the JTE doping concentration. The total length of the SSM-JTE structure is 530 μm.

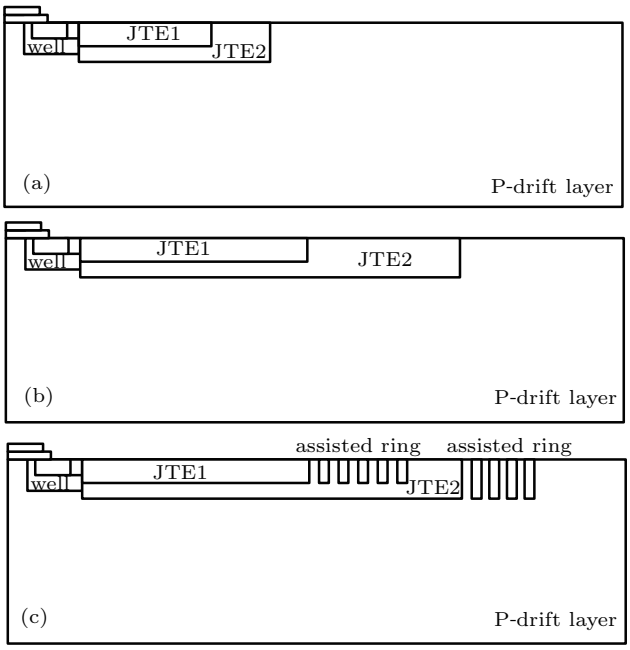


Fig. 2. (a) Structure of 200-μm JTE, (b) 500-μm JTE, (c) step space modulated JTE.

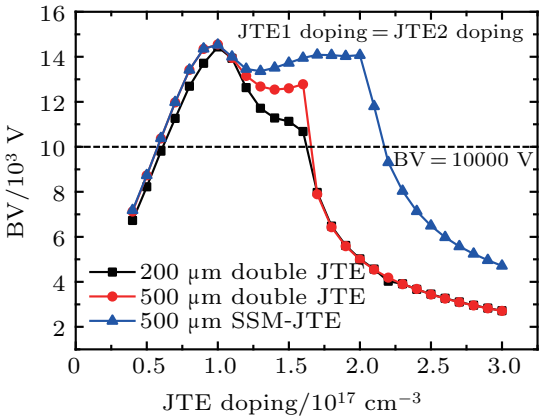


Fig. 3. JTE-dose-dependent breakdown voltages for p-channel IGBTs.

Simulated breakdown voltages of the three edge termination structures with different JTE doses are given in Fig. 3. The device simulation was performed using Sentaurus TCAD software. To reduce the process errors, the ratio of the JTE1 dose to the JTE2 dose was fixed at 1:1 while the ratio of the JTE1 length to the JTE2 length was kept at 13:20. The dashed line was used to note the JTE dose range to obtain a breakdown

voltage over 10 kV. It can be seen that a larger JTE area can make a feasible dose range slightly wider. Furthermore, the introduction of excess assist rings in SSM-JTE can extend the feasible dose range greatly and increase the maximum blocking voltage.

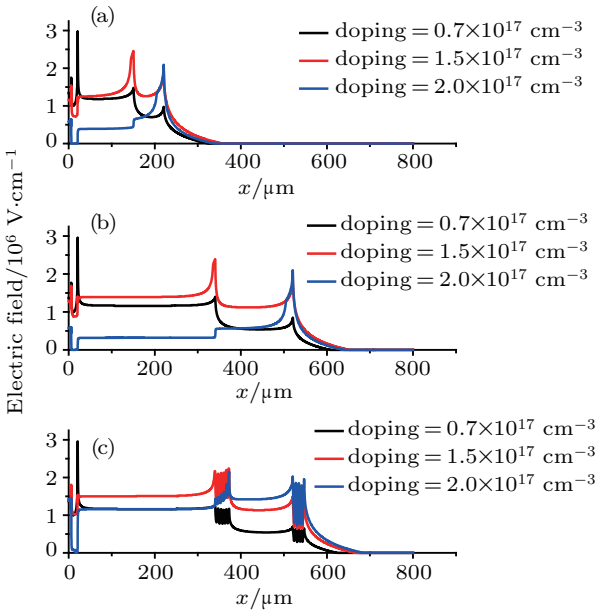


Fig. 4. . Distributions of simulated electric fields at blocking voltage 10 kV.

The distributions of the simulated electric fields with a 0.6-μm depth at a blocking voltage of 10 kV are shown in Fig. 4. Owing to the alleviated electric field around the JTE2 corner, a wide allowable range of doping concentration was achieved in the SSM-JTE. It can be seen that the breakdown occurred at the inner corner of the termination with a low JTE doping level (black curve in Figs. 4(a)–4(c)). As the doping concentration increases, the electric field decreased at the inner corner of the termination, and increased at the JTE1 corner and the JTE2 corner, which are shown by the red curves in Figs. 4(a)–4(c). For double-zone JTE, if the doping concentration was larger than the optimized value, the electric field at the JTE1 corner decreased while the electric field at the JTE2 corner increased, leading to a fast sharp decrease of breakdown voltage. This phenomenon can be seen in the blue curves of Figs. 4(a) and 4(b). However, in the case of SSM-JTE, if the doping concentration was larger than the optimized value, the blocking voltage decreased slightly. This is for the reason that the inner assist ring of the SSM-JTE can share the potential and the outer assist ring can alleviate the electric field crowding, thus the electric field in whole area can be constrained, which can be seen in Fig. 4(c). Consequently, a much wider feasible dose range can be obtained in the SSM-JTE structure. The theoretical blocking voltage obtained by simulation was expected to be 13000 V.

To reduce the on-state resistance, the channel of the 4H–SiC IGBT was formed through a self-alignment method,[19] as mentioned below. The poly-silicon was deposited and etched to serve as the n-well implantation mask. After n-well implantation,[20] an appropriate thickness of SiO_2 was deposited and followed by depositing a layer of titanium. The titanium layer was etched and served as the source implantation mask together with SiO_2 and left poly-silicon in the last step. The channel length of the devices was about 0.5 μm. The JTE based termination was fabricated around the device periphery, which has been discussed in the last section. All the implantations were activated in argon at 1650 °C, and a carbon cap was utilized to suppress surface reconstruction and silicon atom evaporation of 4H–SiC epilayer. The gate oxide[21] of 50 nm was grown in dry O_2 ambient and then annealed in nitric oxide[22] at 1250 °C to reduce the interface trap density of SiO_2/4H–SiC interface and fixed charges of the gate oxide. After the gate oxide process, the poly-silicon was deposited on the gate oxide as a gate electrode. Aluminum/ titanium contacts[23] were deposited as the p-type base ohmic contact metals, while nickel was deposited as an n-type source and back ohmic contact metal, followed by a rapid thermal annealing (RTA) step. The IGBTs have an active area of 2.25 mm^2, and a die size of 3 mm×3 mm. Figure 5 shows a photograph of the fabricated IGBT wafer and the top view of SiC IGBT with I-cell and I-cell.

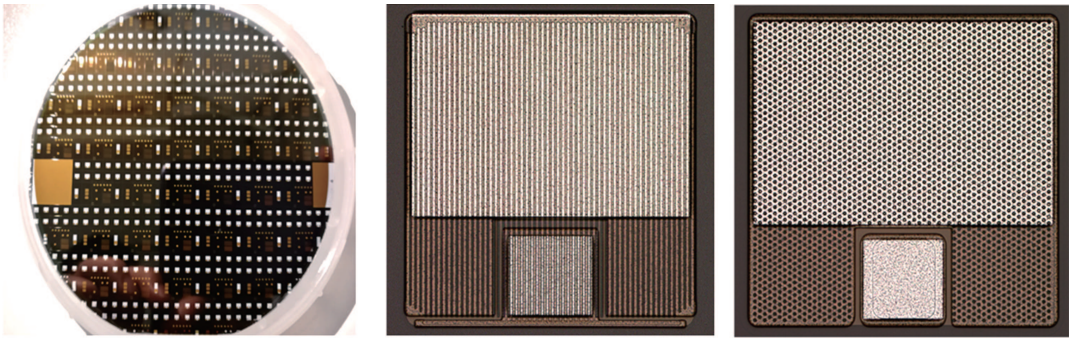


Fig. 5. (color online) (a) Photograph of the fabricated IGBT wafer, (b) top-view photography of SiC IGBT with I-cell layout, (c) top-view photography of SiC IGBT with H-cell layout.

3. Results and discussion

The room temperature blocking characteristics of the H-cell 4H–SiC p-channel IGBTs are shown in Fig. 6, and the inset shows the curves in logarithmic coordinates. All the breakdowns occur at the edge of the termination. The terminal efficiency of the SSM-JTE is more than 71.4%. The IGBT blocking characteristic is tested by using Agilent B1505 A with the gate that is grounded with the emitter. During the blocking characteristic test, the wafer is immersed in fluorinert during the test to prevent it from arcing. It can be seen that the SSM-JTE structure shows the best blocking characteristic. The IGBTs with SSM-JTE structure show a leakage current of 50 nA at −10 kV, while the IGBTs with 200 μm and 500-μm wide double JTE show a leakage current of 970 nA and 590 nA, respectively, which are consistent with the simulation results discussed in the last section.

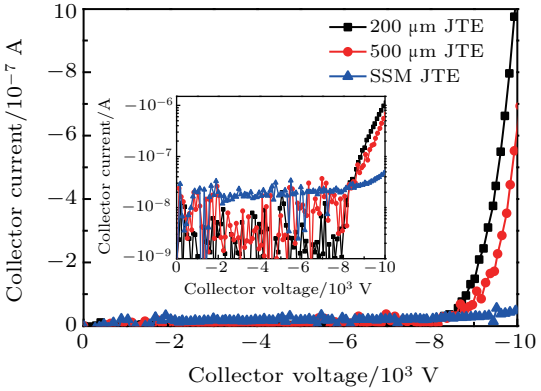


Fig. 6. Room temperature blocking characteristic of the H-cell 4H–SiC p-channel IGBTs.

Figure 7(a) and 7(b) show on-state characteristics of the 4H–SiC p-channel I-cell and H-cell IGBTs with negative potentials on the gate and collector at room temperature, respectively. The collector current density is plotted against the collector voltage in a gate bias range from 0 V to -30 V in steps of −5 V. The turn-on voltage of fabricated IGBT device is about −3 V, which is comparable to the built-in voltage of substance/buffer PN junction. However, the threshold voltage of fabricated p-channel IGBT is approximately −12 V, which indicates that there are a large number of fixed charges[24] in gate oxide. The simulated SiC p-IGBT on-state characteristics with a gate voltage of −30 V are also shown in Fig. 7 for comparison. The relatively high resistance of fabricated IGBT is mainly due to three reasons: (i) the surface recombination reduces the lifetime of ambipolar carriers near the interface; (ii) the relatively high p-type ohmic resistance leads to a large voltage drop at the source contact; and (iii) the graded pn junction between the buffer layer and the emitter layer reduces the injection efficiency of the emitter in the IGBT. At an on-state current of 50 A/cm^2, the voltage drops of I-cell and H-cell IGBTs are 10.1 V and 8.3 V, respectively. Assuming that the IGBT devices must operate under a 300-W/cm^2 package power dissipation limit,[25] the IGBT with I-cell structure and H-cell structure have a working current density of 34.2 A/cm^2 at a forward voltage of 8.8 V and 38.9 A/cm^2 at a forward voltage of 7.8 V, respectively. Meanwhile, the differential specific on-state resistances at 300 W/cm^2 are 72.36 mΩ·cm^2 and 56.92 mΩ·cm^2, respectively. The simulated on-state characteristics of 4H–SiC n-channel MOSFETs and p-channel MOSFETs with a channel mobility of 25 cm^2/V·s are also shown in Fig. 7, and the gate voltage is set to be 30 V for n-channel MOSFETs and −30 V for p-channel MOSFETs. Under the same package power dissipation, the current density of SiC n-channel MOSFET and p-channel MOSFET are only 26 A/cm^2 and 8.9 A/cm^2 with a differential specific differential on-state resistance of 350 mΩ/cm^2 and 3370 mΩ/cm^2, respectively. This indicates that a strong conductance modulation effect cis formed in the drift region of the SiC IGBT device when it is at on-state.

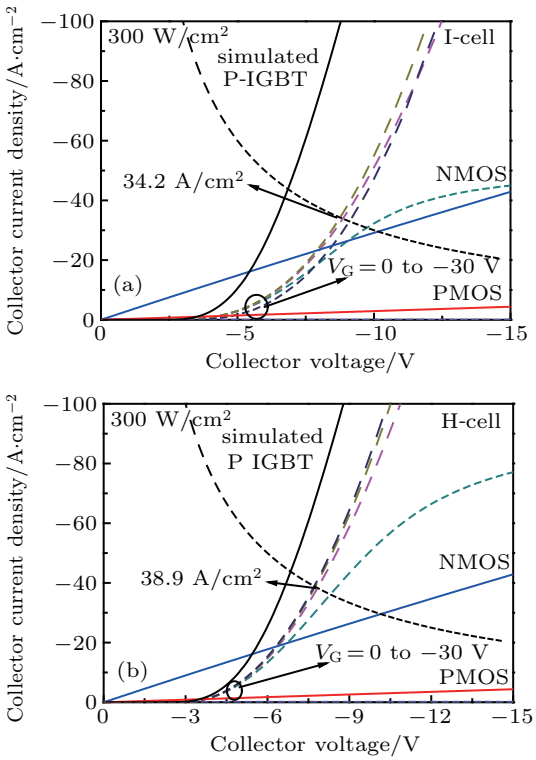


Fig. 7. On-state characteristics of the 4H–SiC p-channel IGBT with (a) I-cell and (b) H-cell.

The on-state characteristic of H-cell structure is better than that of I-cell structure, which is attributed to the fact that the H-cell structure has a larger W/L ratio (410000) than the I-cell structure (whose W/L ratio is 290000). The larger channel density and W/L ratio make the IGBT with H-cell have a superior on-state characteristic. Therefore the H-cell structure is more suitable for SiC p-IGBTs.

Figure 8 shows the relationship between the differential specific on-resistance and blocking voltage for each of the fabricated SiC IGBTs and other reported results. The straight

lines represent the theoretical limitation of the trade-off between the on-resistance and the reverse blocking voltage for each of the SiC unipolar devices. It can be seen that our devices have a better performance than the devices developed by AIST and CETC. Both of the I-cell devices and H-cell devices have already broken through the limit of SiC unipolar devices. To improve the performance of SiC IGBT device, three approaches can be adopted: increase the channel mobility,[26] extend the ambipolar carrier lifetime,[27] and increase the carrier injection efficiencies.[28]

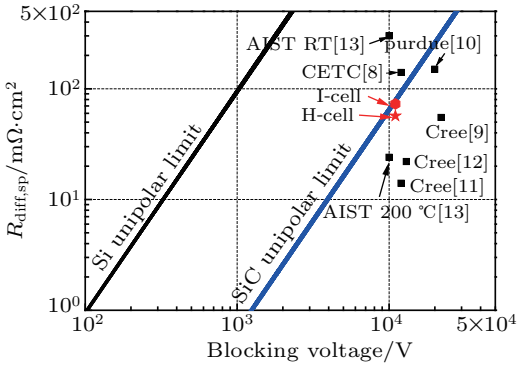


Fig. 8. Relationship between the differential specific on-resistance and blocking voltage.

4. Conclusions

The 10-kV SiC p-channel IGBTs with hexagonal cells and interdigital cells are designed and fabricated successfully. The die size of the p-channel IGBTs is 3 mm×3 mm, with an active area of 2.25 mm^2. The test results show that the voltage drop of I-cell and H-cell IGBTs are 10.1 V and 8.3 V, at an on-state current of 50 A/cm^2, respectively. At 300 W/cm^2, the maximum permissible current density of the I-cell and H-cell IGBTs are determined to be 34.2 A/cm^2 and 38.9 A/cm^2 with forward voltage drops of 8.8 V and 7.8 V, respectively. The differential specific on-resistance of I-cell and H-cell structure IGBTs are 72.36 mΩ·cm^2 and 56.92 mΩ·cm^2, respectively. The SSM-JTE structure shows a better blocking characteristic than the conventional double-zone JTE structure. The IGBTs with SSM-JTE structure show a leakage current of 50 nA at a collector voltage of −10 kV. These results demonstrate that the SiC IGBT with H-cell structure and SSM-JTE structure are both promising candidates for high power applications.

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