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Research on SEE mitigation techniques using back junction and p^+ buffer layer in domestic non-DTI SiGe HBTs by TCAD*

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In this paper we investigate two techniques for single event effect (SEE) mitigation by using back junction and p^+ buffer layer in non-deep trench isolation (DTI) domestic silicon–germanium heterojunction bipolar transistors (SiGe HBTs) based on technology computer aided design (TCAD) simulation. The effectiveness of the two mitigation techniques and the influence of various structure parameters are investigated. Simulation results indicate that the two techniques are more effective in reducing collector charge collection induced by heavy ions striking at positions outside the collector–substrate (C–S) junction where charge collection is dominated by diffusion. By properly adjusting the parameters, charge collection of events outside the C–S junction can be reduced by more than an order of magnitude, while charge collection of events in the device center is halved without affecting the direct current (DC) and alternating current (AC) characteristics of the SiGe HBTs.

Keywords: silicon–germanium HBT, single event effect, mitigation technique, TCAD simulation

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1. Introduction

Microelectronics used for lunar and deep space exploration may be exposed to both extremely low temperatures and various energetic particles in space. Silicon–germanium heterojunction bipolar transistors (SiGe HBTs) are attractive for these space applications due to the superior low-temperature performance and excellent hardness to both total ionizing dose (TID) and displacement damage (DD) without intentional hardening design.[1–5] However, the main problem of using the unhardened SiGe HBTs in space missions is their susceptibility to single event effect (SEE) due to the existence of the large-area collector–substrate (C–S) junction. When the C–S junction is reversely biased, a great number of the excess carriers deposited by high energy particles with tracks passing through or near the junction will be collected, which can disorder the normal working state of the circuits and lead to serious reliability issues for the system.[6] Integrated circuits based on SiGe HBTs have been confirmed to suffer low single event upset (SEU) thresholds and large saturated cross sections.[7–9] Hence, it is crucial to search SEE mitigation techniques for SiGe HBTs aiming at space applications.

Since the SEE results from the collection of excess carriers deposited by incident particles were first identified, there have been in general two kinds of mitigation concepts. The first concept is to reduce the number of excess carriers deposited in the sensitive region. A representative technique is to use SiGe HBTs in the inverse-mode.[10] This method electrically swaps the emitter for the collector, which isolates the electrical collector (physical emitter) from the lightly doped substrate which is a crucial feature dominating the single event charge collection in bulk SiGe HBTs. However, the problem is that the HBTs are not optimized for inverse-mode so that the performance is significantly degraded.[11] The second concept is to reduce the number of carriers that transport to the collecting node. This path was previously implemented by introducing an additional reverse biased p–n junction formed between the p-substrate and an n^+ guard ring, thus resulting in a secondary electric field.[12] As a result, part of the carriers that are going to be collected by the collector will be collected by the n^+ guarding ring. The added n^+ guard ring is also called dummy collector in Ref. [13]. This technique is effective in reducing charges outside the deep trench isolation (DTI) where the charge collection is dominated by diffusion and it may also lead to area penalty. However, most of the existing mitigation techniques are based on SiGe HBTs fabricated with DTI, while few results concerning the non-DTI SiGe HBTs are available. Although SiGe HBT without DTI has a larger sensitive area than DTI SiGe HBT, its charge collection when the ion penetrates the active region is much smaller than DTI SiGe HBT's, which can lead to a higher SEU threshold.[14]

In this work, we evaluate the effectiveness of two SEE mitigation techniques in domestic non-DTI SiGe HBT based on technology computer aided design (TCAD) simulation. The first is the back junction technique, which was originally presented by Niu *et al.* in DTI SiGe HBT.[15] The basic idea of this technique is to add an n^+ layer several micrometers beneath the subcollector to form a back junction between the substrate and n^+ layer. On the one hand, this layer cut off the

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ion track so that the total quantity of charges that can be collected is limited by the thickness of the substrate above it. On the other hand, the deposited charges will be collected by both the C–S junction and the added back junction. In Ref. [15] that authors mainly considered the condition when the ions strike at the center of the device, where the charge collection is dominated by field-funnelling effect. However, it is also necessary to consider the influence of the back junction on event far from C–S junction in non-DTI SiGe HBT. This event can also result in significant charge collection through diffusion, thus making the sensitive area much larger than the area of the C–S junction.[16] The second technique is to form a p^+ buffer layer around the collector through ion implantation. This p^+ layer provides a region with a high rate of recombination with the excess electrons which are responsible for the charge collection on collector, thus the charge collection on collector will be reduced. Simply increasing the doping level of the entire substrate may also result in reducing charge collection, but this will significantly reduce the substrate resistance and lead to other problems such as substrate coupling in mixed-signal circuits. However, the use of a buffer layer with a thickness of several micrometers can avoid this problem.

Based on three-dimensional (3D) TCAD simulation, a quantitative comparison of heavy ion-induced charge collection is performed between the hardened SiGe HBT and the conventional SiGe HBT. The influence of possible factors are also investigated and the mechanisms are discussed. In addition, the mitigation results by the two techniques are also compared to find their advantages.

2. Device structures

The device investigated is a domestic vertical N–P–N SiGe HBT. The top-down and cross section views of the conventional device obtained by TCAD are shown in Fig. 1(a). The active emitter area is 0.4 μm×6 μm. The intrinsic base region is formed by epitaxially growing the SiGe layer, the content of Ge changes gradually from 0% at the emitter–base junction and the base–collector junction to 20% in the intrinsic base, forming two graded heterojunctions. The thickness of the base is ∼ 0.08 μm. The epitaxial base region is located above the local oxidation of silicon (LOCOS). The C–S junction area is 18 μm×20 μm. The substrate contact is extracted through a heavily doped ring wall at the edge of the device. More information about the device can be found in Refs. [17] and [18]. The TCAD model is calibrated with the parameters measured by using Keithley 4200 and the heavy-ion-induced SEE results.[19–22] The structure of back junction SiGe HBT is shown in Fig. 1(b). An n^+ buried layer below the collector divides the lightly doped substrate into two parts. The part below the n^+ layer has no electrical connects with the substrate, so we call this part the supporting substrate. The part above the n^+ layer is connected to the substrate electrode and this part is the real substrate. In the following parts, the word "substrate" refers to the upper part unless otherwise stated. The contact to n^+ layer is lead out by the n^+ plugs. The thickness of the substrate is denoted as L_s, the thickness of the n^+ layer is denoted as L_n, the doping concentration of the n^+ layer and n^+ plugs is denoted as D_n, the number of n^+ plugs is denoted as N. The structure of the SiGe HBT with a p^+ buffer layer is shown in Fig. 1(c). A p^+ layer with Gaussian doping distribution is formed around the collector. The peak value of the Gaussian profile is denoted as D_p and the depth is denoted as L_p. According to the layouts, no additional area penalty is introduced by the two mitigation techniques.

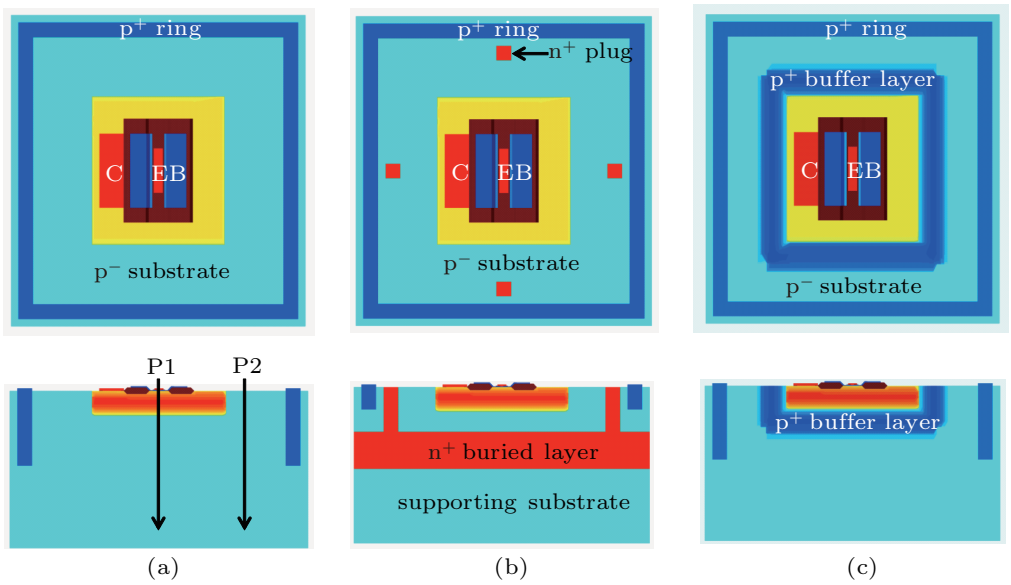


Fig. 1. Top down and cross-section view of (a) conventional HBT, (b) back junction HBT, and (c) buffer layer HBT.

3. Simulation details

In the SEE simulation, a linear charge deposition (LCD) of 0.4 pC/μm, which is equivalent to a linear energy transfer (LET) of 39 MeV·cm^2·mg^{-1} is selected. This LET value is between the LET of 230-MeV Ge (LET = 36.9 MeV·cm^2·mg^{-1}) and 240-MeV Br (LET = 41.8 MeV·cm^2·mg^{-1}). These two ion types are often used in accelerator heavy ion SEE experiments. The ion track is generated by using Gaussian waveform in which the $1/e$ characteristic time scale is 2 ps, the peak of the Gaussian distribution occurs at 5 ps, and the $1/e$ characteristic radius is 0.1 μm. All the ions are at normal incidence. The devices are in the "off state", the emitter, base, and collector are biased with 0 V, while the substrate is biased with −3 V. This is shown to be the most sensitive state to SEE in SiGe circuit. In the back junction structure, the n$^+$ plug is also connected to 0 V to keep the voltage of the n$^+$ layer at the same level as the voltage of the collector. To better evaluate the effectiveness of the two mitigation techniques, the influences of some structure details are considered. For the back junction structure, the influences of L_s, L_n, D_n, and N are investigated; while for the p$^+$ buffer layer structure, the influences of D_p and L_p are investigated.

4. Simulation results and analysis

4.1. Back junction structure

4.1.1. Charge collection characteristics

Figure 2 shows the variations of collector's charge collection with time at two different ion strike positions. The strike positions are marked in Fig. 1(a) with P1 and P2. Position P1 is at $x = 0$ μm (device center) and P2 is at $x = 12$ μm. In the simulated structure, $L_s = 6$ μm, $L_n = 5$ μm, $D_n = 1 \times 10^{20}$ cm^{-3}, and $N = 4$. The simulated time range for conventional device is 10000 ns, while the time range for back junction device is only 100 ns because the charge collections have already been saturated. It is clear that the back junction structure can reduce the charge collection at both ion strike positions. In Fig. 2(a), the charge collection decreases from 3.9 pC in the conventional structure to 1.3 pC in the back junction structure. This decrease can be attributed to two mechanisms. The first mechanism is that the n$^+$ layer reduces the substrate thickness so that the deposited charges that can be collected decrease, and the second one is that the reversely biased back junction will compete with the C–S junction in charge collection so that the charges collected by collector further decrease. Figure 3 shows the electron current profile at 1 ns after the ion has struck at P1. The bi-funnel effect is clearly shown and the excess electrons in substrate are collected through the two paths. For the heavy ion strike at P2, the ion track is outside the C–S junction, the back junction is more effective. As can be seen in Fig. 2(b), the charge collection on collector decreases from 3.9 pC to 0.6 pC. Figure 4 shows the profile of electron current density at 1 ns when heavy ion strikes at P2, and the excess electrons are collected through three paths. Besides being collected by C–S junction and back junction, the electrons are also collected by the junction between substrate and n$^+$ plug which is called S–P junction in this work. In addition, the portion collected by C–S junction is dominated by diffusion, while the portion collected by back junction is dominated by drift-assistant process, therefore the majority of the charges are collected by the back junction and the collector charge collection decreases to a very low level. It is noteworthy that the charge collection at P2 is higher than that at P1 in conventional HBT. This phenomenon is attributed to the special device structure. As introduced above, the substrate contact is connected to a p$^+$ ring wall at the edge, which is shown in Fig. 1(a). When the ion strikes at P2, the ring connected to −3 V can block the rightward diffusion of ion-induced electrons, so that more electrons will diffuse laterally towards the C–S junction.[22] In addition, the ions that strike at P2 only penetrate the lightly doped substrate, while the ions strike at P1 also penetrate the relatively highly doped collector. This means that the ion-induced excess carriers at P2 are free from the severe initial recombination in collector, thus the charge collection is further enhanced.

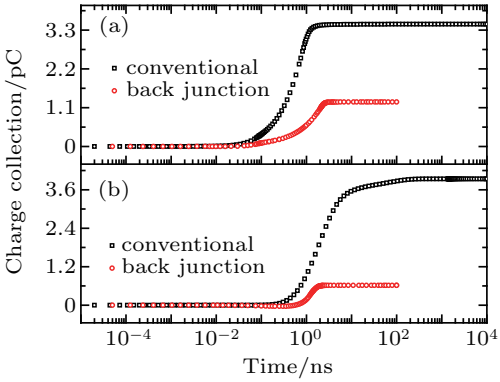


Fig. 2. Plot of charge collection on collector in conventional and back junction HBT at (a) P1 and (b) P2.

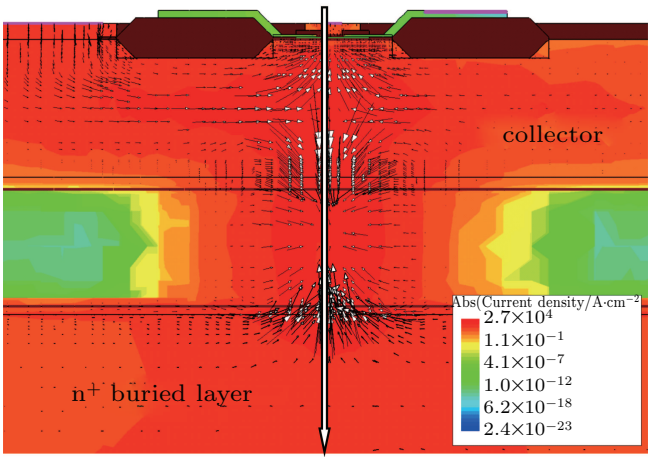


Fig. 3. Profile of electron current density at 1 ns when heavy ion strikes at P1.

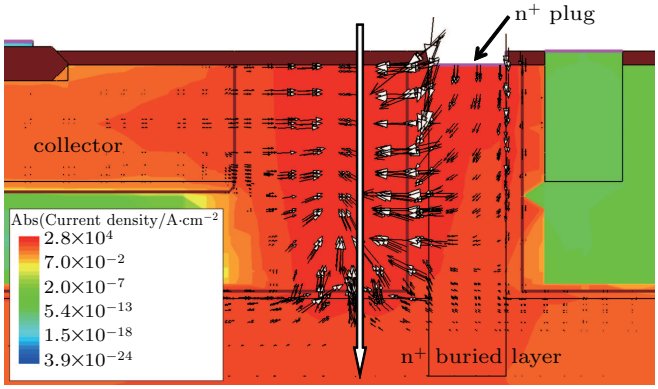


Fig. 4. Profile of electron current density at 1 ns when heavy ion strikes at P2.

4.1.2. Influence of substrate thickness

Figure 5 shows the collector charge collections in back junction structure as a function of L_s. In the simulated structure, $L_n = 5$ μm, $D_n = 1 \times 10^{20}$ cm^{-3}, and $N = 4$. With the decrease of L_s, the collector charge collections induced by events at P1 and P2 both decrease monotonically. With a substrate thickness of 5 μm, the collector charge collection decreases to 1.1 pC at P1 and 0.5 pC at P2. This trend is attributed to the fact that the quantity of deposited charges decreases with the substrate thickness decreasing, and this condition is identical for strike positions both inside and outside the C–S junction. However, it is not feasible to reduce L_s without restriction. The remaining thickness between collector and n$^+$ layer must be large enough to prevent punch through. Although higher doping concentration of the substrate may help to alleviate this problem, it can also lead to other problems (as mentioned earlier).

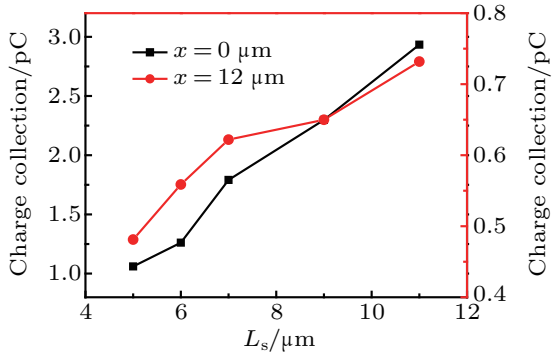


Fig. 5. Plot of collector charge collection in back junction device versus L_s at $x = 0$ μm and 12 μm.

4.1.3. Impact of doping level and thickness of the n$^+$ layer

Figure 6 shows the charge collection on collector in back junction device as a function of D_n. In the simulation model, $L_s = 6$ μm, $L_n = 5$ μm, and $N = 4$. The collector charge collection decreases monotonically with the increase of D_n before 1×10^{19} cm^{-3}, then the decrease reaches saturation. As described above, one of the mechanisms by which the n$^+$ layer reduces collector charge collection is that it divides the initial substrate into two parts and it prevent excess carriers from the supporting substrate from going to the upper part. However, for the n$^+$ layer with a relatively low doping level, the extremely high carrier concentration around the ion track ($> 10^{18}$ cm^{-3}) may neutralize the blocking effect of the layer and form a path from the supporting substrate to the substrate, thus increasing the collector charge collection. With the increase of doping level, the n$^+$ layer can finally eliminate the carriers from the supporting substrate and the decrease of charge collection reaches saturation. Similarly, the n$^+$ layer thickness L_n can also affect the charges from the supporting substrate. Figure 7 shows collector charge collections at P1 and P2 of device with different L_n values. In the simulation models, L_s, D_n, and N are fixed at 5 μm, 1×10^{20} cm^{-3}, and 4, respectively. Collector charge collection decreases monotonically with the increase of L_n. On the one hand, thicker n$^+$ layer can block the electrons from the supporting substrate more effectively. On the other hand, a thicker n$^+$ layer can reduce the thickness of the supporting substrate so that electrons deposited there decrease since the value of L_s cis identical in all models.

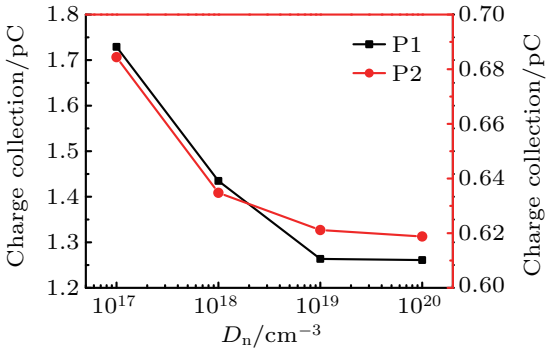


Fig. 6. Plot of collector charge collection of back junction device *versus* D_n for P1 and P2.

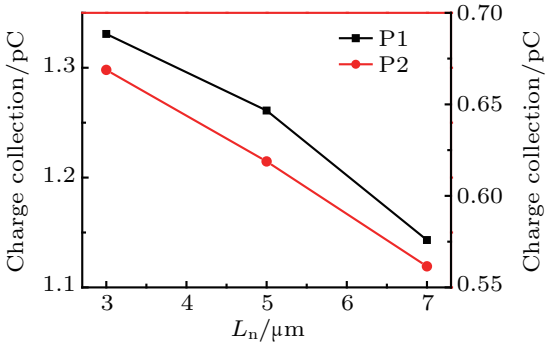


Fig. 7. Plot of collector charge collection of back junction device *versus* L_n for P1 and P2.

4.1.4. Influence of n$^+$ plug number

The n$^+$ plugs are used for contacting the n$^+$ buried layer. The structures in the above sections have four plugs as shown in Fig. 1(b). In this subsection, we add another four n$^+$ plugs

at the corners as shown in Fig. 8. The simulation results of collector charge collection are shown in Table 1. For the heavy ion strike at P1, the influence of plug number seems to be minor, while for the heavy ion strike at P2, the structure with eight plugs results in a further decrease of charge collection compared with the four-plug structure. Based on the result in Fig. 4 concerning the collecting path of ion-induced excess electrons in substrate, this disparity can be explained as follows. For the strike position at P1, the electrons are collected either by the C–S junction or by the back junction, thus the increase of plugs will deliver little influence. On the contrary, for strike position outside C–S junction, some excess electrons are collected by the S–P junctions. Increasing the plug number simply enlarges the total S–P junction area in the device so that more electrons are collected by the plugs. In the SiGe circuits, more n^+ plugs can also be placed in the area between adjacent HBTs to obtain better mitigation results while resulting in no area penalty.



Fig. 8. Top view of back junction device with eight plugs.

Table 1. Collector charge collections in devices with different plug numbers.

	P1	P2
Conventional	3.5 pC	3.9 pC
4 plugs	1.3 pC	0.6 pC
8 plugs	1.2 pC	0.3 pC

4.2. Buffer layer structure

4.2.1. Charge collection characteristics

Figure 9 shows the plot of collector charge collection *versus* time at P1 and P2. In the simulated structure, $D_p = 1 \times 10^{20}$ cm^{-3} and $L_p = 2$ μm. When the ion strikes at P1, the collector charge collection is almost halved by the p^+ buffer layer from 3.5 pC in the conventional device to 1.8 pC (see Fig. 9(a)). The dominant mechanism is that the p^+ buffer layer cuts the ion track into two sections so that the field-funneling effect is suppressed and excess carriers generated below the buffer layer are prevented from transporting to the C–S junction due to the high recombination rate. Figure 10 shows the profile of total recombination rate in the device at 100 ps after the ion has struck at P1. A region with high recombination rate in the buffer layer is clearly shown. In order to make a comparison easy, the recombination rate at 100 ps is extracted as a function of track depth in both the conventional and the buffer layer HBTs and the results are plotted in Fig. 11. It is clear that the recombination rate in the center of buffer layer region is much higher than that in the conventional device, forming a barrier on the transporting path to C–S junction. As for the event at P2, charge collection is dominated by diffusion. Without the assistant of electric field, the transport of the excess carriers is slow and the recombination in the buffer layer results in a better mitigation result. Figure 12 shows the profile of total recombination rate in the device at 2 ns after the ion has struck at P2. A high recombination region enwraps the right part of collector. Consequently, the collector charge collection decreases from 3.9 pC in the conventional device to 0.33 pC (see Fig. 9(b)).

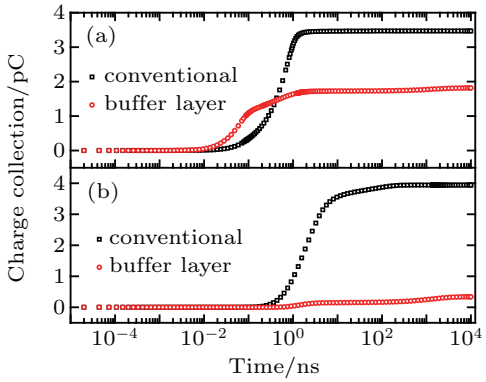


Fig. 9. Plot of charge collection on collector *versus* time at (a) P1 and (b) P2 in conventional and buffer layer HBT.

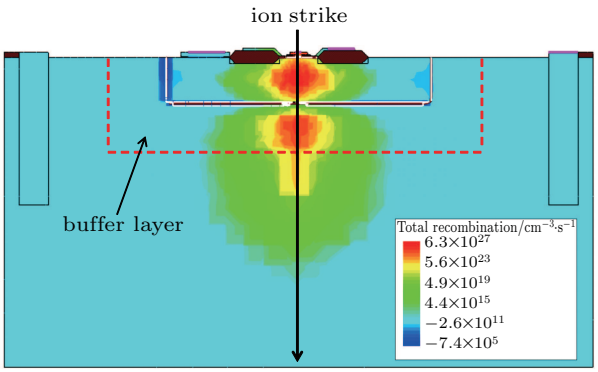


Fig. 10. Profile of recombination rate in HBT with buffer layer 100 ps after ion has struck at P1.

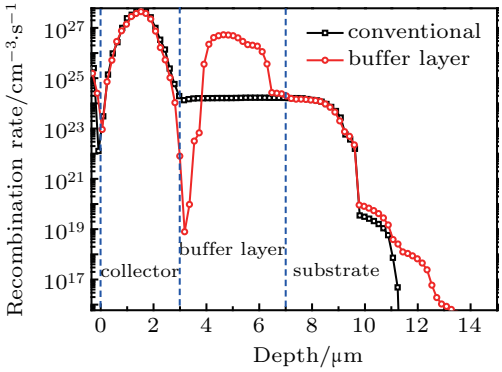


Fig. 11. Plot of recombination rate at 100-ps depth at P1 for conventional and buffer layer device.

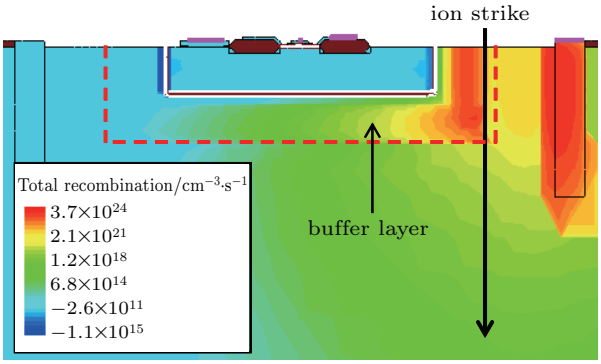


Fig. 12. Profile of recombination rate in HBT with buffer layer 100 ps after ion has struck at P2.

4.2.2. Influence of peak doping concentration and depth of Gaussian profile

Figure 13 shows the collector charge collection in devices with different D_p values. In the simulation, L_p is kept at 2 μm. The results indicate that charge collection at P1 and P2 both decrease with D_p value rising. This is easy to understand because the recombination rate of non-equilibrium carriers has a positive correlation with doping level. The value of L_p has a similar influence to D_p, as is shown in Fig. 14. With the increase of L_p, collector charge collections decrease monotonously. A higher L_p value simply leads to a thicker buffer layer, so the region with high recombination is expand and the electrons entered this region will be further eliminated.

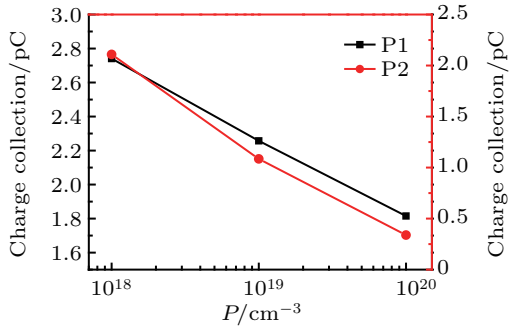


Fig. 13. Plot of collector charge collection as a function of D_p.

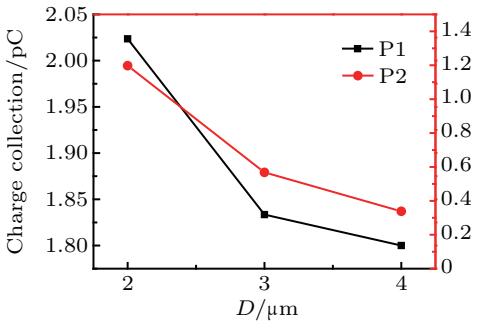


Fig. 14. Plot of collector charge collection *versus* L_p at $x = 0$ and 12.

5. Comparison between two techniques

Figure 15 shows a comparison between the mitigation results obtained by using the two techniques. For the back junction structure, $L_s = 6$ μm, $L_n = 5$ μm, and $N = 8$. For the buffer layer structure, $D_p = 1 \times 10^{20}$ cm^{-3} and $L_p = 2$ μm. The results from the two techniques have something in common. In the conventional device, the area enclosed by the p$^+$ ring wall is found to be sensitive to SET, while for the devices using the mitigation techniques, the charge collection outside the C–S junction is significantly reduced and the sensitive area is confined by the boundary of C–S junction. In addition, the charge collection of events inside the C–S junction is also reduced to a large extent. For the given parameters, the device with back junction structure shows better mitigation results than that with buffer layer structure. However, to obtain good mitigation results, the back junction structure significantly reduces the substrate thickness so that the maximum working voltage should be lower than that in the conventional and buffer layer structure to avoid punch through. In addition, the formation of the n$^+$ plugs and the metal contacts to them need additional masks. The added contacts to n$^+$ plugs will also make the metallization in highly integrated digital circuits more complicated. While for the buffer layer structure, no alteration in the device geometry is required. Only the formation of the buffer layer needs additional masks.

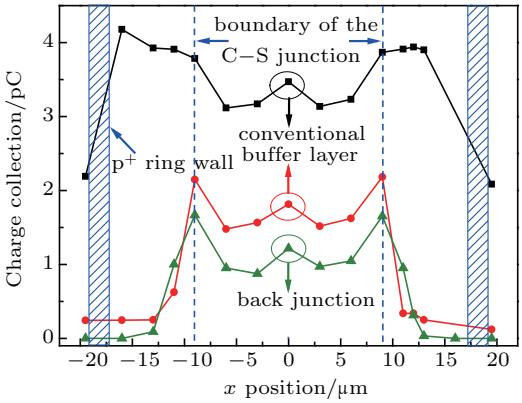


Fig. 15. Plots of collector charge collection as a function of ion strike position for SiGe HBT with different structures.

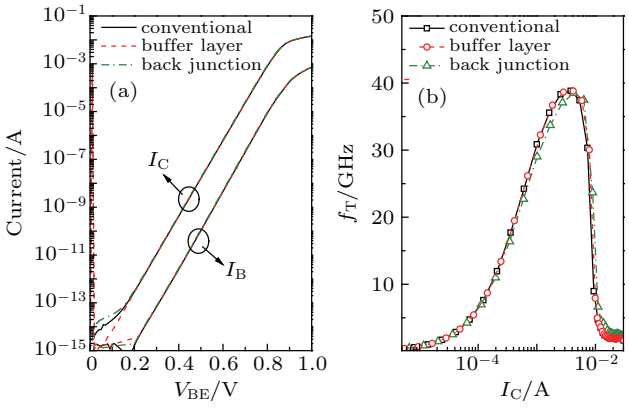


Fig. 16. Influence of mitigation techniques on (a) Gummel characteristics and (b) f_T.

Finally, neither of the two techniques with the parameters given above affect the AC and DC characteristics of the device, as evidenced by the Gummel characteristic and cutoff frequency (f_T) behavior shown in Fig. 16.

6. Summary

In this work, we investigate two mitigation techniques for reducing collector charge collection in non-DTI bulk SiGe HBT by using back junction and p^+ buffer layer. After properly adjusting the structure parameters, the two techniques can significantly reduce the charge collection induced by events inside and outside the C–S junction without affecting the DC or AC characteristics. In addition, they more effectively reduce the charge collections of events outside the C–S junction, thus leading to a significant decrease of the sensitive area to SEE. For the back junction structure, reducing the substrate while increasing thickness and doping level of the n^+ layer as well as n^+ plug number will help to obtain better mitigation results. For the buffer layer structure, the improvement of effectiveness is based on higher peak concentration and higher depth of the layer.

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