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Dark count rate and band to band tunneling optimization for single photon avalanche diode topologies

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This paper proposes two optimal designs of single photon avalanche diodes (SPADs) minimizing dark count rate (DCR). The first structure is introduced as p^+/pwell/nwell, in which a specific shallow pwell layer is added between p^+ and nwell layers to decrease the electric field below a certain threshold. The simulation results show on average 19.7% and 8.5% reduction of p^+/nwell structure's DCR comparing with similar previous structures in different operational excess bias and temperatures respectively. Moreover, a new structure is introduced as n^+/nwell/pwell, in which a specific shallow nwell layer is added between n^+ and pwell layers to lower the electric field below a certain threshold. The simulation results show on average 29.2% and 5.5% decrement of p^+/nwell structure's DCR comparing with similar previous structures in different operational excess bias and temperatures respectively. It is shown that in higher excess biases (about 6 volts), the n^+/nwell/pwell structure is proper to be integrated as digital silicon photomultiplier (dSiPM) due to low DCR. On the other hand, the p^+/pwell/nwell structure is appropriate to be utilized in dSiPM in high temperatures (above 50 °C) due to lower DCR value.

Keywords: single-photon avalanche diode, digital silicon photomultiplier, dark count rate

PACS: 85.30.De, 85.60.Dw, 85.60.Gz, 42.79.Pw **DOI:** 10.1088/1674-1056/28/6/068502

1. Introduction

Digital silicon photomultipliers (dSiPMs) are new elements for detecting low-level light with unique features such as high photon-detection efficiency, single photon timing resolution, low operating voltage, magnetic field insensitivity, high uniformity, compact form factor, low gain drift, high degree of scalability, and high ruggedness.[1,2] Moreover, dSiPMs have numerous applications in different fields of science such as positron emission tomography (PET) and single photon emission computed tomography (SPECT).[2,3]

The light sensitive area in dSiPMs is divided into an array of single photon avalanche diodes (SPADs). An SPAD pixel consists of multiple components like p–n junction, guard rings and quenching, sensing and recharging circuits.[4] Each SPAD functions like a digital sensor which detects single photon absorption. In fact, an SPAD itself is a p–n junction biased above breakdown voltage operating in the Geiger mode.[2] In addition, every SPAD has a depletion region and a multiplication region inside. A multiplication region is an area inside depletion region where avalanche multiplication occurs. Once a photon enters silicon, it can be absorbed in the depletion region and produces an electron-hole pair. Then, the electric field in this region separates electron and hole and accelerates them in opposite directions.[5] One of the positive concepts of the dSiPM's operation is that detecting the avalanche in SPADs is based on the sensing voltage changes. Thus, this makes the sensor response faster and less sensitive to the gains of the individual SPADs.[2]

Despite these distinct features, dSiPMs suffer from high dark count rate (DCR). In the absence of light, because of the thermal excitation, minority carriers are generated to induce avalanche events recognized as dark counts.[5] DCR in these detectors almost consists of band to band tunneling (BTBT), Shockley Read Hall (SRH), and trap assistant tunneling (TAT). These detectors have high DCR in comparison with other detectors like photomultiplier tubes (PMTs) in higher excess biases and temperatures.[6] Due to the dSiPM's total DCR equation which is the summation of pixel DCRs, these detectors have high amount of DCR especially in large array SPADs. Some characteristics of dSiPMs like signal-to-noise ratio (SNR) and dynamic range (DR) are inversely dependent on DCR value. Hence, more DCR also causes less DR and SNR.[7] Different methods are proposed to reduce DCR such as pixel masking and temperature reduction.[8,9] However, in the present work, new SPAD structures are proposed for dSiPMs to decrease DCR.

The novelty of this work is adding one extra layer to previous structures to reduce the electric field in order to reduce DCR. Hence, the pwell layer is added to the p^+/nwell structure and nwell layer is added to the n^+/pwell structure. By adding these layers, the electric field is under control and DCR will be reduced. Some dSiPMs which include p^+/nwell structure for SPADs have high BTBT and DCR. Therefore, using these modified structures as SPADs will decrease DCR.

The rest of this paper is organized as follows The theoretical methods which are needed to describe SPADs operations are introduced in Section 2. In Section 3, new structures

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are proposed with simulation results. Finally, the analysis is given in analysis and discussion section to demonstrate the efficiency of the proposed structures in higher excess biases and temperatures.

2. DCR calculation

DCR can be calculated using[5]

$$\mathrm{DCR} = S \cdot \int_{W_1}^{W_1+W_2} P_{\mathrm{pair}}(x) \cdot G_{\mathrm{TOT}}(x)\,\mathrm{d}x, \tag{1}$$

where S is SPAD active area, $P_{\mathrm{pair}}(x)$ is the total probability that an electron or hole produces an avalanche event at position x and $G_{\mathrm{TOT}}(x)$ is the total carriers generation rate at position x. $P_{\mathrm{pair}}(x)$ and $G_{\mathrm{TOT}}(x)$ are defined as[5]

$$P_{\mathrm{pair}}(x) = P_{\mathrm{Electron}}(x) + P_{\mathrm{Hole}}(x) - P_{\mathrm{Electron}}(x) \cdot P_{\mathrm{Hole}}(x), \tag{2}$$

$$G_{\mathrm{TOT}}(x) = G_{\mathrm{SRH+TAT}}(x) + G_{\mathrm{BTBT}}(x), \tag{3}$$

where $P_{\mathrm{Electron}}(x)$ is electron avalanche triggering probability and $P_{\mathrm{Hole}}(x)$ is hole avalanche triggering probability. In this work, avalanche probabilities are obtained accurately from a commercially available device simulator.[10] $G_{\mathrm{SRH+TAT}}(x)$ and $G_{\mathrm{BTBT}}(x)$ are generation rates of SRH/TAT and BTBT. The BTBT generation rate of carriers is calculated using Schenk's model. This model is one of the meticulous methods for calculating BTBT expressed by[10,11]

$$G_{\mathrm{BTBT}} = A.BBT.SCHENK \cdot F^{7/2} \cdot S \cdot \left(\frac{(A^{\mp})^{-3/2} \cdot \mathrm{e}^{(A^{\mp}/F)}}{\exp[(HW.BBT.SCHENK)/kT] - 1} + \frac{(A^{\pm})^{-3/2} \cdot \mathrm{e}^{(A^{\pm}/F)}}{1 - \exp[(-HW.BBT.SCHENK)/kT]} \right), \tag{4}$$

where S is the statistical factor dependent on carrier concentrations and A^+ can be obtained as[10]

$$A^+ = B.BBT.SCHENK(\hbar w \pm HW.BBT.SCHENK)^{3/2}, \tag{5}$$

where $\hbar w$ is the energy of the transverse acoustic phonon. The upper sign refers to the tunneling generation of electron–hole pairs (reverse biased junction).[10] In addition, the SRH/TAT generation rate of carriers in the depletion region is given by[5,12,13]

$$G_{\mathrm{SRH,TAT}} = \frac{n_{\mathrm{i}}(1+\Gamma)}{\tau_{\mathrm{n}} \cdot \exp\{[-(E_{\mathrm{T}} - E_{\mathrm{i}})/kT]\} + \tau_{\mathrm{p}} \cdot \exp\{[(E_{\mathrm{T}} - E_{\mathrm{i}})/kT]\}}, \tag{6}$$

where Γ is the field effect function of the TAT model and is given by[5]

$$\Gamma = 2\sqrt{3\pi} \cdot \frac{|F|}{F_\Gamma} \cdot \mathrm{e}^{((|F|/F_\Gamma)^2)}, \tag{7}$$

where F is the local electric field strength and F_Γ equals[5]

$$F_\Gamma = \frac{\sqrt{24 \cdot m_{\mathrm{t}}^* \cdot (kT)^3}}{q\hbar}, \tag{8}$$

where $\hbar$ is the reduced Planck's constant, q is the electron charge and m_{t}^* is the electron effective tunneling mass. The DCR, BTBT, and SRH/TAT of the two proposed topologies of this paper will be calculated and shown in Section 3.

3. Design and description

3.1. p$^+$/pwell/nwell structure

In the proposed structure, which is based on Ref. [5] and has been modified in this paper, the p$^+$/pwell/nwell junction is surrounded by pwell and shallow trench isolation (STI) guard rings, which prevents premature breakdown at p–n junction edges. The deep nwell layer isolates the SPAD from other devices.[5] A wide depletion junction which comprises pwell/nwell is used to lower BTBT and DCR.[14,15]

A thin p$^+$ layer is implanted on the device surface to form Ohmic contact and to prevent enhancing DCR of the device.[16] On the other hand, this layer contributes to high DCR since it increases electric field at depletion region edges. In order to have p$^+$ presence advantages and lower electric field, a pwell layer is implanted under p$^+$ layer. It should be mentioned that the depth of new pwell layer is less than pwell guard rings and its doping is considered higher than pwell guard rings. This could be performed with halo implants. Halo doping is used for increasing the doping in specific areas.[17,18] By using this approach, the doping of this layer is enhanced to meet specific value of electric field in order to have avalanche event. Implanting new pwell layer in this structure leads device to have lower DCR due to the lower electric field. However, using p$^+$/pwell/nwell structure instead of p$^+$/nwell structure affects SRH minimally due to TAT model. In addition, by using a thinner layer of p$^+$, timing response will be improved.[19] Figure 1 shows the cross section of this structure. The photon detection efficiency (PDE) in this device is more than that of n$^+$/nwell/pwell structure due to high avalanche probabilities. Figure 2 shows the electric field in the mentioned structure at 4-V excess bias and the multiplication region is displayed in red color.

The nwell layer's doping also affects the electric field and DCR. Higher concentration of nwell doping can be translated as higher DCR,[20] though nwell doping decrement has a limitation. Indeed, this region's doping could be lowered until

a certain threshold. The limitation exists because the electric field attenuates and the avalanche event does not occur when nwell doping decreases below a certain threshold. Eventually, it should be noted that the PDE of this device is about 12.8% and less than p^+/nwell structure's PDE (17.5%) in 300 nm wavelength and 3.5 V excess bias due to lower avalanche probabilities.

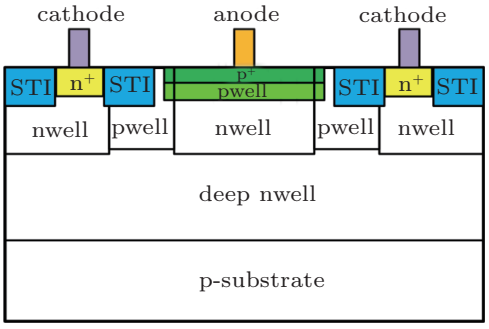


Fig. 1. p^+/pwell/nwell structure.

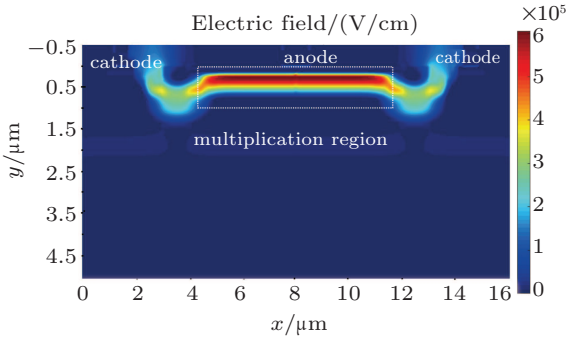


Fig. 2. Two-dimensional (2D) electric field profile of p^+/pwell/nwell structure.

3.2. n^+/nwell/pwell structure

In this structure, which is based on Ref. [21] and has been modified, the n^+/nwell/pwell junction is surrounded by nwell and STI guard rings, which prevent premature breakdown to occur at p-n junction edges. The deep pwell layer isolates the SPAD from other devices. A wide depletion junction which comprises nwell/pwell is used to have a lower BTBT and DCR.[14]

A thin n^+ layer is implanted on the device surface to create ohmic contact with the metal and to impede DCR of the device from enhancement.[16] On the other hand, this layer contributes to high DCR since it increases electric field at the edge of the depletion region. To have the advantages of n^+ presence and lower electric field, a nwell layer is implanted under the n^+ layer. Again, same as previously proposed structure, it should be mentioned that the depth of this layer is less than pwell guard rings and its doping is considered higher than pwell guard rings with the usage of halo implant.[18] Hence, the doping of additional nwell layer is enhanced to meet specific value of electric field in order to have avalanche event.

In conclusion, the device has lower DCR due to lower electric field. However, using n^+/nwell/pwell structure instead of p^+/nwell structure affects SRH minimally due to TAT model. In addition, by using a thinner layer of n^+, timing response will be improved.[19] Another concept that occurs in the proposed structure is that the holes are minority carriers. Thereby, the avalanche probabilities are less than the situation where electrons initiate avalanche. Therefore, this device has low PDE. Namely, nwell and pwell layers play a key role in decreasing DCR by electric field reduction.

The pwell layer's doping also affects the electric field and DCR. Higher pwell doping can be translated as higher DCR.[20] Decreasing pwell doping has a limitation. Indeed, this region's doping could be lowered until a certain threshold. The limitation exists because the electric field attenuates and the avalanche event does not occur when pwell doping is lowered below the certain threshold. Figure 3 shows the cross section of the proposed structure. Finally, it should be mentioned that the PDE of this device is about 10.7% and less than p^+/nwell structure's PDE (17.5%) in 300-nm wavelength and 3.5-V excess bias due to lower avalanche probabilities.

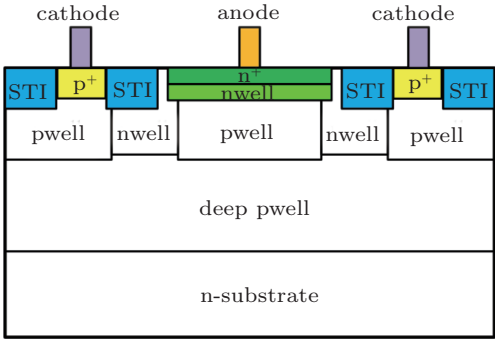


Fig. 3. n^+/nwell/pwell structure.

4. Simulation results

To compare the results of this paper with the previous data, the p^+/nwell structure is considered as a reference.[5,16] The p^+/nwell structure's DCR, BTBT, and SRH/TAT are verified to have certain criteria for comparing results of the simulations. Figures 4 and 5 show this structure and the verified results. In all three structures, DCR is calculated using Eq. (1), BTBT is calculated using Eq. (4), and SRH is calculated using Eq. (6).

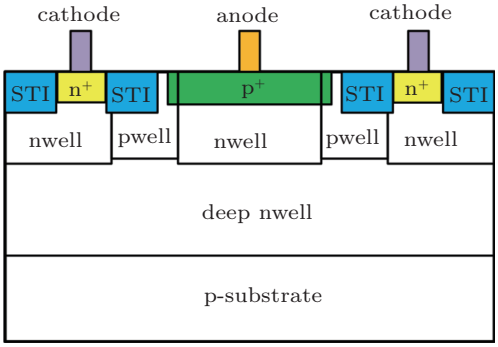


Fig. 4. p^+/nwell structure.

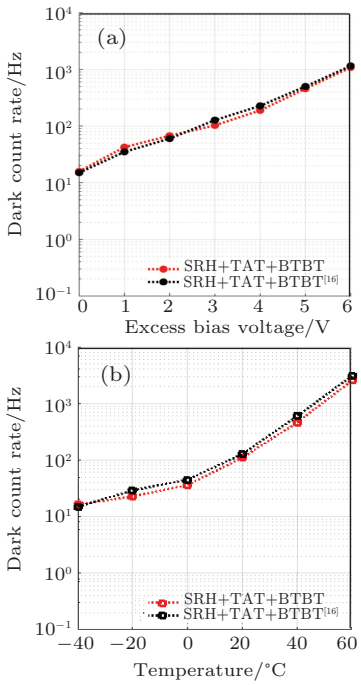


Fig. 5. Verified results. DCR values in: (a) excess bias voltage and (b) temperature variations.

Table 1 shows the main parameters of the proposed structures. SRH model of technology computer aided design (TCAD) tool is used for SRH simulations.[10] The parameters in Section 2 (breakdown voltage, cross section area of depletion region, electron lifetime, hole lifetime, trap energy level, electron tunneling effective mass, rest electron mass, and BTBT parameters) have identical values in both verification and new structures simulations. In the following, the simulation results are reported. In order to validate the accuracy of the results, the simulation outputs are compared with the tested data reported in previous works.

Table 1. The important characteristics of both n^+/nwell/pwell and p^+/pwell/nwell structures.

Parameter	Description	Value	Unity
V_{Break}	breakdown voltage	16	V
S	cross section area of depletion region	78.5	m^2
Node	technology node	150	nm

Table 2 shows the simulation parameters and their values.

Table 2. Simulation parameters.

Parameter	Description	Value	Unity	Ref.
τ_n	electron lifetime	500	ns	[22]
τ_p	hole lifetime	950	ns	[22]
$E_t - E_i$	trap energy level	0.2	eV	[23]
L_e	electron diffusion length	80	nm	[5]
L_h	hole diffusion length	400	nm	[5]
A.BBT.SCHENK	BTBT parameter	1.8×10^{20}	$cm^2 \cdot s^{-1} \cdot V^{-2}$	[11]
B.BBT.SCHENK	BTBT parameter	2.14667×10^7	$eV^{-3/2} \cdot V \cdot cm^{-1}$	[11]
HW.BBT.SCHENK	BTBT parameter	0.0186	eV	[11]

4.1. p^+/pwell/nwell structure analysis

In this section, the p^+/pwell/nwell structure is simulated in excess bias variation from 0 V to 6 V. In addition, simulations are performed in temperature variation from −40 °C to 60 °C.

4.1.1. Excess bias variation

In Fig. 6(a) the DCR and BTBT analogies between p^+/pwell/nwell and p^+/nwell[5,16] structures in excess bias variation are shown. It can be seen that the proposed optimal design decreases BTBT value. Despite lower excess biases, this structure has lower DCR in higher excess biases.

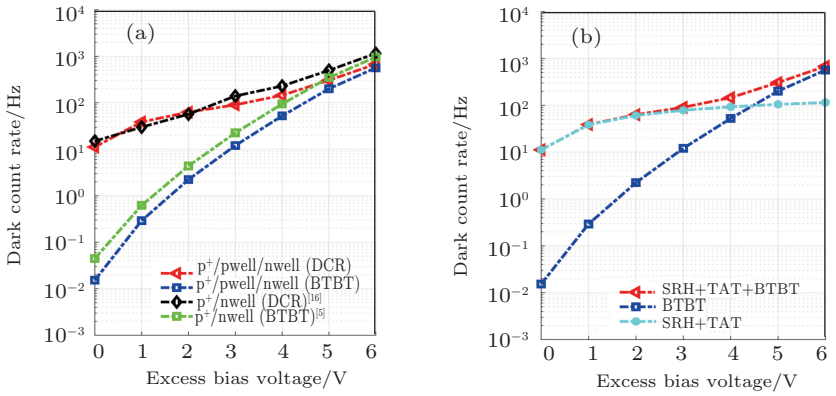


Fig. 6. (a) BTBT, SRH/TAT, and DCR of p^+/pwell/nwell structure at room temperature. (b) Comparison between p^+/pwell/nwell and p^+/nwell[5,16] structures.

Figure 6(b) displays SRH/TAT, BTBT, and DCR of the proposed structure. In lower excess biases, especially below 2-V excess bias, the SRH is dominant in DCR. On the contrary, in higher excess biases, the BTBT becomes the main component of DCR. The simulations are performed at room temperature.

4.1.2. Temperature variation

Figure 7(a) shows the DCR and SRH comparisons between p^+/pwell/nwell and p^+/nwell[5,16] structures. It is clear that the proposed optimal design decreases SRH and DCR values. However, the BTBT changes are negligible. Figure 7(b) exhibits SRH/TAT, BTBT, and DCR of the proposed structure. In lower temperatures, especially below 0 °C, the BTBT is more dominant in DCR. In contrast, in higher temperatures, the SRH becomes the main component of the DCR. This stage simulations are performed at 3.5-V excess bias.

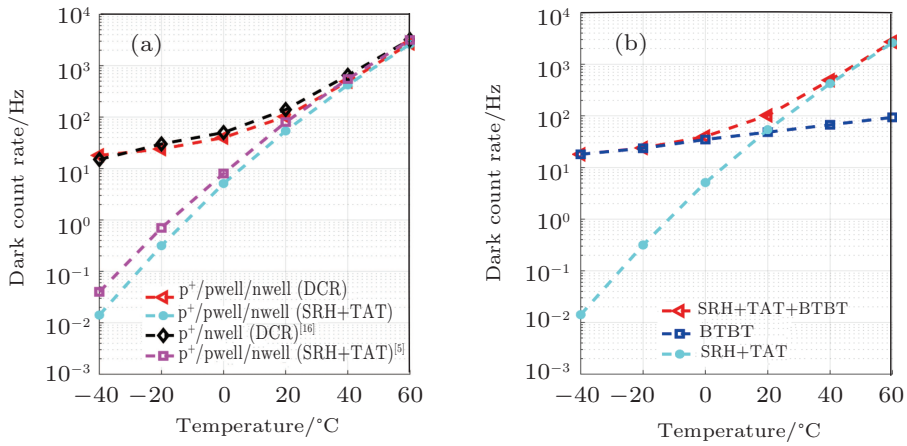


Fig. 7. (a) Comparison between p^+/pwell/nwell structure and p^+/nwell[5,16] at 3.5-V excess bias. (b) BTBT, SRH/TAT, and DCR of p^+/pwell/nwell structure. At 3.5-V excess bias.

4.2. n^+/nwell/pwell structure analysis

In this section, the n^+/nwell/pwell structure is simulated in excess bias variation from 0 V to 6 V. In addition the structure is simulated in temperature variation from −40 °C to 60 °C.

4.2.1. Excess bias variation

Figure 8(a) shows the DCR and BTBT comparisons between n^+/nwell/pwell and p^+/nwell[5,16] structures in excess bias variation. There is no doubt that the proposed optimal design decreases BTBT value. Although in lower excess biases the results are analogous to the tested data in Refs. [5] and [16], n^+/nwell/pwell structure lowers the DCR in higher excess biases obviously. Figure 8(b) shows SRH/TAT, BTBT, and DCR of this structure. In lower excess biases, SRH is more prevailing in DCR. However, in higher excess biases, BTBT becomes the main component of DCR and simulations are performed at room temperature.

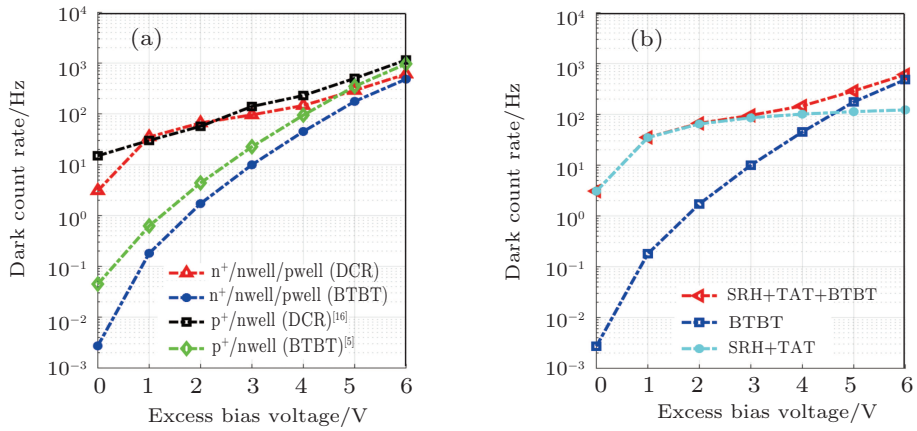


Fig. 8. (a) Comparison between n^+/nwell/pwell and p^+/nwell[5,16] structures. (b) BTBT, SRH/TAT, and DCR of n^+/nwell/pwell structure. At room temperature.

4.2.2. Temperature variation

The comparisons of DCR and SRH between n^+/nwell/pwell and p^+/nwell[5,16] structures in temperature variation are shown in Fig. 9(a). From these curves, it is clear that the proposed optimal design decreases SRH and DCR values. However, the BTBT alterations are negligible. Figure 9(b) exhibits SRH/TAT, BTBT, and DCR of this structure. In lower temperatures, the BTBT is more dominant in DCR while in higher temperatures, the SRH becomes the main component of the DCR, and simulations are performed at 3.5-V excess bias.

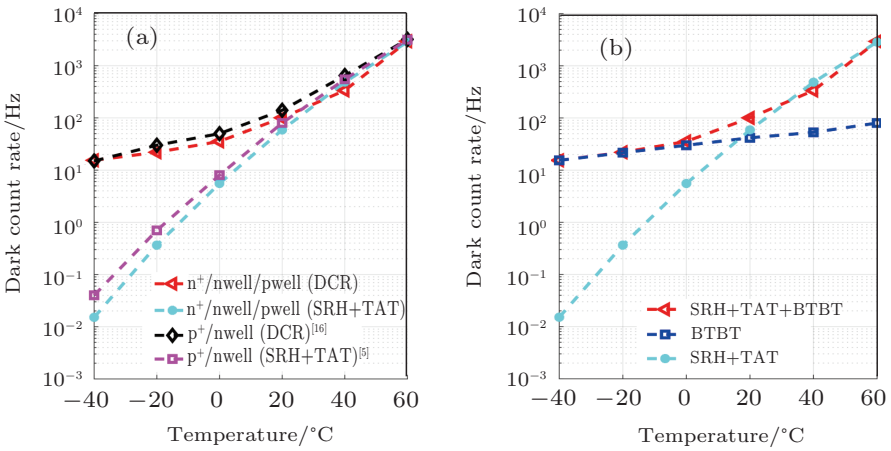


Fig. 9. (a) Comparison between n^+/nwell/pwell and p^+/nwell[5,16] structures. (b) BTBT, SRH/TAT, and DCR of n^+/nwell/pwell structure. At 3.5-V excess bias.

5. Results and discussion

5.1. p^+/pwell/nwell structure

The results and figures indicate that DCR and BTBT are less than those in Refs. [5] and [16] in excess bias variation and more than those of n^+/nwell/pwell structure. In addition, DCR and SRH of this structure are less than those in Refs. [5] and [16] and n^+/nwell/pwell structure in temperature variation. However, to quantitatively evaluate the improvement (DCR reduction), the difference between the DCR of p^+/nwell structure and the DCR of p^+/pwell/nwell structure is averaged in different biases or different temperatures, and the mean difference is calculated for DCR, BTBT, and SRH quantities.

In excess bias variation (between 0 V to 6 V), mean difference value between BTBTs is 49%. In other words, this proposed structure reduces BTBT of p^+/nwell[5,16] by 49%. In addition, this structure diminishes DCR of p^+/nwell[5,16] leastwise 19.7%. In temperature variation (between −40 °C to 60 °C), the mean difference value between SRHs is 15.2% and this structure diminishes DCR of p^+/nwell[5,16] by 8.5%.

5.2. n^+/nwell/pwell structure

In this section, similar to the previous section, mean difference values are evaluated. In excess bias variation (between 0 V to 6 V), the mean difference value between BTBTs is 61.9%. Moreover, the n^+/nwell/pwell structure diminishes DCR of p^+/nwell[5,16] by 29.2%. Eventually, in temperature variation (between −40 °C to 60 °C), mean difference value between SRHs is 12.1% and this structure lessens DCR of p^+/nwell[5,16] by 5.5%.

The DCR improvements become more tangible for using in a dSiPM including an array of several SPADs. Thus, using p^+/pwell/nwell and n^+/nwell/pwell structures for SPAD in dSiPM could diminish the total DCR of dSiPM. Figure 10 shows the comparison between BTBTs, SRHs, and DCRs of three structures of a dSiPM which consists of a 16 × 16 array of SPADs at 6-V excess bias and 60 °C.

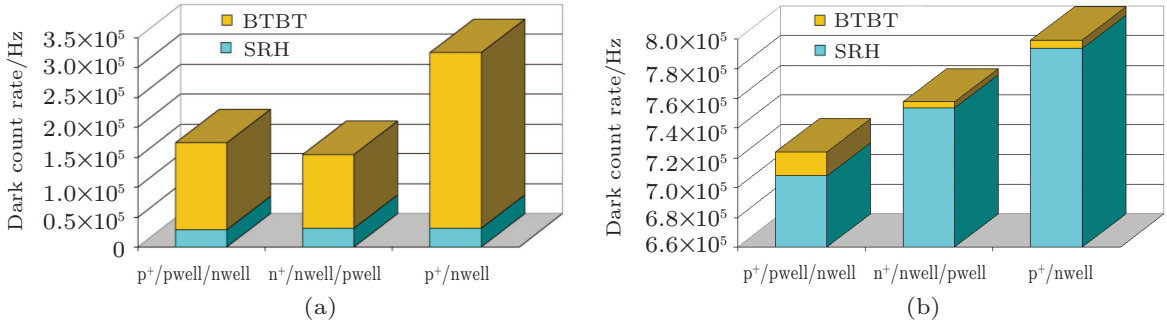


Fig. 10. DCR comparison between three structures of a high voltage dSiPM. (a) DCR at 6-V excess bias (room temperature). (b) DCR at 60 °C (3.5-V excess bias).

Due to obtained results and Fig. 8, it is suggested that for higher excess biases applications, the n^+/nwell/pwell structure is recommended to be used in dSiPM since it has less DCR in comparison with two other structures. Nevertheless, in higher temperatures, the p^+/pwell/nwell structure is recommended to be utilized in dSiPM,since it has DCR in comparison with the other two.

6. Conclusions

In this paper, two optimal designs of SPAD for dSiPM with the same pixel pitch of 16 μm are proposed for DCR reduction. This paper reports that DCR in both p^+/pwell/nwell and n^+/nwell/pwell structures is less than that of p^+/nwell structure. In p^+/pwell/nwell structure, DCR has been decreased by an average of 19.7% in different operational excess biases and 8.5% in different operational temperatures. In n^+/nwell/pwell structure, DCR has been reduced by an average of 29.2% in different operational excess biases and 5.5% in different operational temperatures. It is expected that dSiPMs consisting of p^+/pwell/nwell-structure SPADs or n^+/nwell/pwell-structure SPADs will have less DCR in comparison with dSiPMs comprising p^+/nwell-structure SPADs. In higher excess biases, the n^+/nwell/pwell structure is recommended to be used in a dSiPM detector due to its lower DCR. On the other hand, in higher temperatures, the p^+/pwell/nwell structure is recommended to be used in a dSiPM due to low DCR.

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