ISSN 1674-1056
http://cpb.iphy.ac.cn
http://iopscience.iop.org/cpb
中国物理 B
Chinese Physics
中国物理 Chinese Physics B

Stacked lateral double-diffused metal-oxide-semiconductor field effect transistor with enhanced depletion effect by surface substrate

Qi Li(李琦), Zhao-Yang Zhang(张昭阳), Hai-Ou Li(李海鸥), Tang-You Sun(孙堂友), Yong-He Chen(陈永和), Yuan Zuo(左园)

Citation: Chin. Phys. B . 2019, 28(3): 037201. **doi:** 10.1088/1674-1056/28/3/037201
Journal homepage: http://cpb.iphy.ac.cn; http://iopscience.iop.org/cpb

What follows is a list of articles you may be interested in

Numerical and experimental study of the mesa configuration in high-voltage 4H-SiC PiN rectifiers

Xiao-Chuan Deng(邓小川), Xi-Xi Chen(陈茜茜), Cheng-Zhan Li(李诚瞻), Hua-Jun Shen(申华军), Jin-Ping Zhang(张金平)
Chin. Phys. B . 2016, 25(8): 087201. **doi:** 10.1088/1674-1056/25/8/087201

Improving breakdown voltage performance of SOI power device with folded drift region

Qi Li(李琦), Hai-Ou Li(李海鸥), Ping-Jiang Huang(黄平奖), Gong-Li Xiao(肖功利), Nian-Jiong Yang(杨年炯)
Chin. Phys. B . 2016, 25(7): 077201. **doi:** 10.1088/1674-1056/25/7/077201

New SOI power device with multi-region high-concentration fixed interface charge and the model of breakdown voltage

Li Qi, Li Hai-Ou, Tang Ning, Zhai Jiang-Hui, Song Shu-Xiang
Chin. Phys. B . 2015, 24(3): 037203. **doi:** 10.1088/1674-1056/24/3/037203

New 4H silicon carbide metal semiconductor field-effect transistor with a buffer layer between the gate and the channel layer

Zhang Xian-Jun, Yang Yin-Tang, Duan Bao-Xing, Chen Bin, Chai Chang-Chun, Song Kun
Chin. Phys. B . 2012, 21(1): 017201. **doi:** 10.1088/1674-1056/21/1/017201

Effects of gate-buffer combined with a p-type spacer structure on silicon carbide metal–semiconductor field-effect transistors

Song Kun, Chai Chang-Chun, Yang Yin-Tang, Chen Bin, Zhang Xian-Jun, Ma Zhen-Yang
Chin. Phys. B . 2012, 21(1): 017202. **doi:** 10.1088/1674-1056/21/1/17202

Stacked lateral double-diffused metal–oxide–semiconductor field effect transistor with enhanced depletion effect by surface substrate*

Qi Li(李琦), Zhao-Yang Zhang(张昭阳), Hai-Ou Li(李海鸥),
Tang-You Sun(孙堂友), Yong-He Chen(陈永和), and Yuan Zuo(左园)†

Guangxi Key Laboratory of Precision Navigation Technology and Application, Guilin University of Electronic Technology, Guilin 541004, *China*

(Received 11 September 2018; revised manuscript received 18 December 2018; published online 23 January 2019)

A stacked lateral double-diffused metal–oxide–semiconductor field-effect transistor (LDMOS) with enhanced depletion effect by surface substrate is proposed (ST-LDMOS), which is compatible with the traditional CMOS processes. The new stacked structure is characterized by double substrates and surface dielectric trenches (SDT). The drift region is separated by the P-buried layer to form two vertically parallel devices. The doping concentration of the drift region is increased benefiting from the enhanced auxiliary depletion effect of the double substrates, leading to a lower specific on-resistance ($R_{on,sp}$). Multiple electric field peaks appear at the corners of the SDT, which improves the lateral electric field distribution and the breakdown voltage (BV). Compared to a conventional LDMOS (C-LDMOS), the BV in the ST-LDMOS increases from 259 V to 459 V, an improvement of 77.22%. The $R_{on,sp}$ decreases from 39.62 mΩ·cm^2 to 23.24 mΩ·cm^2 and the Baliga's figure of merit (FOM) of is 9.07 MW/cm^2.

Keywords: double substrates, surface dielectric trench, stacked lateral double-diffused metal–oxide–semiconductor field-effect transistor (ST-LDMOS), breakdown voltage

PACS: 72.80.Cw, 73.40.Qv **DOI:** 10.1088/1674-1056/28/3/037201

1. Introduction

Silicon-on-insulator (SOI) is a widely used technique for power integrated circuits (PIC) because of its effective isolation, low leakage current, and high breakdown voltage (BV).[1–3] Lateral double-diffused metal–oxide–semiconductor field-effect transistor (LDMOS) is a key device for the PIC, but it is not area efficient and suffers the contradiction between the BV and specific on-resistance $R_{on,sp}$. The BV of the power device is limited by the low lateral BV for the poor surface electric field distribution, and some work has been carried out, such as the variable lateral doping (VLD),[4–7] super junction,[8,9] and charge islands.[10] Enhancing the electric field (ENDIF) of the dielectric buried layer is a feasible method to increase the vertical BV and several new structures have been developed[11–15] in which introducing self-adaptive interface charges are effective and attractive.

In this paper, a stacked LDMOS with enhanced depletion effect by surface substrate is proposed. The additional surface substrate is formed of polysilicon, and the doping concentration in the drift region is increased based on the enhanced auxiliary depletion effect of the dual substrates, thus a lower $R_{on,sp}$ is obtained. The multiple electric field peaks located in the surface dielectric trenches (SDT) modulate the bulk electric field distribution and improve the BV. The influences of the structure parameters on the BV and $R_{on,sp}$ are analyzed.

2. Mechanism and device structure

Figure 1(a) shows the schematic cross-sectional view of the ST-LDMOS. The drift region is separated by the P buried layer to form two vertically parallel devices, and polysilicon and p-type silicon form the upper substrate and the lower substrate, respectively. The surface substrate enhances drift region depletion. Meanwhile it also enhances the compensation effect of the drift region, leading to the decrease of $R_{on,sp}$. Furthermore, many electric field peaks appear at the edge of the SDT, which prevents premature surface breakdown and increases the lateral BV. SDT parameter optimization is easy and the manufacturing process is simple.

Figure 1(b) gives the charge composition in the double dielectric trenches. According to the electric neutralization principle, the charge composition is expressed as

$$\sigma_{h1} + N_{d1} + \sigma_{h2} + N_{d2} = N_{pb} + N_{p1} + \sigma_{e1} + N_{p2} + \sigma_{e2}, \quad (1)$$

where N_{p1} and N_{p2} are the acceptor concentrations in the top and bottom substrates, respectively; N_{d1} and N_{d2} represent the top ionized donor and bottom ionized donor in the drift region, respectively; σ_{e1}, σ_{e2}, σ_{h1}, and σ_{h2} represent the top electron, bottom electron, top hole, and bottom hole in the top and bottom substrates, respectively. The optimum doping concentration (N_{d1} and N_{d2}) in the drift region of the ST-LDMOS is increased due to the extra σ_{e1} and N_{p1} charge in the right side of the equation. But for the conventional LDMOS (C-LDMOS),

*Project supported by the National Natural Science Foundation of China (Grant No. 61464003) and the Guangxi Natural Science Foundation, China (Grant Nos. 2015GXNSFAA139300 and 2018JJA170010).

†Corresponding author. E-mail: juear615@outlook.com

© 2019 Chinese Physical Society and IOP Publishing Ltd

$\sigma_{e1} = 0$ and $N_{p1} = 0$. The detailed parameters of the devices are listed in Table 1.

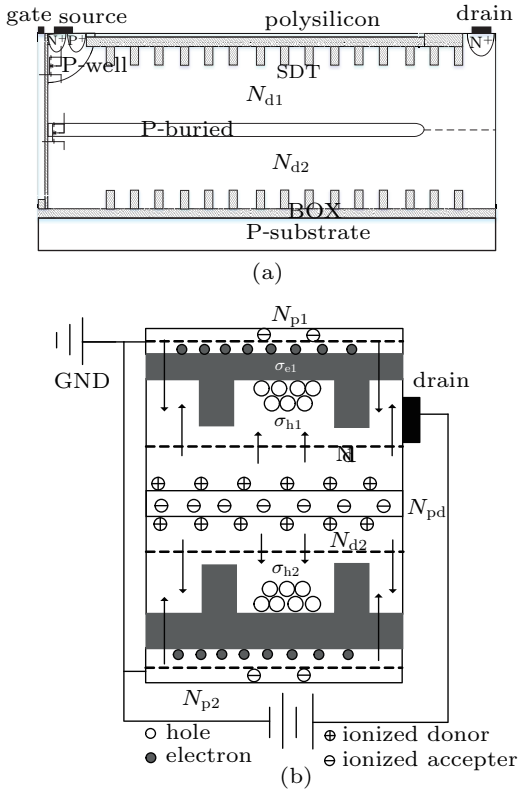


Fig. 1. (a) Schematic cross section of the proposed ST-LDMOS; (b) the charge distribution at off-state ($V_{DS} > 0$, $V_{GS} = 0$).

Table 1. Device parameters used in the simulation.

Device parameters	ST-LDMOS	C-LDMOS
Drift length L_d/μm	24	24
Thickness of BOX/μm	1	1
Length of P-buried layer L_p/μm	10–40	–
Height of oxide trench H/μm	0.25–0.75	–
Width of oxide trench W/μm	0.5	–
Spacing of oxide trench D/μm	0.5	–
Buried concentration N_p/cm^{-3}	(2–4)×10^{16}	–

3. Results and discussion

Figure 2(a) shows the equipotential contour distributions. The contours of the ST-LDMOS device present in a uniform manner, thus the BV reaches 459 V; while the optimal conventional device shows field crowding at the drain and source edges and the BV is limited to 259 V. In contrast with the C-LDMOS, the doping concentration of the ST-LDMOS is increased by an enhanced depletion effect from the surface substrate. Figure 2(b) shows the comparison of the off-state I–V characteristics between the C-LDMOS and ST-LDMOS, and the BV of the proposed device is greatly improved by 77.22%. The simulation results show that the proposed device has almost the same switching characteristics as the traditional Con device.

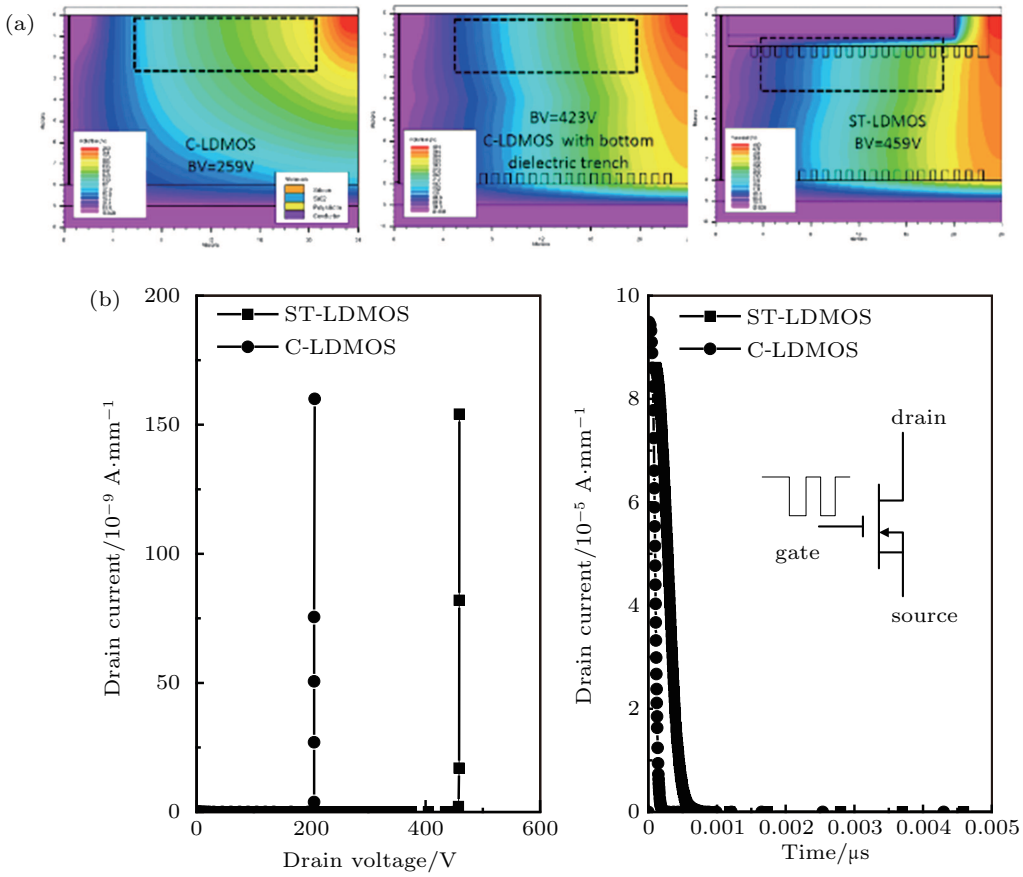


Fig. 2. (a) The equipotential contour distributions; (b) the off-state I–V and turn off time characteristics of the C-LDMOS and ST-LDMOS.

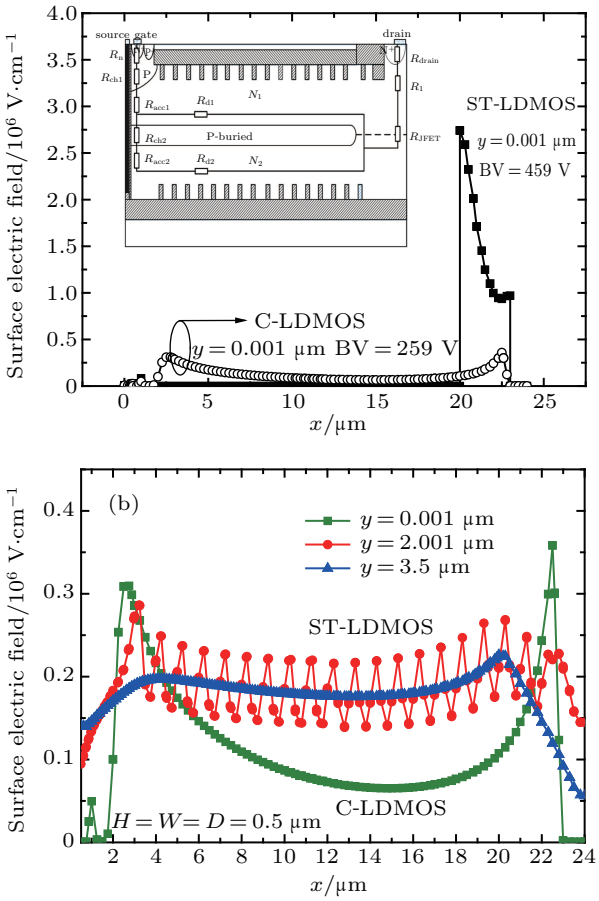


Fig. 3. Lateral electric field distribution at breakdown for two LDMOSs: (a) $y = 0.001$ μm, (b) $y = 2.001$ μm and $y = 3.5$ μm.

Figure 3 shows the lateral electric field distribution for the two LDMOSs. In Fig. 3(b), the ST-LDMOS shows a significant advantage over the optimal C-LDMOS. The lateral electric field of the ST-LDMOS is more uniform and its average is higher than that of the C-LDMOS because of the modulation effect by the multiple electric field peaks at the edge of the SDT in Fig. 3(b). According to the equivalent circuit of ST-LDMOS in Fig. 3(a), the on-resistance can be given as follows:

$$R_{\mathrm{DS(on)}} = R_{\mathrm{n}} + R_{\mathrm{ch1}} + R_{\mathrm{acc1}} + R_{\mathrm{d1}} \| (R_{\mathrm{ch2}} + R_{\mathrm{acc2}} + R_{\mathrm{d2}}) + R_{\mathrm{JFET}} + R_1 + R_{\mathrm{drain}}. \quad (2)$$

Generally,

$$R_{\mathrm{ch2}} + R_{\mathrm{acc2}} \ll R_{\mathrm{d2}}. \quad (3)$$

Based on the body resistance expression,

$$R_{\mathrm{d1}}/R_{\mathrm{d2}} = N_{\mathrm{d2}}/N_{\mathrm{d1}}. \quad (4)$$

When $N_{\mathrm{d1}} \gg N_{\mathrm{d2}}$, the optimal resistance $R_{\mathrm{on,sp}}$ is derived as

$$R_{\mathrm{on,sp}} = R_{\mathrm{n}} + R_{\mathrm{ch1}} + R_{\mathrm{acc1}} + R_{\mathrm{d1}} + R_{\mathrm{JFET}} + R_1 + R_{\mathrm{drain}}. \quad (5)$$

Figure 4(a) shows the vertical electric field and potential distributions. The electric field of the buried oxide layer (BOX), E_{I}, increases from 90 V/μm of the C-LDMOS to 400 V/μm, and BV of 796 V is obtained. More than 87.1% of BV is shared by the BOX for the ST-LDMOS, but only 55% for the C-LDMOS. In addition, the multiple electric field peaks increase the vertical electric field in SDT and modulate the electric field in the drift region, both result in the enhancement of the BV. Figure 4(b) shows the 3D electric field distribution of the ST-LDMOS, the voltage drop of SDT near the drain is the highest, and the electric field increases from the source to drain. The new electric field peak appears in the silicon layer and the lateral electric field is significantly improved.

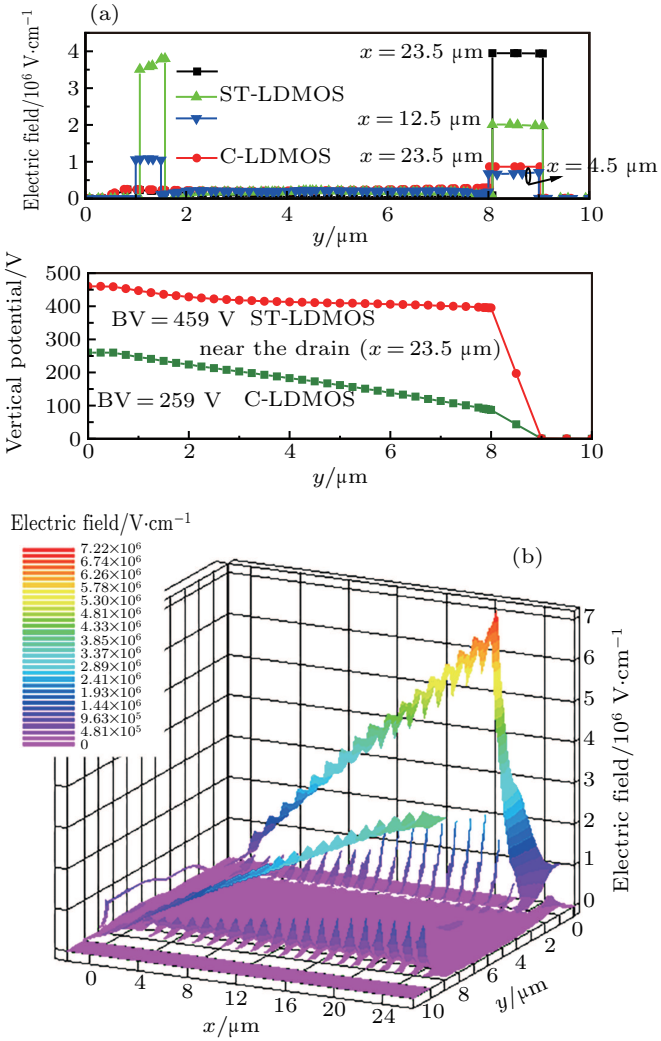


Fig. 4. (a) Vertical electric field and potential distributions, (b) 3D electric field distribution of ST-LDMOS.

Figure 5(a) gives the relationship between the doping concentration N_{d2} and BV with $H = W = D = 0.5$ μm, $L_{\mathrm{p}} = 20$ μm, and $t_{\mathrm{p}} = 1$ μm. The maximum BV increases with the increase of N_{d2}. The optimum N_{d1} decreases with the increase of N_{d2} as the sum of optimized doping concentration in the drift region is fixed. Figure 5(b) shows the relationship between the doping concentration N_{d2} and $R_{\mathrm{on,sp}}$, and the ratio of the doping concentration distribution is given by

$$N_{\mathrm{ratio}} = N_{\mathrm{d1}}/N_{\mathrm{d2}}.$$

More current flows across the top of the drift region with the increase of N_{ratio}, and when N_{ratio} is equal to 4, the minimal $R_{on,sp}$ is 21.87 mΩ·cm^2.

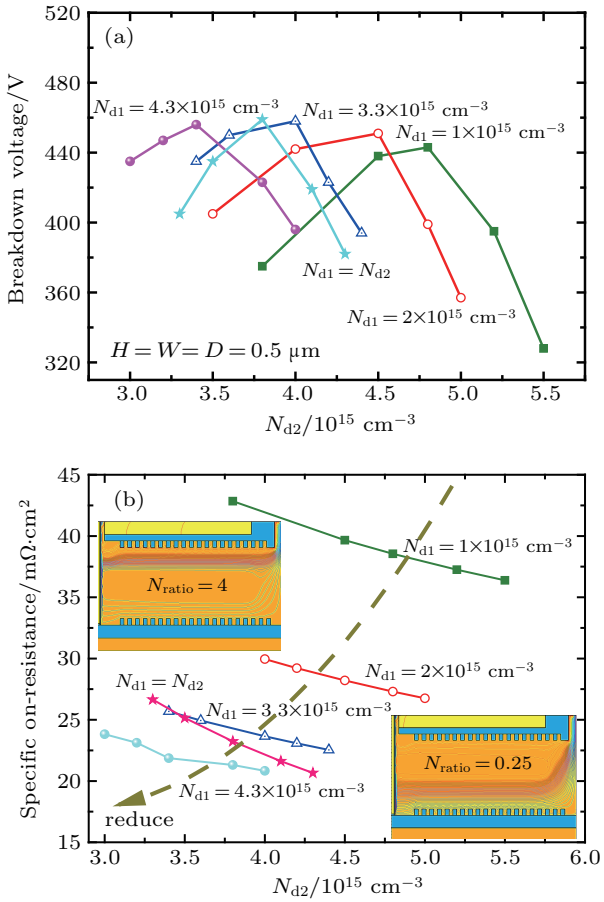


Fig. 5. Influence of the drift region doping concentration on (a) BV and (b) $R_{on,sp}$.

Figure 6(a) shows the BV versus drift region doping concentration of the ST-LDMOS with P-buried length L_p as a parameter. The maximum of the BV decreases with the decrease of L_p, because when L_p is shorter, the electric field modulation is weaker. The $R_{on,sp}$ reduces with the increase of N_d in Fig. 6(b) due to the enhancement of charge compensation effect, and the inset describes the relationship between the width (W_p) of the P-buried layer and $R_{on,sp}$. Figure 6(c) analyzes the influence of the P-buried position on the BV and $R_{on,sp}$. The optimum BV changes little within a small range of P-buried position, and the $R_{on,sp}$ decreases with increasing P-buried position. The insertion table shows the effect of the P-buried diffusion process on the voltage.

Figure 7 illustrates the influence of H on the BV and $R_{on,sp}$ with $L_p = 20$ μm. The BV increases with increasing H, but $R_{on,sp}$ is increased. The multiple electric field peaks increase with the increase of H, which is helpful to optimize the lateral electric field in the Si layer.

Figure 8(a) is a summary of $R_{on,sp}$ versus BV for currently reported LDMOS devices[16–20] and ST-LDMOS. It is noticeable that the proposed structure significantly relieves the trade-off between the BV and $R_{on,sp}$. Compared with the C-LDMOS with the same dimensions of $L_d = 22.5$ μm, the BV of the ST-LDMOS is increased by 77.22% due to the electric field modulation effect of the SDT. Furthermore, owing to the assisted-depletion effect of the double substrates, the optimal N_d and $R_{on,sp}$ are greatly improved. Figure 8(b) is a summary of BV versus L_d for currently reported LDMOS devices.[21,22] The ST-LDMOS exhibits the figure of merit (FOM) of 9.07 MW/cm^2, superior over the C-LDMOS and prior arts. There is little difference between the experimental data and the simulation data. The simulation uses the same model, so the simulation has certain reliability. The proposed structure is better than the conventional SOI LDMOS.

The process simulation of the ST-LDMOS is shown in Fig. 9 by SILVACO. The starting material is a silicon wafer and the trench is etched. The SiO_2 is deposited and planarized.

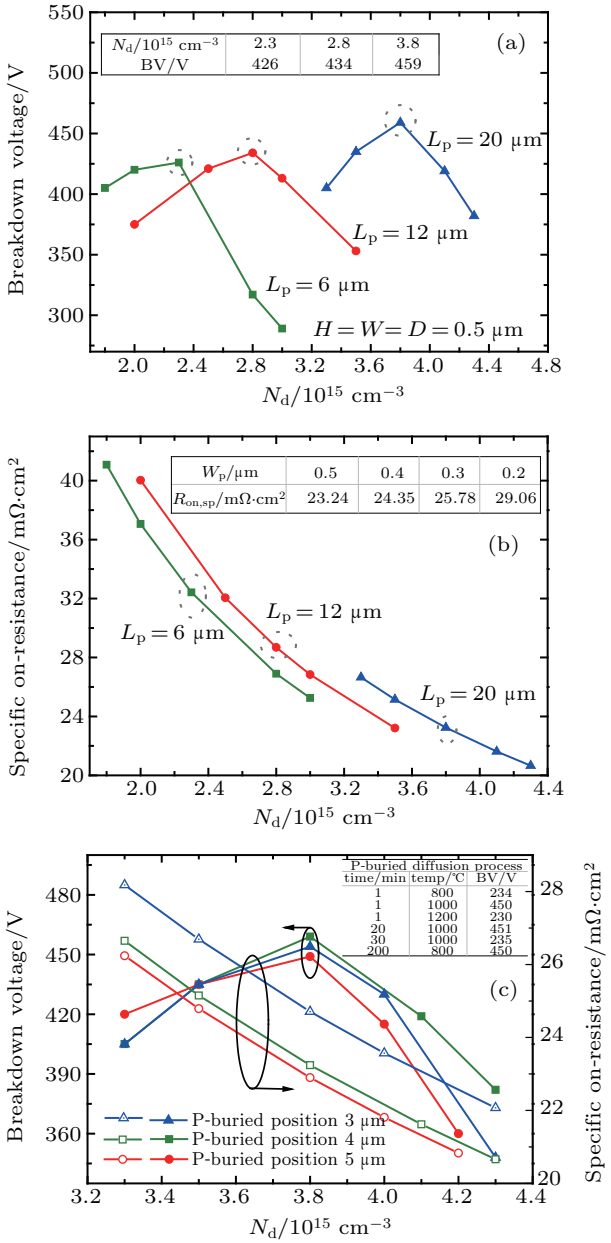


Fig. 6. Influence of N_d on the BV and $R_{on,sp}$ with different (a) L_p, (b) W_p, and (c) the P-buried position.

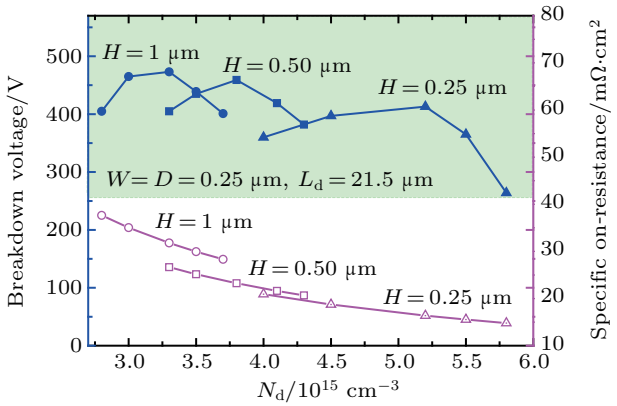


Fig. 7. BV and $R_{on,sp}$ versus N_d with different H.

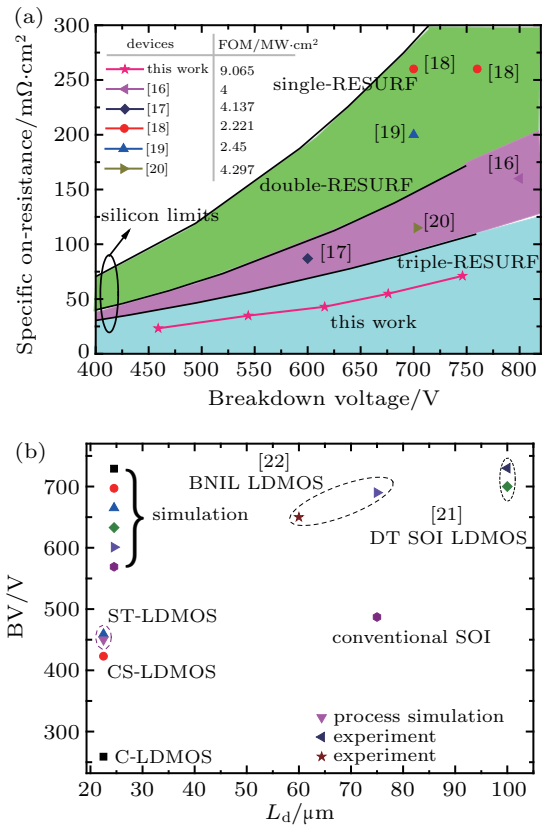


Fig. 8. (a) The $R_{on,sp}$ versus BV relationship of the ST-LDMOS, (b) the BV versus L_d relationship.

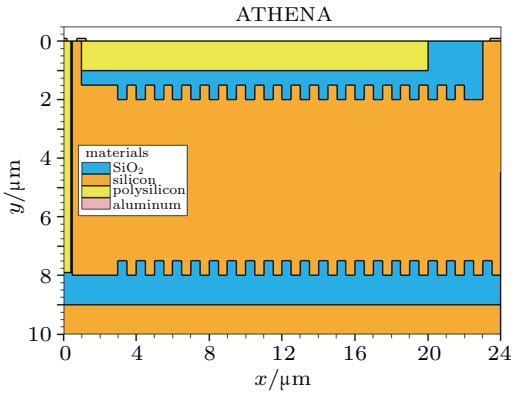


Fig. 9. Process simulation of ST-LDMOS.

The trench substrate is created by the wafer bonding technology. A layer of high-quality 0.2 μm thick SiO_2 layer is thermally oxidized on the surface of the silicon groove, then repeatedly accumulated, so as to obtain SiO_2 with set thickness, good interface characteristics, and density. The bonding process is consistent with the conventional preparation process by using the planarization method combined with chemical mechanical polishing (CMP). The P-buried layer is formed by diffusion process. The remaining technology is compatible with the traditional CMOS process.

4. Conclusion

A stacked LDMOS with enhanced depletion effect by surface substrate is proposed. Due to the electric field modulation effect in SDT, the proposed structure greatly increases the BV. The $R_{on,sp}$ is improved based on the depletion enhancement of the double substrates. The ST-LDMOS exhibits an off state BV of 459 V and a $R_{on,sp}$ of 23.24 mΩ·cm^2. The ST-LDMOS increases the BV by 77.22% and reduces the $R_{on,sp}$ by 41.34% compared with the C-LDMOS. In addition, it reduces the size of the device and has potential applications in the PIC.

References

[1] Jin-rong M, Ming Q and Bo Z 2015 *Chin. Phys. B* **24** 047303
[2] Zhang Y H, Wei J, Yin C, Tan Q, Liu J P , Li P C and Luo X R 2016 *Chin. Phys. B* **25** 027306
[3] Qian Q, Sun W, Wei S, Liu S and Shi L 2012 *IEEE Trans. Device Mater. Reliab.* **12** 146
[4] Zhou K, Luo X, Xu Q, Li Z and Zhang B 2014 *IEEE Trans. Electron. Devices* **61** 2466
[5] Luo X, Udrea F, Wang Y, Yao G and Liu Y 2010 *IEEE Electron Dev. Lett.* **31** 594
[6] Luo X, Zhang B and Li Z 2007 *Solid. State. Electron.* **51** 493
[7] Li W, Zheng Z, Wang Z, Li P, Fu X, He Z, Liu F, Yang F, Xiang F and Liu L 2017 *Chin. Phys. B* **26** 017701
[8] Zhang W, Zhan Z, Yu Y, Cheng S, Gu Y, Zhang S, Luo X, Li Z, Qiao M, Li Z J and Zhang B 2017 *IEEE Electron Dev. Lett.* **38** 1555
[9] Tsai J Y and Hu H H 2016 *IEEE J. Electron. Devices Soc.* **4** 430
[10] Wu L J, Hu S D, Zhang B and Li Z J 2011 *Chin. Phys. B* **20** 107101
[11] Hu Y, Liu H, Xu Q, Wang L, Wang J, Chen S, Zhao P, Wang Y and Wang G 2017 *IEEE J. Electron. Devices Soc.* **5** 157
[12] Cheng J, Chen W and Li P 2018 *IEEE Trans. Electron Dev.* **65** 1404
[13] Wang Y, Wang Z, Bai T and Kuo J B 2018 *Fellow IEEE Trans. Electron Dev.* **65** 1056
[14] Zhang B, Li Z, Hu S and Luo X 2009 *IEEE Trans. Electron. Devices* **56** 2327
[15] Duan B, Zhang B and Li Z 2005 *Solid. State. Electron.* **49** 1965
[16] Raba M, Bdra M, Demlb G, Kapelsc H, Schmittc M, Sedlmaierc S, Tolksdorf C and Willmerothc 2006 *Proc. 18th Int. Symp. Power Semicond. Devices ICs, Hiroshima,* 4–8 June 2006, Naples, Italy
[17] Disney D R, Paul A K, Darwish M, Basecki R and Rumennik V 2001 *Semicond. Devices ICs* 2001 *ISPSD'01. Proc. 13th Int. Symp.*, 7–7 June 2001, Osaka, Japan
[18] Kim M H, Kim J J, Choi Y S, Jeon C K, Kim S L, Kang H S and Song C S 2002 *Eur. Solid-State Device Res. Conf.*, 24–26 Sept. 2002, Firenze, Italy
[19] Hossain Z, Ishigwo T, Tu L, Corleto H, Kuramae F and Nair R 2004 *Power Semicond. Devices ICs* 2004 *Proceedings. ISPSD '04. 16th Int. Symp.* 237
[20] Fujishima N, Saito M, Kitamura A, Urano Y, Tada G and Tsuruta Y 2001 *Power Semicond. Devices ICs (ISPSD'01)*, 4–7 June 2001, Osaka, Japan
[21] Luo X, Zhang B, Guo Y, Tang X and Liu Y 2007 *IEEE Electron Device Letters* **28** 422
[22] Luo X, Zhang B, Lei T, Wang Y, Gao H, Fang J, Qiao M, Zhang W, Deng H, Zhang B, Li Z, Xiao Z, Chen Z and Xu J 2009 *IEEE Electron Device Letters* **30** 1093