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Citation: Chin. Phys. B . 2019, 28(2): 027303. **doi:** 10.1088/1674-1056/28/2/027303
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Influence of deep defects on electrical properties of Ni/4H-SiC Schottky diode*

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(Received 28 August 2018; revised manuscript received 27 November 2018; published online 10 January 2019)

In this paper, we investigate the influence of deep level defects on the electrical properties of Ni/4H–SiC Schottky diodes by analyzing device current–voltage (I–V) characteristics and deep-level transient spectra (DLTS). Two Schottky barrier heights (SBHs) with different temperature dependences are found in Ni/4H–SiC Schottky diode above room temperature. DLTS measurements further reveal that two kinds of defects $Z_{1/2}$ and Ti(c)^{a} are located near the interface between Ni and SiC with the energy levels of E_C–0.67 eV and E_C–0.16 eV respectively. The latter one as the ionized titanium acceptor residing at cubic Si lattice site is thought to be responsible for the low SBH in the localized region of the diode, and therefore inducing the high reverse leakage current of the diode. The experimental results indicate that the Ti(c)^{a} defect has a strong influence on the electrical and thermal properties of the 4H–SiC Schottky diode.

Keywords: 4H–SiC Schottky diodes, Schottky barrier heights, deep defects, DLTS

PACS: 73.40.Sx, 61.72.J–, 71.55.–i, 73.30.+y **DOI:** 10.1088/1674-1056/28/2/027303

1. Introduction

The SiC Schottky barrier diode (SBD) has attracted widespread attention in high-power and high-frequency electronic applications due to its ideal physical and chemical properties of SiC, such as high reverse breakdown voltage, short reverse recovery transient, high operating temperature and low switching loss.[1–3] However, SiC SBD currently suffers the inhomogeneity of Schottky barrier heights (SBHs), which may increase leakage current and reduce breakdown voltage.[4]

The inhomogeneity of SBHs has been widely investigated by measuring the current–voltage (I–V) properties of SiC SBD. A large number of studies have shown that the inhomogeneity of SBHs is related to the presence of defects. The various origins of the defects from the materials and devices have been reported, including crystallographic defects (micropipes, dislocations, grain boundaries, stacking faults, *etc.*)[5–7] and surface defects (comets, carrots, growth pits, scratches, and so on).[8,9] The micropipes are regarded as "killer defects" originating from growth processes, resulting in serious performance degradation of SiC SBD. Fortunately, the present innovative epitaxial growth technologies have reduced the number of micropipes to a negligible value (< 1 cm^{-2}).[10] In addition, the "latent defects" such as defect clusters and deep defects have a strong influence on the electrical performance and reliability of SiC SBD. They may cause device performance to degrade at high temperature and high bias voltage, finally leading to the device failure in the practical operation. Ewing *et al.* have also revealed that the defect clusters situated near the metal/SiC interfaces create partial low-barrier patches, resulting in the SBHs' inhomogeneity.[11] Furthermore, Mandal *et al.* have reported that the differences in performance and leakage current among the different SiC SBDs are attributed to the existence of varying degrees of deep defects.[12] Rao *et al.* have shown that the leakage current is due to the effect of electrical field and temperature on the emission of electrons from a trap state in Schottky diodes.[13] Although these deep level defects have been studied, the physics mechanism of defects or trap influence on the barrier height and the leakage current of SiC SBD are still unclear. In order to further explore the physics behind the correlation between the properties of the SiC SBDs and deep defects, the present work focuses on the diode performance study with consideration of junction properties, leakage current and defect behaviors near the interfaces.

In this work, the current–voltage (I–V) characteristics of SiC Schottky diode at various temperatures are measured to study the barrier height inhomogeneity and the reverse current transport mechanism. The deep-level transient spectrum (DLTS) measurements are performed in a temperature range of 80 K–450 K to investigate the deep level defects. The experimental results reveal that the deep level defects can be responsible for the observed barrier height inhomogeneity. The presence of deep level defects lowers the Schottky barrier height,

*Project supported by the National Key Research and Development Program of China (Grant No. 2016YFB0400402).
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thus significantly affects the electrical characteristics of SiC Schottky diode.

2. Experiment

The 4H–SiC SBDs were fabricated on Si-face 4-inch (1 inch = 2.54 cm) 4H–SiC n-type substrates. The substrates had been highly doped with nitrogen and cut off at 8° towards the [11$\bar{2}$0] direction. The schematic structure of the fabricated Schottky diodes is shown in Fig. 1. A 13-μm-thick n-type epilayer with a doping concentration of 6×10^{15} cm^{-3} was grown by the chemical vapor deposition (CVD) technique. Here, SiH_4, C_3H_8, and HCl were used as source gases while H_2 was selected for dilution and carrier gas. The typical epitaxial growth rate was fixed at 12 μm/h, and the epitaxial temperature and growth pressure were controlled within 1550 °C–1600°C and 50 mbar–150 mbar (1 bar = 10^5 Pa), respectively. Finally, a 75-nm Ni Schottky contact layer and a 100-nm Ni Ohmic contact layer were sputtered in the front and back sides of the device respectively. The Ni Ohmic contact was formed by annealing in nitrogen at 1000 °C for 5 min, and the obtained ohmic contact resistivity was 5.25×10^{-6} Ω·cm^2 by the transmission line mode (TLM) and four-probe measurement.

The electrical measurements were conducted by using a Keithley 4200 semiconductor characterization system in a Cascade Summit 12000 probe station with a built-in temperature controller. The temperature of the sample holder can be tuned from 210 K to 470 K continuously with an error less than 0.1 K. The *C*–*V* characteristic measurements were conducted at a frequency of 1 MHz. The DLTS measurements were performed to analyze the deep level defects by using DLS-83D Deep Level Transient Spectroscopy test system based on standard techniques.

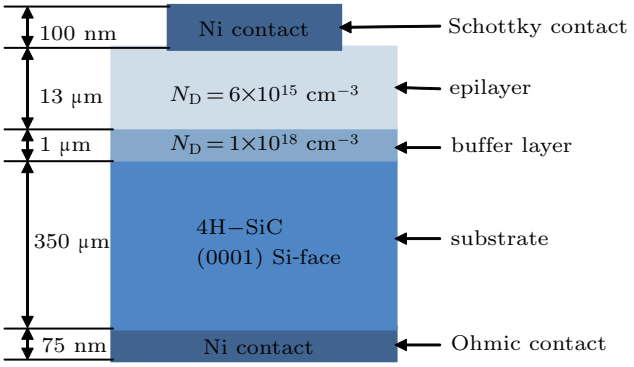


Fig. 1. Schematic structure of Ni/4H–SiC Schottky barrier diode.

3. Results and discussion

Figure 2 shows the typical forward current–voltage (*I*–*V*) characteristics of Ni/4H–SiC SBD in a temperature range of 300 K–423 K in steps of 15 K. It is found that the forward current has different behaviors with varying temperature. In a relatively low temperature range $T \leq 348$ K, the forward current curves each show a single slope, suggesting that the SBD has a unique barrier height, which can be associated with the thermionic emission (TE) theory given by[14,15]

$$J = J_{\rm sat}\left[\exp\frac{qV}{nkT} - 1\right]. \tag{1}$$

Here, the reverse-saturation current $J_{\rm sat}$ is defined as

$$J_{\rm sat} = A^* T^2 \exp\left(\frac{-q\Phi_{\rm B0}}{kT}\right), \tag{2}$$

where n represents the ideality factor, V is the applied voltage, $\Phi_{\rm B0}$ is the zero bias Schottky barrier height, and A^* is the effective Richardson constant with 146 A/cm^2·K^2 for 4H–SiC.[16] The values of the barrier height $\Phi_{\rm B0}$ and the ideality factor n can be calculated from intercepts and slopes of the semi-logarithmic forward *I*–*V* characteristics by using Eqs. (1) and (2). At room temperature, the extracted n from the *I*–*V* curves is 1.03 for Ni/4H–SiC diode. The ideality factor n close to one indicates that the TE mechanism is responsible for the current transport through the Schottky junction. In addition, the extracted $\Phi_{\rm B0}$ from *I*–*V* plots is 1.53 eV which is consistent with the value extracted from *C*–*V* plots for Ni/4H–SiC diode. On the other hand, as the temperature increases to above 348 K, the semi-logarithmic *I*–*V* curves exhibit distinct slopes corresponding to the low voltage region ($V \leq 0.7$ V) and moderate voltage region (0.7 V$< V \leq 1.1$ V), respectively. Such an unexpected behavior can be attributed to the spatially inhomogeneous barrier heights and potential fluctuations at the interface.[17,18] We use a simple model based on TE theory with two independent Schottky barrier heights in parallel[19,20] to express the forward current density as

$$J_{\rm F} = J_{\rm sat}^{\rm H}\exp\left[\frac{qV}{n^{\rm H}kT}\right] + J_{\rm sat}^{\rm L}\exp\left[\frac{qV}{n^{\rm L}kT}\right]. \tag{3}$$

Here, $J_{\rm F}$ represents the forward current density, the superscripts L and H denote the low and high barrier regions, respectively. The extracted values of n and $\Phi_{\rm B0}$ at each temperature in the L-SBHs and H-SBHs regions are summarized in Table 1. As seen in Fig. 3, the value of $\Phi_{\rm H-SBH}$ ranges from 1.53 (300 K) to 1.60 (423 K), and the value of $\Phi_{\rm L-SBH}$ changes from 1.29 (363 K) to 1.37 (423 K). Figure 3 and Table 1 show that $\Phi_{\rm L-SBH}$ and $\Phi_{\rm H-SBH}$ increase and the $n_{\rm L}$ and $n_{\rm H}$ decrease with temperature increasing. Aydın *et al.*[21] and Kumar *et al.*[22] attributed such behavior to the existence of Gaussian distribution (GD) of the SBHs around a mean value due to SBH inhomogeneity at the M/S interface. Özavcı *et al.* further confirmed that the temperature dependence of double SBH and the ideal factor can be successfully explained in terms of the TE mechanism with a double GD of SBHs for the low bias region and the moderate bias region, respectively.[23] Since our experimental results in this paper are consistent with the results in the above literature, it can be considered that the variation of $\Phi_{\rm B0}$ and n with temperature are mainly due to the

double GD at the interface. Therefore, current flows primarily through the patches of lower barrier height at the low temperature. As the temperature rises, more and more electrons have sufficient energy to overcome the higher barriers, and therefore increasing the barrier height.[24] Additionally, the value of n greater than 1 is due to other mechanisms besides thermionic emission. Many researchers have reported that such behavior can be due to thermionic field emission (TFE) tunneling, surface states, and interface traps, or inhomogeneous barrier height distribution at the interface, *etc*.[25,26] It can also be seen that the excess current appears at the temperature above 348 K. This means that the excess current flows through the increasing L-SBH area induced by the thermally activated defects at the low voltage. The increasing low barrier patches lead to a higher degree of inhomogeneity of SBHs, and the local low barrier heights can be attributed to the existence of the possible defect energy level below the conductive energy level E_C of SiC.

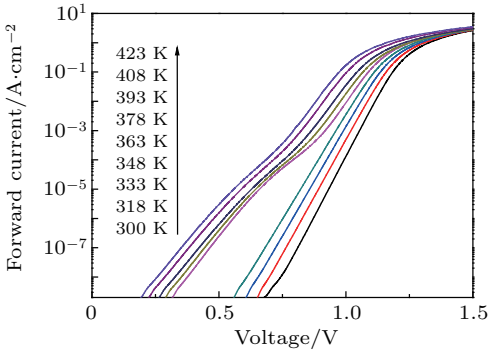


Fig. 2. Semi-logarithmic forward *I–V* characteristics on Ni/4H–SiC Schottky barrier diode in temperature range of 300 K–423 K in steps of 15 K.

Table 1. Temperature dependent values of n and Φ_{B0} for Ni/4H–SiC Schottky barrier diodes obtained from forward bias *I–V* characteristics.

T/K	Moderate bias region		Low bias region	
	Φ_{H-SBH}/eV	n_H	Φ_{L-SBH}/eV	n_L
300	1.530	1.025		
318	1.537	1.023		
333	1.552	1.019		
348	1.560	1.017		
363	1.565	1.015	1.289	1.287
378	1.574	1.013	1.308	1.269
393	1.584	1.01	1.321	1.245
408	1.589	1.008	1.347	1.199
423	1.599	1.006	1.374	1.153

To understand the individual contributions of the L-SBH and H-SBH regions to the leakage current in the measured temperature and voltage range, an analytical model is presented where two proportions of regions with different barrier heights are equivalent to two Schottky barrier heights in parallel.[27] The total leakage current density (J_L) is modeled by two components, which is expressed as

$$J_L = ZJ_{L-SBH} + (1-Z)J_{H-SBH}, \tag{4}$$

where Z denotes the ratio of the area of the L-SBH region to the total diode area, J_{L-SBH} and J_{H-SBH} are the current density flowing through L-SBHs and H-SBHs regions, respectively and they obey the TE theory described in Eq. (1). As the leakage currents are measured at the relatively high reverse bias, the image-force related barrier-height lowering ($\Delta\Phi_B$) due to the electric field across the Ni/SiC interface should be also considered with the following relation:[28]

$$\Delta\Phi_B = \sqrt{\frac{qE_y}{4\pi\varepsilon_s\varepsilon_0}}, \tag{5}$$

where the electric field E_y across the M/S interface, is defined as

$$E_y = \sqrt{\frac{2qN_DV_R}{\varepsilon_s\varepsilon_0}}. \tag{6}$$

Figure 4(a) shows the reverse *I–V* characteristics of Ni/4H–SiC SBD in an applied bias region of 0 V–200 V at various temperatures, and the calculated and experimental reverse *I–V* characteristics of Ni/4H–SiC SBD at 363 K, 378 K, and 393 K are shown in Figs. 4(b)–4(d). Based on the model described above, using the fitting parameters listed in Table 2, the theoretical fits are shown to be in good agreement with the experimental reverse *I–V* plots in the applied bias range of 0 V–200 V. It can be seen that the magnitude of leakage current is dominated by the contribution from L-SBHs regions. At 363 K and 378 K, the extracted Z values are equal to 0.0113 and 0.0117, respectively. At 393 K, the extracted Z value of the low barrier area is increased to 0.0312, *i.e.*, $Z = 0.0312$, and then breaks down. The increasing of low barrier patches leads to a higher leakage current, and these results are well consistent with the observation from forward *I–V* plot. Increasing the area Z seems to dramatically increase the leakage current. This result indicates that a small Schottky barrier height inhomogeneity or localized lowering of the barrier height can significantly affect the reverse *I–V* characteristics of metal/4H–SiC Schottky contacts.

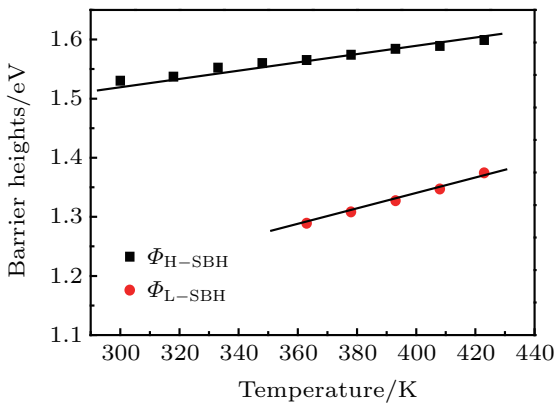


Fig. 3. Variations of barrier height from the forward *I–V* for low bias region and moderate bias region with temperature.

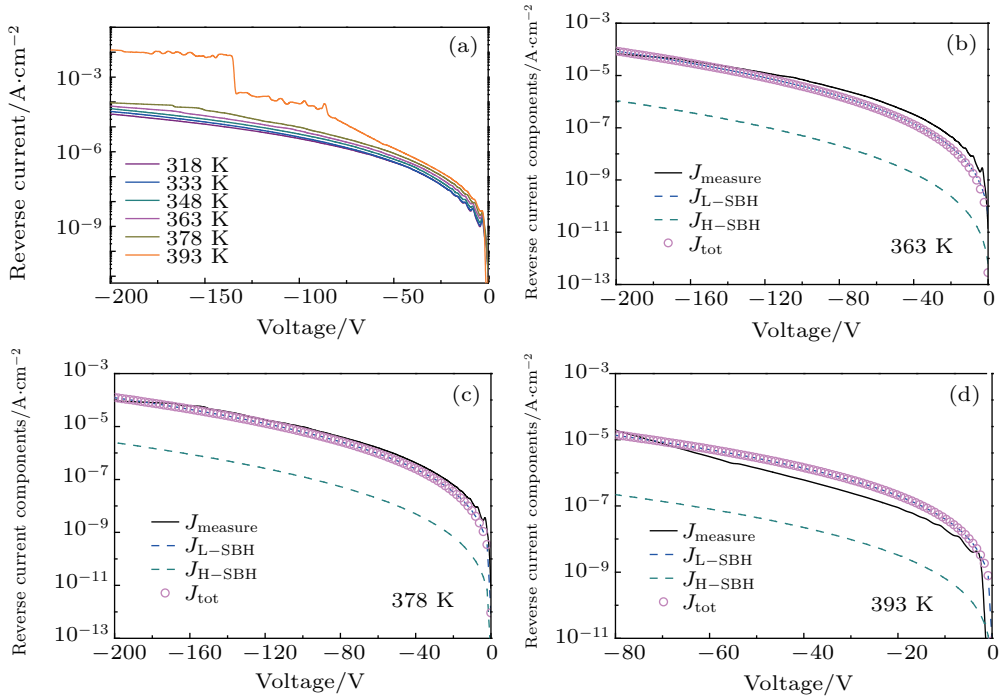


Fig. 4. (a) Semi-logarithmic reverse *I*–*V* characteristics of Ni/4H–SiC Schottky barrier diode in the temperature range of 300 K–423 K in steps of 15 K. Experimental and simulated reverse *I*–*V* characteristics of Ni/4H–SiC Schottky barrier diode at (b) $T = 363$ K, (c) $T = 378$ K, and (d) $T = 393$ K. Solid lines are for measured data, solid circles and dashed lines are for simulated results. Leakage current components due to high-SBH and low-SBH region are also shown.

Table 2. Defect parameters obtained from the DLTS measurements.

Trap #	σ/cm^2	ΔE/eV	N_t/cm^{-3}	Possible trap identity
E1	5.89×10^{-15}	E_C-0.66	$4.2\times10^{+12}$	$Z_{1/2}$ intrinsic defect
E2	2.60×10^{-15}	E_C-0.16	$7.6\times10^{+12}$	Ti(c)[a] impurity defect

The average values of activation energy ($E_a = 0.16$ eV) are calculated from the thermal dependence of leakage current at various bias voltages as shown in Fig. 5. It is indicated that the localized defects exist in the epitaxial layer at the metal/SiC interface, which can lower the barrier height of the Schottky contact at the defect site. The schematic of basic reverse leakage current mechanisms of a Schottky diode is shown in Fig. 6, which shows (a) thermionic emission, (b) thermionic field emission, (c) field emission,[29] and also (d) the defects related leakage current. The leakage current is greatly dependent on the nature of the defects in the presence of electrically active defect centers. As shown in Fig. 6, the existence of the possible defects with E_T below the conductive energy level E_C of SiC can induce the local defective current paths. At the relatively high temperature, the defects promote the ability of electrons to be injected into the conduction band, and thus increasing the reverse current and causing the observed *I*–*V*–*T* characteristics in Fig. 4. Trap and defect-assisted tunneling, and barrier-thinning caused by charge trapping could be responsible for this excessive leakage current. This mechanism has already been proved by the fact that the ideality factors extracted from the forward *I*–*V*–*T* plots are greater than 1.

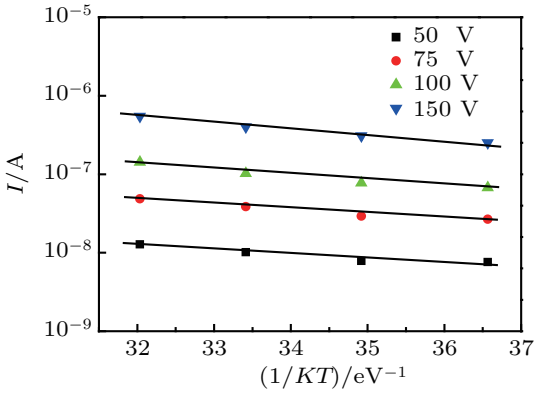


Fig. 5. Activation energy extracted from reverse *I*–*V* characteristics of Ni/4H–SiC Schottky barrier diode at various voltages.

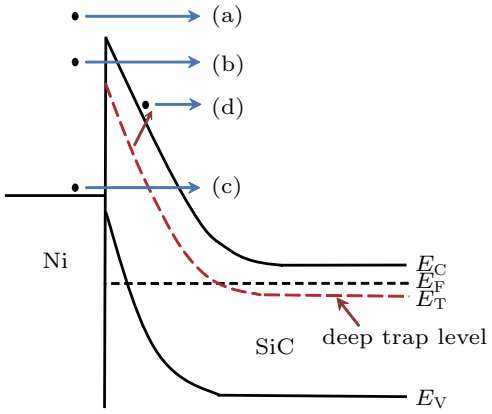


Fig. 6. Schematic diagram of the current conduction mechanism in Ni/4H–SiC Schottky diode, showing (a) thermionic emission, (b) thermionic field emission, (c) field emission, and (d) the defects related leakage current that may occur.

To further understand the defect properties near the

Ni/SiC interface of diode, DLTS measurements are carried out in a temperature range of 80 K–450 K. Figure 7 shows the typical DLTS results for Ni/4H–SiC SBD under the measurement conditions of a reverse bias of −3 V and the pulse voltage of 0 V with a pulse width of 50 μs. Both peaks of E1 and E2 are related to majority carrier traps (electron traps in this case) are observed. The inset of Fig. 7 shows the Arrhenius plots for all the peaks obtained from the DLTS spectra. The parameters of defects, such as activation energy, capture cross-section and defect density are calculated from the temperature-dependent thermal emission rates of the traps and summarized in Table 2. The defect level corresponding to E1 peak is located at E_C-0.67 eV.[30,31] This trap is widely designated as $Z_{1/2}$, an intrinsic growth defect in SiC and most likely related to carbon vacancies.[32] For E2 peak, the defect level is situated at E_C-0.16 eV, which is attributed to the ionized titanium acceptor residing at cubic Si lattice sites.[33–35] Zhang *et al.*[36] and Dalibor *et al.*[37] have also identified the similar defect level E_C–0.16 eV for a Ti electron trap level in as-grown SiC epilayers. The Ti may be a background impurity as a result of its presence in the graphite susceptor used in the high temperature region in the growth chamber. Combining the analysis of the DLTS property and that of *I*–*V* property, the observed Ti impurities level is consistent with the mean activation energy E_a previously extracted from the leakage current, which causes the barrier height to locally lower. These defects are electrically active and can lead the diode leakage current to increase by acting as trap or recombination and generation centers. The character of Ti deep trap can be responsible for the observed barrier height inhomogeneity at the temperature above 348 K. Therefore, the presence of deep level defects can significantly influence the nature of the Ni/4H–SiC interface and then the electrical characteristics of the SiC Schottky diode.

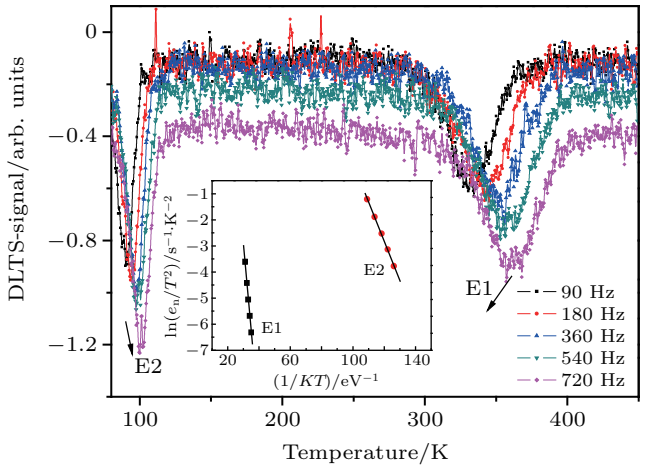


Fig. 7. DLTS spectra measured for different lock-in frequencies and fixed other parameters: $U_R = -3$ V, $U_P = 0$ V, and $t_p = 50$ μs, using Ni/4H–SiC SBD in temperature range 80 K–450 K. Inset shows Arrhenius plots obtained for E1 and E2 from DLTS spectra.

4. Conclusions

The influences of deep defects on electrical properties of Ni/4H–SiC Schottky diodes are investigated in depth. The inhomogeneities of SBHs (∼ 1.53 eV high SBH and ∼ 1.28 eV low SBH) are discovered in the forward *I*–*V* characteristics at temperatures above 348 K. Meanwhile, the inhomogeneity of barrier heights is also found to increase with increasing temperature. An analytical model is presented to explain the current flowing through the high and low SBHs regions. The low SBH region due to the existence of defects is thought to be main cause for the unusually high reverse leakage current observed in Ni/4H–SiC SBD. The DLTS measurement is carried out to provide key information about the electrical characteristics of SiC/metal interface at localized defect sites. The DLTS results reveal the presence of two kinds of electron traps in the SiC epilayer in the temperature range from 80 K to 450 K, where the deep level defect at E_C–0.67 eV ($Z_{1/2}$) is an intrinsic point defect related to a carbon vacancy in SiC layer, while the defect at E_C–0.16 eV is related to titanium impurity (Ti(c)[a]). The later deep level trap may be the main origin of the low barrier heights and significantly affect the performance of SiC SBD.

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