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Ru Han(韩茹), Hai-Chao Zhang(张海潮), Dang-Hui Wang(王党辉), Cui Li(李翠)

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Optimization of ambipolar current and analog/RF performance for T-shaped tunnel field-effect transistor with gate dielectric spacer*

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A new T-shaped tunnel field-effect transistor (TTFET) with gate dielectric spacer (GDS) structure is proposed in this paper. To further studied the effects of GDS structure on the TTFET, detailed device characteristics such as current-voltage relationships, energy band diagrams, band-to-band tunneling (BTBT) rate and the magnitude of the electric field are investigated by using TCAD simulation. It is found that compared with conventional TTFET and TTFET with gate-drain overlap (GDO) structure, GDS-TTFET not only has the minimum ambipolar current but also can suppress the ambipolar current under a more extensive bias range. Furthermore, the analog/RF performances of GDS-TTFET are also investigated in terms of transconductance, gate-source capacitance, gate-drain capacitance, cutoff frequency, and gain bandwidth production. By inserting a low-κ spacer layer between the gate electrode and the gate dielectric, the GDS structure can effectively reduce parasitic capacitances between the gate and the source/drain, which leads to better performance in term of cutoff frequency and gain bandwidth production. Finally, the thickness of the gate dielectric spacer is optimized for better ambipolar current suppression and improved analog/RF performance.

Keywords: tunneling field effect transistor, T-shaped tunnel field-effect transistor, gate dielectric spacer, ambipolar current, analog/RF performance

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1. Introduction

As MOSFET's sizes continually scaling, the characteristics of MOSFET are affected by various short-channel effects (SCEs), such as drain-induced barrier lowering, surface scattering, and so on.[1–3] In addition, as device sizes continue to shrink, the effects of subthreshold leakage currents on device power consumption are becoming more and more severe.[4–6] However, for MOSFET, the carrier injection in source-channel junction is governed by thermionic emission over the build-in potential barrier and hence the inverse subthreshold slope is limited to 60 mV/decade at room temperature.[7,8] Therefore, tunnel field-effect transistor (TFET) has been actively investigated as one of the most promising candidates for future ultra-low power applications. Due to its band-to-band tunneling (BTBT) based carrier injection mechanism, TFET can overcome the 60 mV/dec subthreshold swing limitation of conventional MOSFET.[9–15] However, low on-current and sizeable ambipolar current are major shortcomings of traditional silicon-based TFET, which limit the use of TFET in low-power and high-frequency applications.[16–21] To improve the drive current while reducing the footprint of TFET, various L-shaped architectures based on gate-source overlap structure and vertical channel have been proposed.[22–32] However, it has been pointed out that conventional L-TFET suffers from severe ambipolar behavior, which needs further optimizations.[32,33]

Recently, a T-shaped TFET (TTFET) with gate-drain overlap (GDO) structure has been proposed to improve the drive current and suppress the ambipolar current simultaneously.[34] However, it is found that this T-shaped TFET with GDO structure (GDO-TTFET) can only suppress ambipolar current when V_{ds} is low. Besides, the GDO structure also increases the gate-drain capacitance, resulting in poor RF/analog performance.

To suppress the ambipolar current under a more extensive bias range while improving the RF/analog performance, a new T-shaped TFET with gate dielectric spacer (GDS) structure is proposed in this paper. TCAD simulation results show that our proposed T-shaped TFET with GDS (GDS-TTFET) not only suppress ambipolar current over a broader bias range but also improves analog/RF performance compared with GDO-TTFET. To implement the proposed GDS structure, just a layer of low-κ dielectric needs to insert between the high-κ dielectric and gate electrode material. Additionally, the process of the GDS-TTFET is compatible with the self-aligned process used in Ref. [33], which makes the process of GDS-TTFET much simpler than that of GDO-TTFET.

2. Device structure and simulation method

The proposed T-shaped TFET with gate dielectric spacer (GDS-TTFET) is shown in Fig. 1(a). The device contains two vertical gate-overlapped channels and two lightly doped p-type tunneling regions located between the source and the gate dielectric layer. Below the gate electrode, a low-κ dielectric

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spacer is inserted between the gate electrode and the high-κ gate dielectric. Based on the process steps of LTFET demonstrated in Ref. [33], T-shaped TFET (TTFET) with symmetrical vertical double gate structure can be easily fabricated. Therefore, based on conventional TTFET processes, the structure proposed in this paper can be achieved only by adding a layer of gate dielectric spacer.

The detailed device parameters are listed below: height of the gate $H_G = 50$ nm, height of the source $H_S = 30$ nm, height of the drain $H_D = 10$ nm, width of the gate $W_G = 10$ nm, width of the source $W_S = 20$ nm, width of tunneling region between the source and the gate dielectric layer $W_{tun} = 3$ nm, thickness of the high-κ gate dielectric $T_{OX} = 2$ nm, the default height of the inserted low-κ gate dielectric spacer $H_{spacer} = 4$ nm, gate work function $\Phi = 4.2$ eV, p^+ type source doping $N_S = 10^{20}$ cm^{-3}, p^- type channel doping $N_{Sub} = 10^{17}$ cm^{-3}, and n^+ type drain doping $N_D = 10^{20}$ cm^{-3}. For comparison, conventional TTFET and GDO-TTFET proposed in Ref. [34] are also demonstrated in Figs. 1(b) and 1(c), respectively.

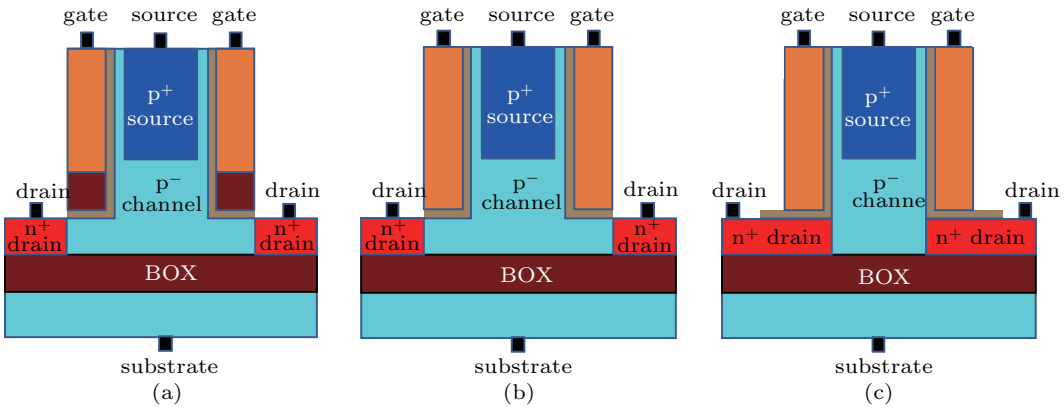


Fig. 1. Cross-sectional view of (a) proposed GDS-TTFET, (b) conventional TTFET, and (c) GDO-TTFET proposed in Ref. [34].

In this paper, the three devices mentioned above are all silicon-based and investigated by using Sentaurus TCAD with a dynamic nonlocal tunneling model. With this dynamic nonlocal tunneling approach, tunneling paths are dynamically determined according to the variation of the electric field, so it can model the tunneling process more accurately, especially for non-planner TFET like L-shaped and T-shaped TFET. According to Ref. [37], two calibrated Kane's tunneling model coefficients for silicon are $A = 4.0 \times 10^{14}$ cm$^{-1} \cdot$ s^{-1} and $B = 9.9 \times 10^6$ V/cm. In addition to using the BTBT model, the OldSlotboom band-gap narrowing model and Shockley–Read–Hall recombination model are also used in the TCAD simulations. For simplicity, an idealized device structure with abrupt source/drain-channel junctions has been considered, and the defect-related traps and charges are ignored in this paper.

3. Simulation results and discussion

3.1. Performance comparison between conventional TTFET, GDO-TTFET, and GDS-TTFET

The I_{ds}–V_{gs} for conventional TTFET, GDO-TTFET, and GDS-TTFET at $V_{ds} = 1.5$ V is shown in Fig. 2. It is clear that when V_{gs} is negatively biased from -2.0 V to 0 V, the GDS-TTFET has the lowest ambipolar current. Especially, when $V_{gs} = -1.0$V, the bipolar current of the GDS-TTFET is reduced to the order of 10^{-11} A/μm, which is 4 orders of magnitude smaller than that of conventional TTFET and 5 orders of magnitude lower than that of GDO-TTFET. It is also noticed that since the source structure of conventional TTFET, GDO-TTFET, and GDS-TTFET are identical, the I_{ds}–V_{gs} of those three devices are the same when V_{gs} is positively biased from 0 V to 2.0 V.

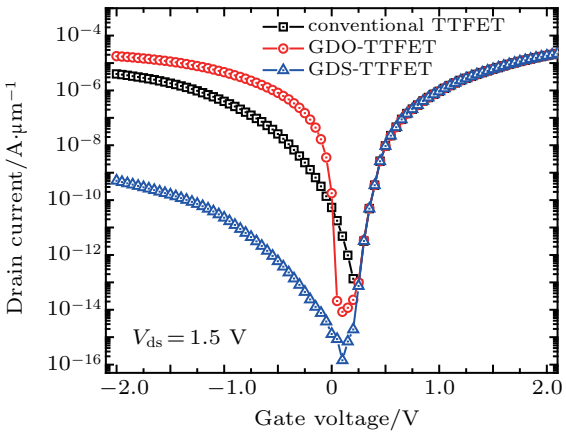


Fig. 2. I_{ds}–V_{gs} for conventional TTFET, GDO-TTFET, and GDS-TTFET with $V_{ds} = 1.5$ V.

To further explain why the GDS structure can effectively suppress the ambipolar current, energy band profiles of conventional TTFET, GDO-TTFET, and GDS-TTFET are plotted in Fig. 3. It can be seen that when $V_{ds} = 1.5$ V and $V_{gs} = -2.0$ V, the conduction band of the drain is far below the valence band of the channel, which produces a wide tunneling window for holes from the conduction band of the drain

to the valence band of the channel when gate voltage is negatively biased. As the tunneling windows appears, the band to band tunneling (BTBT) probability is mainly determined by the width of the tunneling barrier, which is defined as the closest distance between the conduction band and the valence band when tunneling window is open. By inserting the low-κ gate dielectric spacer between the gate electrode and the gate dielectric, the GDS structure effectively reduces the influence of the gate bias on the lateral channel potential when the gate voltage is reversely biased at $V_{gs} = -2.0$ V, leading to a slow variation of energy band profile. It can be seen from Fig. 3 that GDS-TTFET has the widest tunneling distance, which means the smallest tunneling probability, and thus the lowest ambipolar current when the gate voltage is negatively biased.

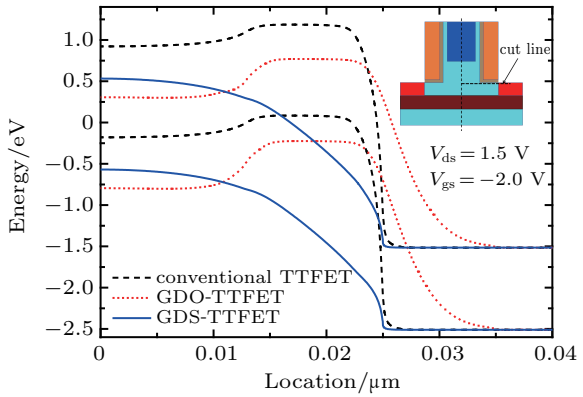


Fig. 3. Energy band diagram alone the channel at $V_{ds} = 1.5$ V and $V_{gs} = -2.0$ V for conventional TTFET, GDO-TTFET, and GDS-TTFET.

It also should be noticed that although GDO-TTFET has a wider tunneling width than conventional TTFET, it has larger ambipolar current than conventional TTFET. This because that by using gate-drain overlap (GDO) structure, BTBT current of GDO-TTFET is dominated by the tunneling component perpendicular to the channel, which also referred to as "line tunneling".[11]

Figure 4 shows the energy band diagram perpendicular to the channel for conventional TTFET, GDO-TTFET, and GDS-TTFET. It can be seen that the energy band diagram of the GDO-TTFET has the most significant band bending curvature at the channel surface, resulting in a small tunneling distance between the valence band and the conduction band, thereby causing substantial "line tunneling" BTBT current. However, for GDS-TTFET, the band-bending curvature perpendicular to the channel direction is so small that there are no tunneling windows and no "line tunneling" occurs.

For better explanation, 2D contour plots of the BTBT generation G_{BTBT} for conventional TTFET, GDO-TTFET, and GDS-TTFET at $V_{ds} = 1.5$ V and $V_{gs} = -2.0$ V are shown in Fig. 5. According to Fig. 5, the G_{BTBT} peak value of the GDS-TTFET is on the order of 10^{25}, which is 6 orders of magnitude smaller than that of the conventional TTFET and GDO-TTFET. Since higher G_{BTBT} and larger BTBT distribution area will result in greater tunneling current, the GDS-TTFET has the lowest ambipolar current. In addition, although the G_{BTBT} peak value of conventional TTFET and the GDO-TTFET is of the same order of magnitude, since the tunneling area of the GDO-TTFET is much larger than that of the conventional TTFET, the GDO-TTFET has the largest ambipolar tunneling current when gate voltage is biased at $V_{gs} = -2.0$ V.

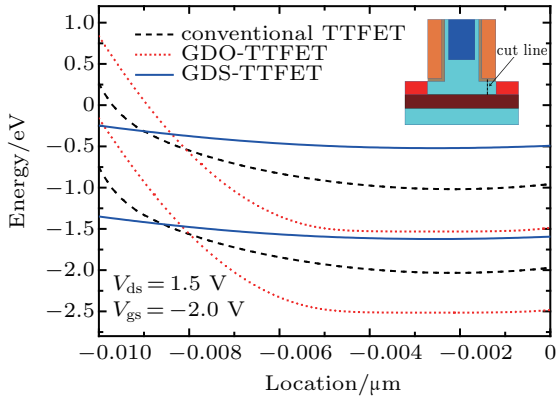


Fig. 4. Energy band diagram perpendicular to the channel at $V_{ds} = 1.5$ V and $V_{gs} = -2.0$ V for conventional TTFET, GDO-TTFET, and GDS-TTFET.

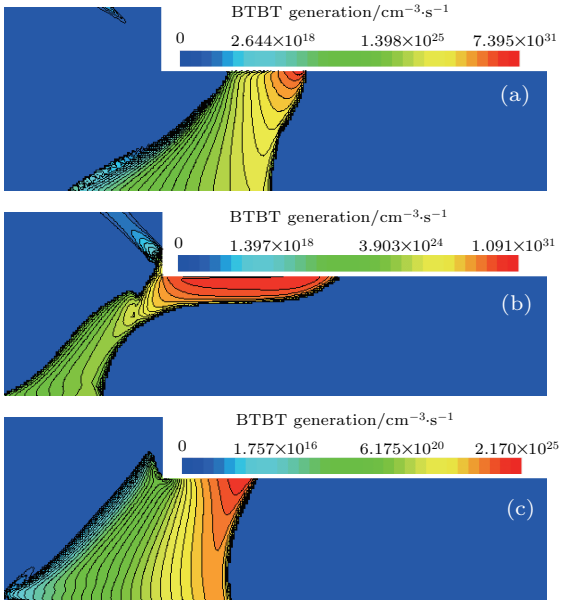


Fig. 5. 2D contour plots of the BTBT generation G_{BTBT} for conventional TTFET (a), GDO-TTFET (b), and GDS-TTFET (c) with $V_{ds} = 1.5$ V and $V_{gs} = -2.0$ V.

The electric field variation along the channel surface from channel to drain for conventional TTFET, GDO-TTFET, and GDS-TTFET are shown in Fig. 6. As can be seen from Fig. 6, for conventional TTFET and GDS-TTFET, there is a spike of electric field variation at the interface between channel region and drain region. According to Kane's theory, when band-to-band tunneling occurs, the tunneling probability exponentially depends on the local electric field strength. It can be seen that the electric field strength of the GDS-TTFET near the channel/drain interface is much smaller than that of the conventional TTFET, which means that GDS-TTFET has lower

ambipolar current than conventional TTFET. Due to the gate-drain overlap structure used in GDO-TTFET, the electric field variation of the GDO-TTFET is different from that of conventional TTFET and GDS-TTFET. In the whole gate-drain overlap region, the electric field strength of the GDO-TTFET remains constant at around 1.0×10^{7} V/cm, which lead to significant "line tunneling" current.

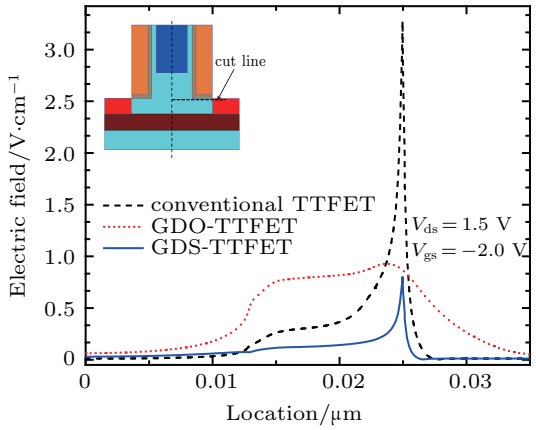


Fig. 6. Electric field variation alone the channel surface from channel to drain for conventional TTFET, GDO-TTFET, and GDS-TTFET with $V_{ds}=1.5$ V and $V_{gs}=-2.0$ V.

Further, the spike of the electric field variation present at the surface of drain/channel junction is the primary cause of the hot carrier effects, which will lead to threshold voltage roll-off and poor device reliability.[35] It is shown in Fig. 6 that the GDS structure can help to reduce the surface electric field near the drain/channel junction. For GDS-TTFET, the electric field is about 3 times smaller than conventional TTFET. Therefore, compared with conventional TTFET, GDS-TTFET has better suppression of hot carrier effects, hence smaller threshold voltage roll-off and better device reliability.

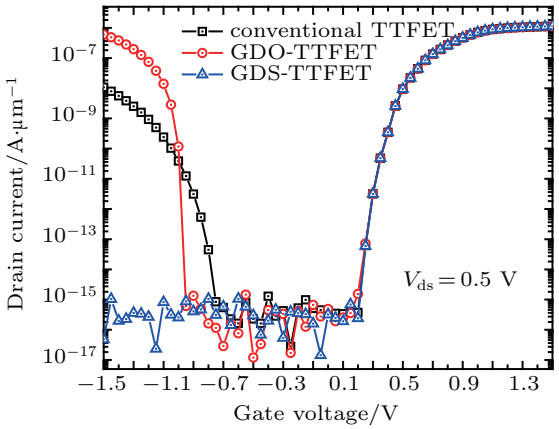


Fig. 7. Transfer characteristics for conventional TTFET, GDO-TTFET, and GDS-TTFET with $V_{ds}=0.5$ V.

When V_{ds} is small, GDS-TTFET still has the advantage over conventional TTFET and GDO-TTFET. As shown in Fig. 7, when V_{gs} is biased at specific voltage range, the ambipolar is equal to the OFF-state current of TTFET, which means TTFET is turned off. It can be seen that the GDS-TTFET has the broadest OFF-state range compared with others (-0.7 V$< V_{gs} <0.2$ V for TTFET, -0.9 V$< V_{gs} <0.2$ V for GDO-TTFET, and -1.5 V$< V_{gs} <0.2$ V for GDS-TTFET). This unique feature of GDS-TTFET makes it have a better application prospect in integrated circuits.

3.2. Parasitic capacitance and analog/RF performance

By inserting a low-κ spacer layer between the gate electrode and the gate dielectric, the GDS structure not only effectively suppress the bipolar current, but also reduce parasitic capacitances between the gate and the source/drain, which are vital parameters for analog/RF performance of TTFET. Figure 8 shows the gate-source and the gate-drain parasitic capacitance versus gate voltage for conventional TTFET, GDO-TTFET, and GDS-TTFET. For simplicity, $V_{ds}=1.0$ V, AC simulation frequency is set to 1 MHz.

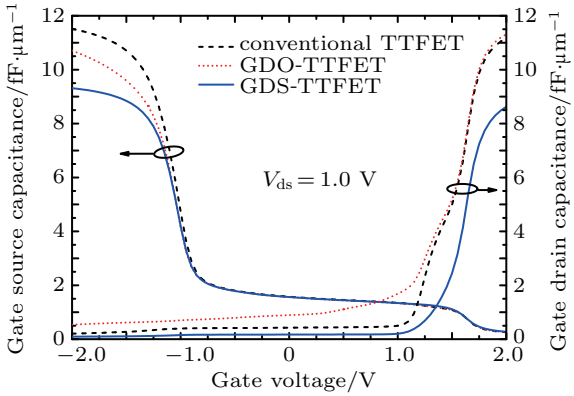


Fig. 8. Gate-source and gate-drain parasitic capacitance versus gate voltage for conventional TTFET, GDO-TTFET, and GDS-TTFET with $V_{ds}=1.0$ V.

It can be seen that compared to conventional TTFET and GDO-TTFET, GDS-TTFET not only has smaller gate-source capacitance but also has smaller gate-drain capacitance, which has a significant impact on cutoff frequency f_T and gain bandwidth production (GBP).

In addition, it is also found that the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} have opposite trends with the gate voltage V_{gs}. For TFETs, the source and drain regions have different types of doping. In this paper, the source region is heavily doped with P-type dopant and the drain region is heavily doped with N-type. So the source region is hole-rich region, while drain region is electron-rich region. When the V_{gs} is biased in the negative range, the inversion layer in the channel is of holes. Thus the gate-source capacitance C_{gs} is larger than the gate-drain capacitance C_{gd}, and the gate-source capacitance C_{gs} becomes larger as the gate voltage is biased more negative. On the contrary, when the V_{gs} is biased in the positive range, the gate-source capacitance C_{gs} becomes small, the gate-drain capacitance C_{gd} is dominant. Since the analog/RF performance of TTFET is mainly

analyzed under the forward operating mode ($V_{gs} > 0$), the gate-drain capacitance has a more significant influence on analog/RF performance than the gate-source capacitance.

Another parameter closely related to analog/RF performance is the transconductance g_m of the TTFET. The g_m of the TTFET device is primarily determined by its forward conduction characteristics, which is mainly dependent on the gate-source structure of the device. Figure 9 shows the transfer characteristics for conventional TTFET, GDO-TTFET, and GDS-TTFET with $V_{ds} = 1.0$ V. It can be seen that since those three TTFET devices have identical gate-source structures, their forward conduction characteristics are the same $I_{ds} - V_{gs}$ relationship or $\log I_{ds}$–V_{gs} relationship. In other words, when V_{gs} is biased within the positive voltage range, those three TTFET devices have the same transconductance.

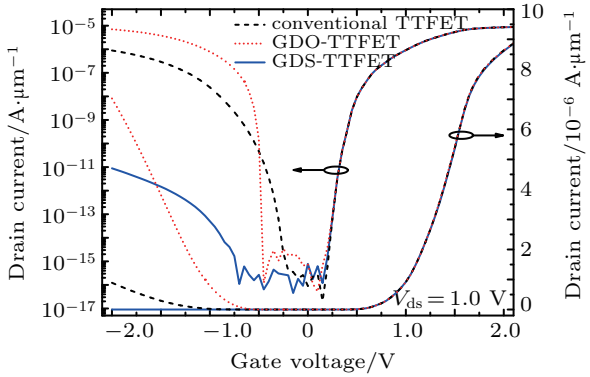


Fig. 9. Transfer characteristics for conventional TTFET, GDO-TTFET, and GDS-TTFET with $V_{ds} = 1.0$ V.

Based on transconductance and parasitic capacitance, two other essential figures-of-merits for analog/RF applications are available: cutoff frequency f_T and gain bandwidth product (GBP). The cutoff frequency depends on the ratio of transconductance to the total capacitance and can be defined as

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)}, \tag{1}$$

where g_m is the transconductance, C_{gs} and C_{gd} are gate to source and gate to drain intrinsic parasitic capacitances.[36]

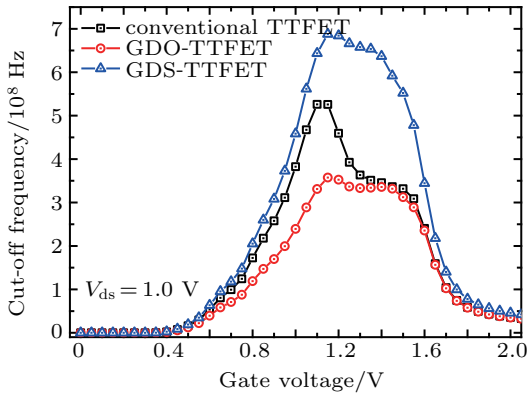


Fig. 10. Cut-off frequency for conventional TTFET, GDO-TTFET, and GDS-TTFET at $V_{ds} = 1.0$ V.

Figure 10 shows the comparisons of f_T as a function of gate voltage for conventional TTFET, GDO-TTFET, and GDS-TTFET. For all these three TTFET devices, it can be seen that cutoff frequency f_T increases with gate voltage increasing and reaches the maximum value when the gate voltage is biased at a specific value, and then the f_T decreases as the gate voltage continues to increase. Moreover, it can be seen that due to the reduced parasitic gate-drain capacitances, GDS-TTFET attains the highest values of f_T as compared with conventional TTFET and GDO-TTFET.

Due to its gate-drain overlap structure, the GDO-TTFE has the largest parasitic gate-drain capacitance among these three TTFET devices, so with the same transconductance, the f_T of the GDO-TTFET is always the smallest when V_{gs} is biased from 0 V to 2.0 V.

The same variation tendencies of gain bandwidth product (GBP) can be found in Fig. 11, while the GBP is defined as

$$\mathrm{GBP} = \frac{g_m}{2\pi 10 C_{gd}}, \tag{2}$$

where g_m is the transconductance and C_{gd} is the gate to drain intrinsic parasitic capacitances.[26] Among these three TTFET devices, the GDS-TTFET has the smallest parasitic gate-drain capacitance C_{gd}, so when the transconductance of the three devices is the same, the GDS-TTFET has the largest GPB.

It also should be noticed that both maximum f_T and maximum GBP of this three TTFET are less than 1 GHz, because silicon-based TTFET still has low on-current I_{ON} due to the silicon's relatively large energy band gap and sizeable effective tunneling mass.[12] Low I_{ON} means small transconductance, which put a limitation on maximum f_T and GBP. Therefore, in the future work, III–V materials and heterojunction structures can be introduced into the TTFET to boost the on-state current and further improve the analog/RF characteristics.

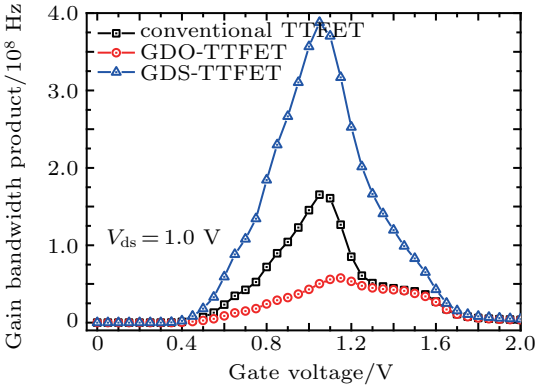


Fig. 11. Gain bandwidth production for conventional TTFET, GDO-TTFET, and GDS-TTFET at $V_{ds} = 1.0$ V.

3.3. Parameter optimization for GDS-TTFET

For GDS-TTFET devices, the thickness of the low-κ dielectric layer inserted between the gate electrode and the gate dielectric is represented by parameter H_{spacer}, which has an

enormous influence on the GDS-TTFET's performances in terms of bipolar current suppression capability and analog/RF characteristics.

Figure 12 shows the transfer characteristics of the GDS-TFET with different H_{spacer}. It can be seen that when the gate voltage is negatively biased, the larger the H_{spacer} is, the weaker the control ability of the gate electrode to the channel is, and the smaller the ambipolar tunneling current generated. However, if the H_{spacer} is larger than 4 nm, the gate control ability to the tunneling region (between the gate and the source) will also deteriorate as H_{spacer} increases, resulting in a decrease in the I_{ON}.

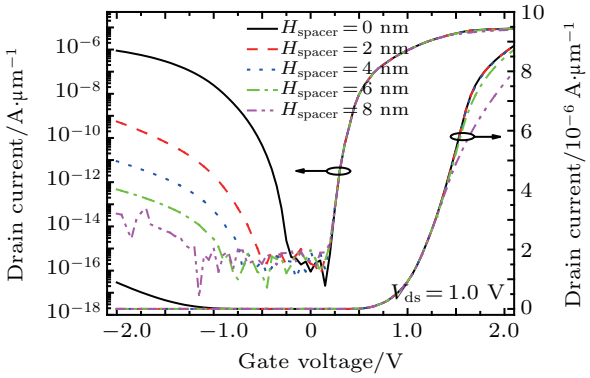


Fig. 12. Transfer characteristics for GDS-TTFET with different H_{spacer} at V_{ds} = 1.0 V.

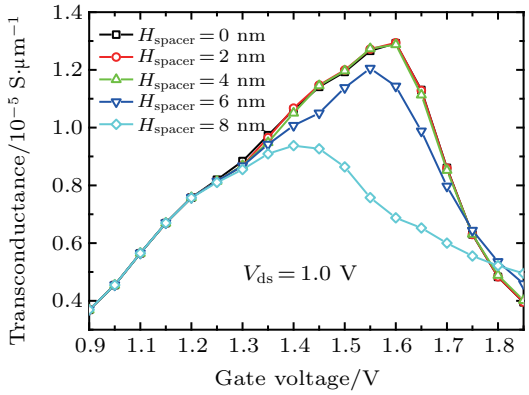


Fig. 13. Transconductance of the GDS-TTFET with different H_{spacer} at V_{ds} = 1.0 V when V_{gs} is biased from 1.0 V to 2.0 V.

To further investigate the impact of H_{spacer} on the GDS-TTFET's on-current I_{ON}, figure 13 shows the effect of H_{spacer} on the transconductance of GDS-TTFET when V_{gs} is biased from 1.0 V to 2.0 V. It can be seen that when H_{spacer} is less than 4 nm, the GDS structure has almost no influence on the transconductance of the GDS-TTFET. However, when H_{spacer} is larger than 6 nm, the transconductance of the GDS-TFET is significantly reduced. Also, as shown in Fig. 14, larger H_{spacer} means smaller gate-source and gate-drain parasitic capacitances, which is beneficial to improve the analog/RF characteristics of the GDS-TTFET.

In order to comprehensively analyze the influence of H_{spacer} on the analog/RF performance of the GDS-TTFET, the effects of H_{spacer} on the cutoff-frequency f_T and the gain bandwidth product (GBP) of the GDS-TTFET are shown in Figs. 15 and 16, respectively.

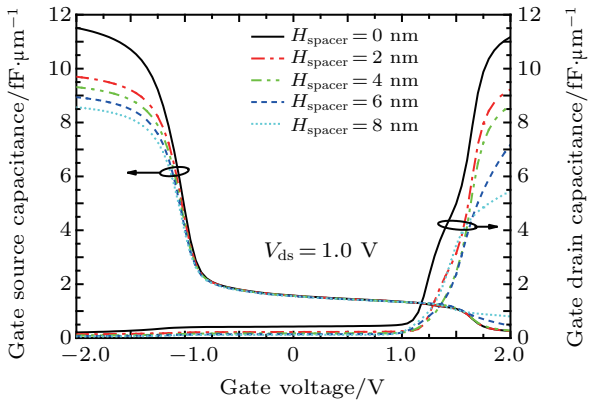


Fig. 14. Gate-source and gate-drain parasitic capacitance versus gate voltage for GDS-TTFET with different H_{spacer} at V_{ds} = 1.0 V.

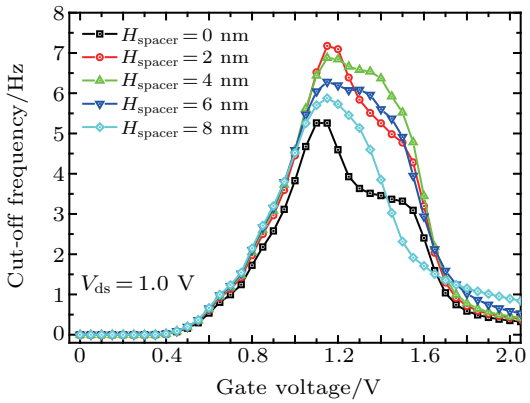


Fig. 15. Cut-off frequency for the GDS-TTFET with different H_{spacer} at V_{ds} = 1.0 V.

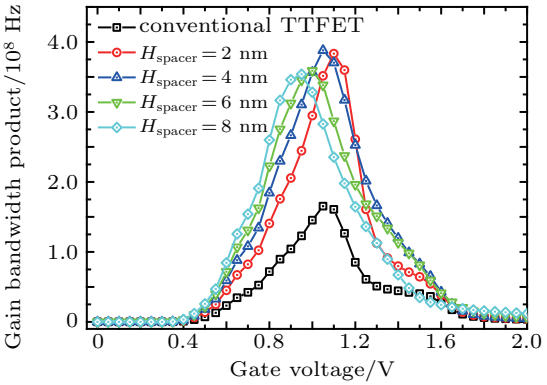


Fig. 16. Gain bandwidth product (GBP) for the GDS-TTFET with different H_{spacer} at V_{ds} = 1.0 V.

It can be seen from Fig. 15 that the GDS structure has a significant improvement on the cutoff frequency characteristics of the GDS-TTFET. Especially, when H_{spacer} is equal to 4 nm, the cutoff frequency f_T of the GDS-TTFET can obtain a higher peak value around 7×10^8 Hz, and this peak value can be maintained over a wider V_{gs} bias range. However, when H_{spacer} is increased to 6 nm, the cutoff frequency characteristic of the GDS-TTFET starts to degrade, both the cutoff frequency

peak value and the V_{gs} bias range with high cutoff frequency will decrease.

Same variation tendencies of gain bandwidth product (GBP) can be found in Fig. 16, when H_{spacer} is equal to 4 nm, the peak value of the GBP is the highest, but when H_{spacer} is further increased, the peak value of the GPB will decrease gradually.

Therefore, it is necessary to optimize the H_{spacer} of the GDS-TTFET. By selecting the appropriate H_{spacer}, the GDS-TTFET can effectively suppress the bipolar current and reduce the gate-drain parasitic capacitance while keeping the I_{ON} unaffected, thus obtaining the best analog/RF performance.

4. Conclusion

To better suppress the ambipolar current under a broader bias range while reducing the gate-drain and gate-source parasitic capacitances, a new T-shaped TFET (TTFET) with gate dielectric spacer (GDS) structure is proposed in this paper. I_{ds}–V_{gs} characteristics analysis shows that by inserting a low-κ gate dielectric spacer between the gate electrode and the gate dielectric, the ambipolar current of the TTFET can be drastically reduced. According to the energy band diagrams both in directions parallel and perpendicular to the channel, GDS-TTFET has the widest tunneling barrier, which results in the smallest BTBT generation and lowest ambipolar tunneling current. Further, analog/RF performance of GDS-TTFET are investigated regarding parasitic capacitance, cutoff frequency and gain bandwidth production. Simulation results show that due to the reduced value of total capacitance, GDD-TTFET has the highest amounts of cutoff frequency and gain bandwidth production as compared with conventional TTFET and GDO-TTFET. Finally, according to our simulations, the thickness of the gate dielectric spacer $H_{spacer} = 4$ nm is the best option for ambipolar current suppression and analog/RF performance improvement. The theoretical simulation results of this paper not only provide insights for understanding the physical mechanism of the TTFET, but also have theoretical guiding significance for designing and optimizing TTFET devices in the future.

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