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Investigation and active suppression of self-heating induced degradation in amorphous InGaZnO thin film transistors*

Dong Zhang(张东)[1], Chenfei Wu(武辰飞)[1], Weizong Xu(徐尉宗)[1,†], Fangfang Ren(任芳芳)[1], Dong Zhou(周东)[1], Peng Yu(于芃)[2], Rong Zhang(张荣)[1], Youdou Zheng(郑有炓)[1], and Hai Lu(陆海)[1,‡]

[1] *School of Electronic Science and Engineering, Jiangsu Provincial Key Laboratory of Advanced Photonic and Electronic Materials, Nanjing University, Nanjing* 210093, *China*

[2] *State Grid Shandong Electric Power Research Institute, Jinan* 250001, *China*

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Self-heating effect in amorphous InGaZnO thin-film transistors remains a critical issue that degrades device performance and stability, hindering their wider applications. In this work, pulsed current–voltage analysis has been applied to explore the physics origin of self-heating induced degradation, where Joule heat is shortly accumulated by drain current and dissipated in repeated time cycles as a function of gate bias. Enhanced positive threshold voltage shift is observed at reduced heat dissipation time, higher drain current, and increased gate width. A physical picture of Joule heating assisted charge trapping process has been proposed and then verified with pulsed negative gate bias stressing scheme, which could evidently counteract the self-heating effect through the electric-field assisted detrapping process. As a result, this pulsed gate bias scheme with negative quiescent voltage could be used as a possible way to actively suppress self-heating related device degradation.

Keywords: amorphous InGaZnO thin-film transistor, self-heating effect, threshold voltage shift, pulsed negative gate bias

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1. Introduction

Transparent oxide-based thin-film transistors (TFTs), such as amorphous InGaZnO (α-IGZO) TFTs, have shown considerable potential for applications in flat, flexible, and transparent display devices, benefiting from their advantageous properties like high mobility, excellent uniformity, low processing temperature, and high optical transparency.[1–5] As a result, they have been practically used as pixel switches and current drivers in active-matrix liquid crystal displays (AMLCDs) and active-matrix organic light-emitting diodes (AMOLEDs).[6,7] However, reliability remains a critical issue in α-IGZO TFTs, especially for applications under bias stress, light illumination, or other extreme working conditions.[8–10] As has been reported in previous studies, channel current under gate and drain bias operation would generate Joule heating in devices and produce a particularly serious self-heating effect in α-IGZO TFTs, considering the low thermal conductivity of the α-IGZO channel layer and the typically used glass substrate.[11–13] With the self-heating stress, electron trapping process would be intensified and hence cause a large impact on the devices on-and-off performance, e.g., shift of threshold voltage ($V_{\rm th}$).[11,12] Therefore, understanding and developing approaches to suppress the self-heating effect have highly important research and application significance, which is worthy of further investigation.[14,15]

In this work, reliability behaviors of α-IGZO TFTs have been studied by using specially designed pulsed current–voltage analysis. Transfer characteristics are measured to verify the self-heating effect in the fabricated α-IGZO TFTs. With variation of $V_{\rm th}$ shift at different applied gate bias waveform and channel width, the impact of the self-heating stress on devices stability is attributed to the Joule heating assisted charge trapping process. Moreover, pulsed negative gate bias has then been applied on devices to reduce the self-heating induced device degradation, with which $V_{\rm th}$ shift can be effectively suppressed.

2. Experiment

The α-IGZO TFTs tested in this work are fabricated on a heavily doped n-type silicon substrate, which serves as the back gate, as shown in Fig. 1(a). 200 nm of SiO_2 gate insulator is first deposited on top of the silicon substrate by plasma enhanced chemical vapor deposition (PECVD) at 350 °C (see Fig. 1(a)). Then, 50 nm α-IGZO active layer is grown on the SiO_2 layer with a direct-current (DC) type magnetron sputtering system at room temperature. The composition of the

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†Corresponding author. E-mail: wz.xu@nju.edu.cn

‡Corresponding author. E-mail: hailu@nju.edu.cn

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IGZO target used is $In_2O_3 : Ga_2O_3 : ZnO = 1 : 1 : 1$ in mole ratio, while the oxygen content of the Ar/O_2 mixture gas is maintained at 15% during the sputtering. Subsequently, source/drain electrodes composed of Ti/Au (30 nm/70 nm) bilayer are produced with the standard lithography process and e-beam evaporation technique. Then, Ti/Au (30 nm/70 nm) is deposited on the back-side of the highly conductive Si substrate as the metal conducting layer. Finally, the devices are subjected to thermal annealing at 250 °C in air for 1 h.[16,17] Two kinds of device dimensions have been prepared, with channel width/length (W/L) of 25 μm, 200 μm/5 μm. Here, V_{th} is defined as the gate voltage when the normalized drain current ($NI_D = I_D \times L/W$) reaches 1 nA.[12,13,18] The field effective mobility (μ_{EF}) in the saturation region is extracted by the normal method of the square root I_D versus V_G plot.[19] The α-IGZO TFTs with $W = 200$ μm are determined to have 0.96 V in V_{th} and 16.05 $cm^2/(V{\cdot}s)$ in μ_{EF} while the devices with $W = 25$ μm have 1.16 V in V_{th} and 15.06 $cm^2/(V{\cdot}s)$ in μ_{EF}, respectively.

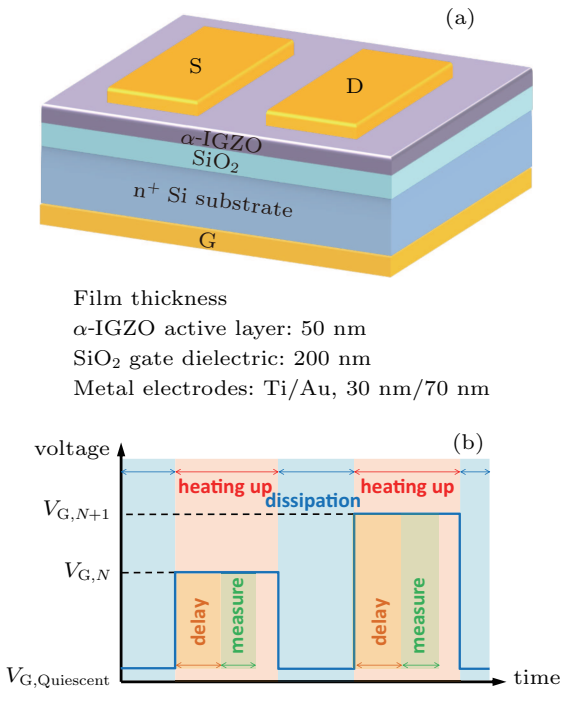


Fig. 1. (a) Structure of α-IGZO TFT fabricated on n^+ Si substrate; (b) waveform of the pulsed gate bias applied in the pulsed I_D–V_G measurement.

After device fabrication, pulsed I_D–V_G measurements are performed considering the practical environment of α-IGZO TFTs in switching applications. Figure 1(b) shows the waveform of the pulsed gate bias applied in the pulsed I_D–V_G (drain current versus gate voltage) measurement. At the first stage, the device is stressed at the quiescent voltage (V_{quies}) for a certain time (t_{quies}). Given $V_{quies} = 0$ V here, the enhancement mode α-IGZO TFTs will be at off-state with no channel current. Then, the gate voltage is pulsed from V_{quies} to gate voltage ($V_{G,N}$) for I_D measurement.[20] Here, N stands for the sequential number of measurement steps. The output current I_D is evaluated at the time of 100 ms (delay time) from the rise edge of the measurement pulse. When $V_{G,N}$ is higher than the threshold voltage, i.e., large enough to turn on the channel, heat would accumulate in the channel with on-state drain current. While, with V_{quies} bias, heat would dissipate since the channel is at off-state. As a result, varied t_{quies} corresponds to different heat dissipation time. All measurements have been conducted in a dark environment.

3. Results and discussion

Figure 2(a) shows the transfer curves of α-IGZO TFTs with various t_{quies} at $V_D = 20$ V, $W/L = 200$ μm/5 μm. During such measurements, the devices are stressed at $V_{quies} = 0$ V for different quiescent time (0 ms, 100 ms, 200 ms, 500 ms, 1000 ms, 2000 ms) and then measured at each $V_{G,N}$, obtaining transfer curves from pulsed I_D–V_G measurements. As illustrated in Fig. 2(b), the devices with $W = 25$ μm exhibit positive threshold voltage shift with reduced quiescent time, reaching ~ 0.6 V at zero dissipation time. These findings correspond very well with the previous relevant reports,[11–13] attributing the threshold voltage shift to charge trapping in oxides assisted by self-heating stress induced Joule heating, which would seriously degrade the devices performance and stability. Thus, reduced quiescent time, i.e., less heat dissipation time, would cause larger V_{th} shift. It should be additionally noted that, almost the same subthreshold swing (~ 0.32 V/dec) and on-state current have been obtained from the transfer curves with different heat dissipation time, which reveals the negligible degradation of carrier mobility and subthreshold swing. Thus, there should be no additional trapping states in α-IGZO TFTs induced by self-heating, which suggests the possible recoverability of the device degradation.[11]

Further pulsed transfer measurement reveals the strong dependence of V_{th} shift on the gate width (see Fig. 2(b)). When compared to the devices with $W = 25$ μm (V_{th} shift ~ 0.6 V), IGZO TFTs with $W = 200$ μm exhibit larger threshold voltage shift (~ 1 V) with the same heat dissipation time. Thus, it verifies that the devices degradation is indeed dominated by the self-heating effect, instead of the gate-stress effect or hot-carrier injection effect, both of which theoretically should be insensitive to the channel width.[11,21] For the self-heating effect, larger channel width makes dissipation of Joule heating more difficult, especially for heat generated within the central region of the channel.[22] This could well explain the results shown in Fig. 2(b), i.e., the self-heating effect issue is more serious in devices with wider channels.[12,18] Additionally, it could be observed from Fig. 2(b) that V_{th} shift becomes much smaller with increased t_{quies}, demonstrating the recoverability of the self-heating induced charge trapping process, while

larger gate width needs longer heat dissipation time, 500 ms and 2000 ms for channel widths of 25 μm and 200 μm, respectively.

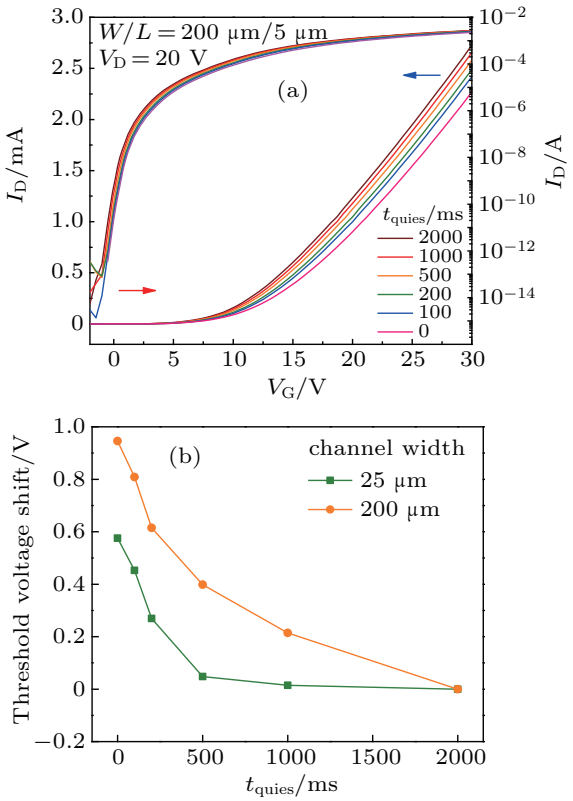


Fig. 2. (a) Transfer curves of α-IGZO TFTs with various quiescent state time t_{quies} at $V_D = 20$ V, $V_{quies} = 0$ V, and $W/L = 200$ μm/5 μm. (b) Derived threshold voltage shift versus t_{quies} with different channel widths of 25 μm (green) and 200 μm (orange).

For a detailed understanding of this degradation, different drain bias has been applied to investigate the dependence of the self-heating effect on the channel current. Figures 3(a) and 3(b) additionally illustrate the transfer curves of α-IGZO TFTs at $V_D = 10$ V and 30 V, respectively. It could be noted that larger threshold voltage shift can be observed with higher drain voltage, as directly shown in Fig. 3(c) with the threshold voltage shift curved as a function of t_{quies} at different V_D (30 V, 20 V, 10 V). That is, larger drain bias induces higher channel current, accumulating more Joule heat within the channel, and as a result more electrons could be activated and trapped into defect states, resulting in more serious V_{th} shift.

Based on the above analysis, the existence of the self-heating effect has been verified with pulsed I_D–V_G measurements with varying pulse intervals as well as transfer characteristics with different channel widths. Charge trapping process assisted by Joule heat has been recognized as the dominant factor for α-IGZO TFT degradation under self-heating stress.[11–13,22] Thus, to enhance heat dissipation or to reduce charge trapping should be both effective to suppress the self-heating effect. Although heat dissipation shows large dependence on the gate width (see Fig. 2(b)), it is infeasible for barely developing heat dissipation technique in α-IGZO TFTs by varying the device geometry. Therefore, electrical-bias based active suppression of charge trapping process is worthy of investigation.

The inset of Fig. 4 illustrates the proposed active self-heating suppression method, utilizing pulsed gate bias with negative V_{quies}. Correspondingly, transfer curves have been recorded and shown in Fig. 4 with various V_{quies} under the condition of $V_D = 30$ V and $t_{quies} = 200$ ms. It can be observed that, V_{th} shift has been apparently mitigated with large negative gate quiescent bias, and tends to be negligible with V_{quies} extending −15 V.

As shown in Fig. 5(a), continuously repeated measurements have been conducted on transfer properties to confirm the suppression effect on self-heating stress with $V_{quies} = -15$ V. Ideal repeatability of transfer curves has been observed with the almost same V_{th} (V_{th} shift < 40 mV) in Fig. 5(b), demonstrating the effectiveness of negative gate bias on counteracting self-heating stress induced degradation.

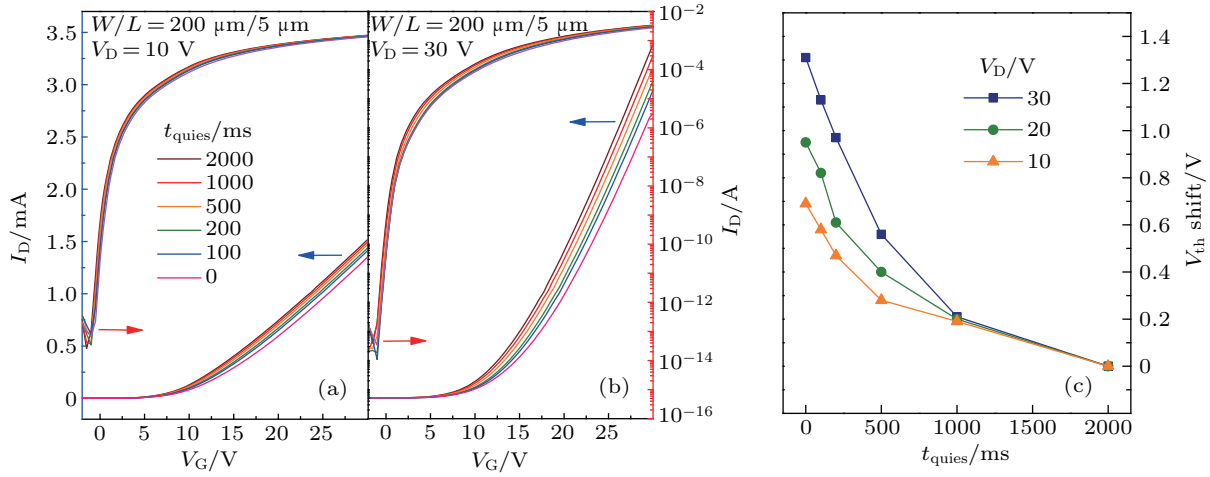


Fig. 3. Transfer curves of α-IGZO TFTs with various t_{quies} at (a) $V_D = 10$ V and (b) $V_D = 30$ V, while $V_{quies} = 0$ V, $W/L = 200$ μm/5 μm. (c) Derived threshold voltage shift versus t_{quies} with drain biases of 30 V (blue), 20 V (green), and 10 V (orange).

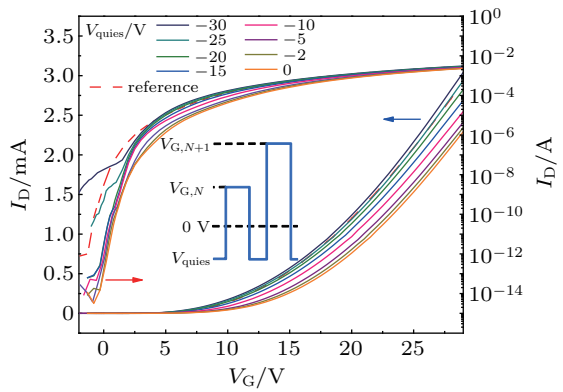


Fig. 4. Transfer curves of α-IGZO TFTs with various V_{quies} at V_D = 30 V and t_{quies} = 200 ms. The red dash line stands for transfer characteristics measured at t_{quies} = 2000 ms, where V_{th} shift could be taken as zero owing to enough heat dissipation time. The inset shows the pulsed negative gate bias stressing scheme.

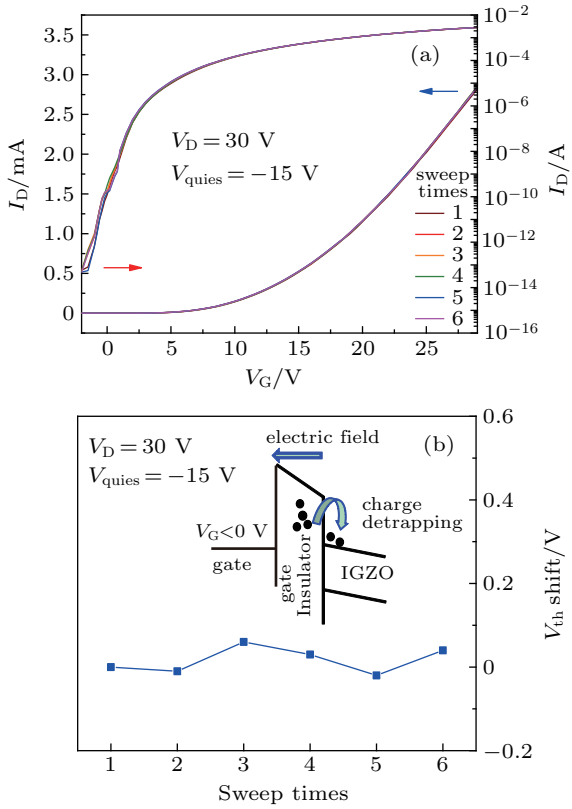


Fig. 5. (a) Transfer curves of α-IGZO TFTs obtained in continuously repeated measurements with V_D = 30 V and V_{quies} = −15 V. (b) Derived threshold voltage shift versus sweep times, the inset illustrates the electric field assisted charge detrapping process with negative quiescent gate bias.

The underlying mechanism could be well illustrated with the physical picture of charge detrapping process as suggested in the inset of Fig. 5(b).[23] During the pulse interval (with negative quiescent gate bias), vertical electric field under gate electrode is in the direction of channel to gate metal, which is the reverse direction to the charge trapping process. Hence, electrons trapped at the InGaZnO/SiO_2 interface or in bulk SiO_2 during on-state stage would get detrapped from the trap states with the assistance of the electric field, as indicated by the blue arrow in the inset of Fig. 5(b).[24] Ultimately, devices exhibit excellent stability, with remarkably suppressed V_{th} shift. Meanwhile, the effectiveness of pulsed negative gate bias stress on suppressing self-heating induced degradation also verifies the suggested charge trapping mechanism under self-heating stress.

4. Conclusion

We have investigated self-heating induced degradation in α-IGZO TFTs with pulsed I_D–V_G measurements. The large dependence of V_{th} shift on channel width demonstrates that device degradation is dominated by the self-heating effect instead of the hot-carrier effect or gate stress effect. Detailed investigations on V_{th} shift at various quiescent state times and drain currents have also revealed that, degradation of devices under self-heating stress should be attributed to the charge trapping process assisted by Joule heat, aggravated by limited heat dissipation ability. Pulsed negative gate bias based active suppression method on self-heating effect has then been proposed. With negative quiescent voltage of gate pulse (V_{quies} < −15 V), devices show evidently suppressed V_{th} shift owing to the electric field assisted detrapping process, which could be useful to reduce charge trapping related devices degradation.

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