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Heavy ion induced upset errors in 90-nm 64 Mb NOR-type floating-gate Flash memory*

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Upset errors in 90-nm 64 Mb NOR-type floating-gate Flash memory induced by accelerated ^{129}Xe and ^{209}Bi ions are investigated in detail. The linear energy transfer covers the range from 50 to 99.8 MeV/(mg/cm^2). When the memory chips are powered off during heavy ions irradiation, single-event-latch-up and single-event-function-interruption are excluded, and only 0->1 upset errors in the memory array are observed. These error bit rates seem very difficult to achieve and cannot be simply recovered based on the power cycle. The number of error bits shows a strong dependence on the linear energy transfer (LET). Under room-temperature annealing conditions, the upset errors can be reduced by about two orders of magnitude using rewrite/reprogram operations, but they subsequently increase once again in a few minutes after the power cycle. High-temperature annealing can diminish almost all error bits, which are affected by the lower LET ^{129}Xe ions. The percolation path between the floating-gate (FG) and the substrate contributes to the radiation-induced leakage current, and has been identified as the root cause of the upset errors of the Flash memory array in this work.

Keywords: heavy ion, Flash memory, single event upset, annealing

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1. Introduction

Non-volatile memories are one of the key components in modern electronic devices with a wide range of applications including harsh environments such as military and space.[1] Flash memory, which consists of floating-gate (FG) MOSFETs, is the largest fraction of modern non-volatile memories. An FG MOSFET is basically a metal-oxide-semiconductor (MOS) transistor where a polysilicon layer (the so-called FG) is interposed between the transistor gate (which is now called the Control Gate, CG) and the substrate. Flash memory cell is programmed or erased by the charge stored into or discharged from the floating-gate, which shifts the threshold voltage of the MOSFET between normally off and on.[2] In this way, different logic values are represented and stored. There are two main categories of Flash memories, which are the NOR and NAND architectures. NAND memories are more often used as mass storage devices, while NOR memories are usually utilized to store codes.[3]

Radiation effects, such as total ionizing dose (TID) and single event effect (SEE), have been identified as the major causes of component malfunction for spacecraft in a space radiation environment.[4–6] Thus, for space-grade electronic systems, it is crucial to characterize and understand the effects of radiation on Flash memories. TID causes a shift in the threshold voltage of Flash memory cells and may subsequently change the program state to the erase state.[7–9] SEE may also adversely affect the page buffer circuit (mainly SRAM) directly or induce SEFI in the peripheral circuit. These are soft errors and can be simply recovered by power cycles.

The Flash memory cell has been continuously scaled down to increase memory density and capacity. On the other hand, the quantity of charge in the floating-gate has also gradually decreased, and consequently, this has exacerbated the radiation tolerance performance.[10–12] The shrinking of the tunnel oxide thickness obviously degrades the retention and endurance performance in radiation environments. Therefore, hard errors (not SEL) induced by heavy ions in the tunnel oxide, i.e., the upset error of transition from logic 0 to 1 that remains even after the power cycle, are the main challenges of mission-critical systems.

In this work, 90-nm 64 Mb NOR-Type floating-gate Flash memory was irradiated with ^{129}Xe and ^{209}Bi ions to observe the upset errors in the memory array. Heavy ions induce physical damage in the tunnel oxide, which serves as a leakage path for stored electrons in the FG. The quantity of upset errors is related to the (LET). Upset errors can be partially erased, but appear gradually after the program operation. Annealing has a great impact on the recovery of this type of errors.

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2. Irradiation experiments

2.1. Devices under test

The high-performance SPI (Serial-Peripheral-Interface) NOR-type floating-gate Flash devices were designed by our group and manufactured using commercial 90-nm technology. A cross-section transmission electron microscope (TEM) image of a floating-gate Flash cell is shown in Fig. 1. The chip size is 3.4 mm×2.5 mm. It is organized as 8M×8 with a single power supply voltage set between 2.7 V and 3.6 V. The logic diagram of the 64 Mb SPI NOR Flash is given in Fig. 2(a). The layout snapshot is demonstrated in Fig. 2(b). The Flash memory array is divided into two Big Blocks as BBLK0 and BBLK1. The Big Block is divided into 64 kb blocks, which are composed of 4 kb sectors. These devices operate in a temperature range from −55 °C to 125 °C and are available with an access time of 20 ns. They come with some standard control pins including chip select (/CS), write protect (/WP), and hold (/HOLD). The serial clock enters the SCLK pin, and the serial data input and output pins are SI and SO, respectively. Internally generated and regulated voltages are provided for the program and erase operations.

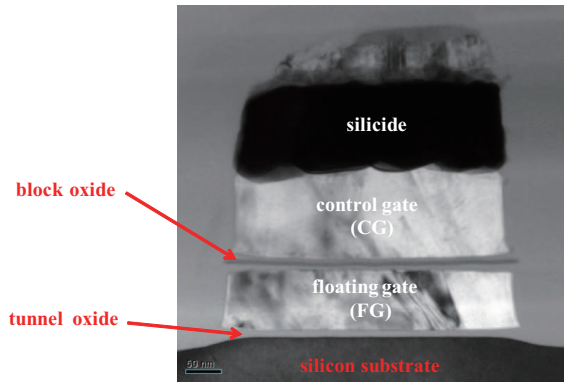


Fig. 1. (color online) Cross-section TEM of a floating-gate Flash cell fabricated in the 90-nm node.

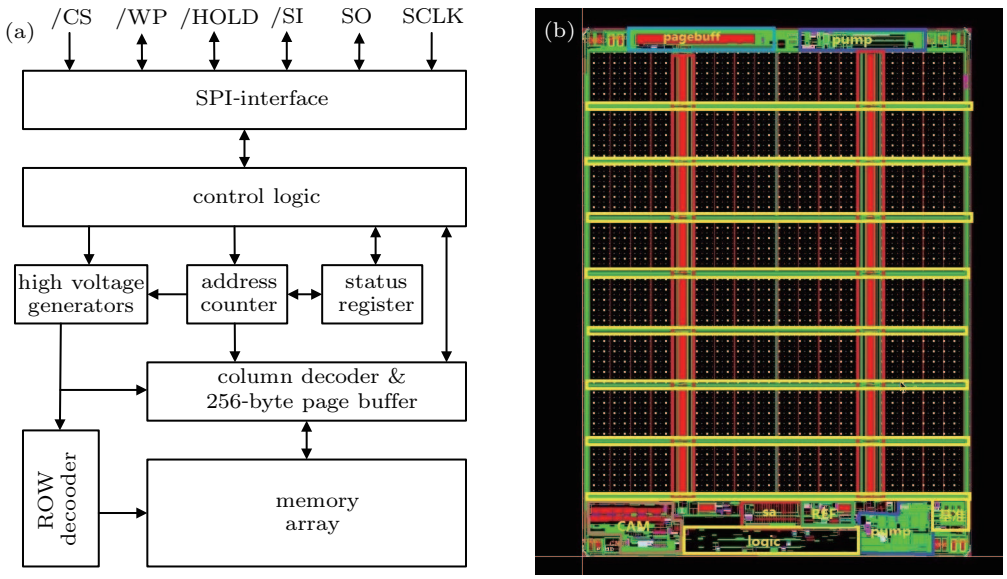


Fig. 2. (color online) (a) Logic diagram and (b) layout of 64 Mb SPI NOR Flash.

2.2. Heavy ion experimental setup

The heavy ion irradiation was carried out at the Heavy Ion Research Facility in Lanzhou (HIRFL) at the Institute of Modern Physics, Chinese Academy of Sciences with 19.5 MeV/u ^{129}Xe and 9.5 MeV/u ^{209}Bi ions (initial kinetic energy). Different LET values were tuned using aluminum degraders with different thicknesses. For the ^{129}Xe ions, the LET values in silicon are 50 and 57.5 MeV/(mg/cm^2), while the LET is 99.8 MeV/(mg/cm^2) for ^{209}Bi ions. The total fluence in this series of experiments was 10^7 ions/cm^2. The DUT is written with a data pattern 55 H and then kept powered off. Subsequently, the DUT with no bias is irradiated to a predefined fluence. During completion of the irradiation, the power-up is followed by a comparison operation. The whole chip is then erased and rewritten with 55 H, then read and comparison operations are performed.

3. Experimental results

After the DUT was irradiated by the ^{209}Bi ions with a LET of 99.8 MeV/(mg/cm^2) and fluence of 10^7 ions/cm^2, it was powered up and accessed to check the upset error bits in the memory array. The testing results are displayed in Fig. 3. As can be seen, there are 136189 error bits immediately after irradiation. After the whole chip was again erased and rewritten with 55 H, the number of errors decreased dramatically to 1600 bits. This suggests that some of the errors may be permanent and cannot be corrected by rewriting during a short time period at room temperature. The read operation

was again performed just 2 minutes after rewriting and the error bits increased up to 136834. It should be noted that all the upset errors were 0 to 1 transitions and they are caused by the radiation-induced leakage path between the storage floating gate and the substrate in the experiment, i.e., the tunnel oxide.

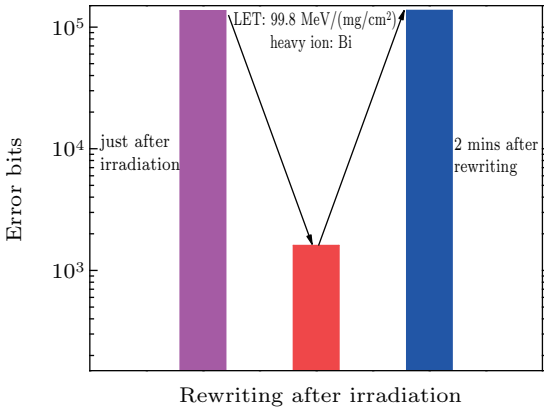


Fig. 3. (color online) Error bits after ^{209}Bi ions injection with different operations.

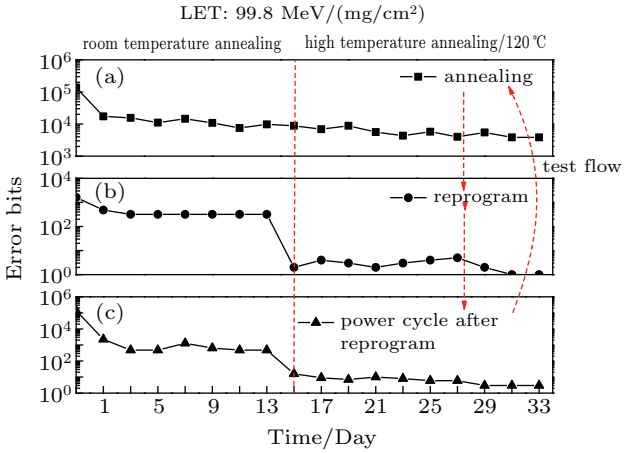


Fig. 4. (color online) Error bit change with annealing conditions after ^{209}Bi ions injection. (a) Annealing, (b) reprogramming, and (c) power cycle after reprogramming.

^{209}Bi ions induced upset errors which varied with respect to the annealing conditions, such as room-temperature annealing from day 1 to day 15 and 120 °C high-temperature annealing from day 15 to day 33 as shown in Fig. 4. The dashed red line illustrates the test sequence: read the DUT first immediately after completion of the annealing process, then rewrite the DUT and read the data, finally power up to check the data again (about 2 minutes later after reprogramming). The error bits on day 1 are consistent with the data in Fig. 3. The error bits just after annealing (the upper plot) decreased gradually with time. The number of errors is reduced greatly after the rewriting operation and then increased very slightly after the power cycle. However, for high-temperature annealing, the phenomenon is quite different. The error bits just after annealing (the upper plot) are further decreased to 3500 on day 33. There are almost no observed upset errors after reprogramming and power cycle operations (middle and lower plots). However, error bits reappear with a decreasing number after 2 days of high-temperature annealing.

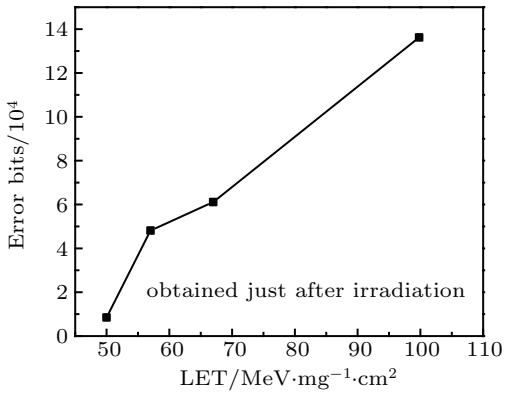


Fig. 5. The impact of LETs on error bits.

Figure 5 is a plot of the linear relationship between the error bits and LET from 50 to 99.8 MeV/(mg/cm^2). ^{129}Xe and ^{209}Bi ions are utilized here. The upset errors increased by more than two decades when the LET value doubles from 50 to 99.8 MeV/(mg/cm^2). The annealing trends with different LET values are similar, as shown in Fig. 6. The error bits are relatively easy to remove in the case of the lower LET values such as 67.1 and 57.5 MeV/(mg/cm^2), even under room temperature annealing. After 120 °C high-temperature annealing is performed, the error bits with lower LET values are almost diminished, while there are still more than 3000 upset errors for the case of LET equal to 99.8 MeV/(mg/cm^2).

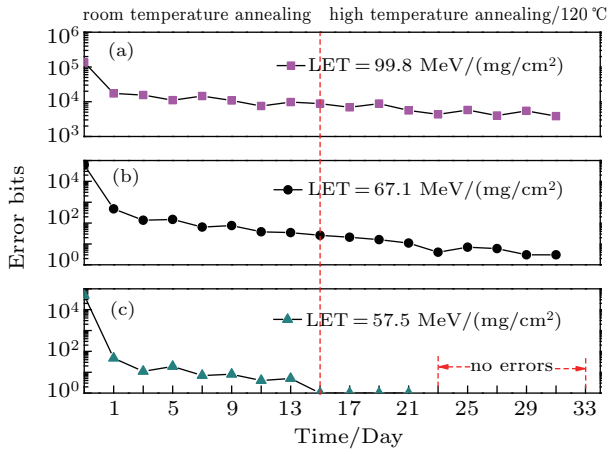


Fig. 6. (color online) Error bits with respect to LETs and annealing conditions. (a) LET = 99.8 MeV/(mg/cm^2), (b) LET = 67.1 MeV/(mg/cm^2), and (c) LET = 57.5 MeV/(mg/cm^2).

4. Discussions

The FG discharge after heavy ion irradiation is governed by two different mechanisms: a transient one and a long-term one. The transient mechanism occurs during or immediately

after ion penetration, assuming a transient leakage path is activated that discharges the FG,[13,14] or the carrier flux generated by the impinging radiation enables unbalanced tunneling and transitorily discharge the FG.[15] Although this may lead to single event effects such as SEU, this can be mitigated through appropriate ECC and redundancy techniques, and the bit errors can be effectively eliminated after a program operation. In contrast, the long-term effect cannot be easily addressed. A stable current-leakage path, known as a radiation-induced leakage current (RILC),[16] is created and this will cause a progressive discharge of the FG cell that cannot be repaired by rewrite operations. This long-term leakage phenomenon is observed in our experiments.

The oxide-nitride-oxide (ONO) block oxide separating FG and CG is believed to avoid any significant leakage path due to the large thickness and the low tunneling probability of this layer.[17] Thus, stable leakage is assumed to take place in the tunnel oxide (SiO_2) between the FG and the silicon substrate, as shown in Fig. 7. When a heavy ion with a high LET penetrates the SiO_2 layers, it loses energy and generates electron/hole pairs that are condensed in a cylinder with a diameter of several nanometers. Among these generated charge carriers, only about 1% can survive while the other 99% recombine according to the columnar recombination model.[18] The recombination process releases energy in the form of phonons or photons and results in physical damage along the ion track, which acts as charge trap centers. These charge trap centers partly trap the holes that survive the recombination and form electrically active defects (EADs) at the Si/SiO_2 interface,[19] or in the oxide bulk aligned in the direction normal to the oxide layer.[20] With the assistance of the EADs, a percolation path between the FG and the substrate is formed as the basic contributor to the RILC. The RILC further leads to a continuous discharge of the programmed FG cell and finally, to a bit error with the progression of time.

In MOS technologies which exploit the very thin ($<$ 6 nm) SiO_2 layer, RILC can be dominated by the single trap-assisted tunneling (s-TAT) mechanism.[9] Several conductive paths may exist in the oxide, but each one is formed by a single EAD. In FG Flash memories, however, the thickness of the tunneling oxide is normally approximately 10 nm, and this "single EAD" form of RILC is too small to discharge an FG cell because of the low tunneling probability. To build a conductive path that can discharge an FG cell, more than one EAD working together is needed. This is known as the multi-trap-assisted tunneling (m-TAT) mechanism[21,22] which is represented in Figs. 7(c) and 8.

This m-TAT leakage path can be efficient. In Fig. 3, we show that the RILC induced by ^{209}Bi irradiation discharges a programmed FG cell quite rapidly (within 2 minutes). Since the distribution of the EADs has a statistical property, not all the FGs bombarded by ions suffer from a RILC. In fact, only approximately 0.3% of the memory cells in our 64 Mb Flash experienced bit errors after the ^{209}Bi irradiation with a fluence up to $1 \times 10^7/\text{cm}^2$.

The LET of the impinging ion plays an important role in the formation of the RILC. Higher LET ions generate denser electron-hole tracks where the recombination process is significantly more efficient. Thus, more energy is released to create more physical damage and more EADs. Therefore, the higher the LET of the impinging ion, the more severe the impact of the RILC on the FG Flash cells.

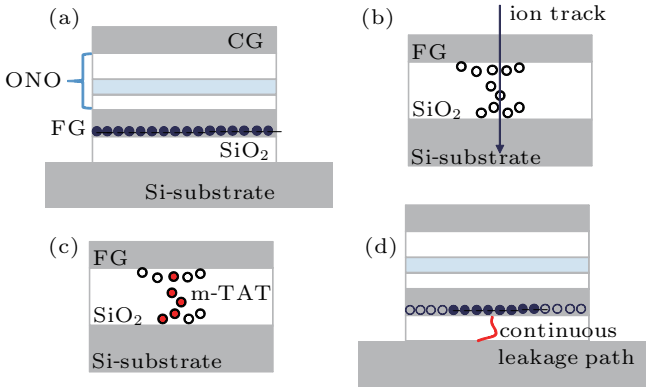


Fig. 7. (color online) Radiation-induced conductive path in the tunneling oxide of the FG cell. (a) FG cell after programming. (b) Impinging heavy ion creates physical damage in the tunneling oxide. Electrons stored in the FG are not shown. (c) Holes are trapped to form electrically active defects (EADs). RILC occurs with the help of EADs, through the multi-trap-assisted tunneling (m-TAT) mechanism. Electrons stored in the FG are not shown. (d) RILC progressively discharges the programmed FG cell.

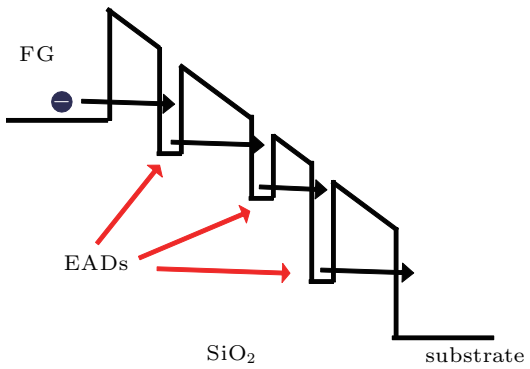


Fig. 8. (color online) Schematic representation of the multi-trap-assisted tunneling mechanism involving several electrically active defects (EADs).

5. Conclusion

This work describes ^{129}Xe and ^{209}Bi ions induced upset errors in 90-nm 64 Mb NOR-type floating-gate Flash memory. Only 0 to 1 transition error has been observed, which show a strong dependence on LET, annealing temperature, and operations. The underlying physical mechanisms are discussed in detail. This work is useful in the development of radiation-tolerant Flash memories aiming at space applications.

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