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Characteristics and threshold voltage model of GaN-based FinFET with recessed gate*

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In this work, AlGaN/GaN FinFETs with different fin widths have been successfully fabricated, and the recessed-gate FinFETs are fabricated for comparison. The recessed-gate FinFETs exhibit higher transconductance value and positive shift of threshold voltage. Moreover, with the fin width of the recessed-gate FinFETs increasing, the variations of both threshold voltage and the transconductance increase. Next, transfer characteristics of the recessed-gate FinFETs with different fin widths and recessed-gate depths are simulated by Silvaco software. The relationship between the threshold voltage and the AlGaN layer thickness has been investigated. The simulation results indicate that the slope of threshold voltage variation reduces with the fin width decreasing. Finally, a simplified threshold voltage model for recessed-gate FinFET is established, which agrees with both the experimental results and simulation results.

Keywords: AlGaN/GaN, FinFET, recessed gate, threshold voltage

PACS: 73.61.Ey, 52.77.Bn, 73.40.Qv **DOI:** 10.1088/1674-1056/27/9/097308

1. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) are considered to be the most promising candidate for power electronics devices and switch applications due to their superior material properties, such as high critical electric field, high saturation velocity, large bandgap, and temperature stability.[1,2] FinFET has a three-dimensional (3D) gate electrode structure, which can control the two-dimensional electron gas (2DEG) from three directions of the channel, so that the short channel effect of AlGaN/GaN HEMTs can be suppressed.[3] Meanwhile, better transconductance can be obtained by FinFET structure.[4] Moreover, the GaN-based FinFET device with narrow fin width can achieve the positive threshold voltage for enhancement-mode device applications.[5] It is also known that the recessed-gate technique has been paid great attention to achieve higher transconductance and positive threshold voltage for enhancement-mode device.[6,7] However, few papers have reported recessed-gate FinFETs based on AlGaN/GaN, and the relationship between the threshold voltage and the AlGaN layer thickness with different fin widths has also not been discussed at present.

In this work, the fabrication and characterization of GaN-based recessed-gate FinFETs with varying fin widths are reported. The current and transconductance characteristics of the device with different fin widths of 100 nm, 120 nm, 140 nm, and 160 nm are investigated, respectively. Then the transfer characteristics of the recessed-gate with different fin widths and varying recessed-gate depths are simulated by Silvaco software, and the relationship between the threshold voltage and the AlGaN layer thickness is investigated in detail. A new simplified threshold voltage model has been built for recessed-gate FinFET.

2. Growth and device fabrication

AlGaN/GaN heterostructures were grown on sapphire substrates by metal organic chemical vapor deposition. The conventional HEMT epitaxial structure consists of a low-temperature GaN nucleation layer, a 2 μm-thick unintentionally doped GaN buffer layer, and a 26 nm-thick un-doped AlGaN barrier layer. An electron sheet density of 9.2×10^{12} cm^{-2} and an electron mobility of 1650 cm^2/Vs were obtained by room temperature Hall measurements. The fabrication process began with the device mesa, and the mesa was formed by using Cl_2 plasma dry etching in an inductively coupled plasma (ICP) system. The Ohmic contacts were formed by Ti/Al/Ni/Au evaporation followed a thermal annealing at 830 °C for 30 s. Then the wafer was split into two pieces, one for the fabrication of FinFET device and the nanowire channel using electron beam lithography, where the nanowire channel was performed by using Cl_2 plasma dry etching in ICP system with 10 W bias power, and the other for the fabrication of conventional HEMT device for comparison. The fin

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width ranged from 100 nm to 160 nm, and the fin height was 70 nm. Recessed-gate etching was performed on the AlGaN barrier layer of devices in ICP system with 7 W bias power, and the etch depth is 5 nm. A 60 nm-thick SiN was deposited by plasma enhanced chemical vapor deposition (PECVD). The SiN in the gate region was etched by ICP system. The Ni/Au (30 nm/200 nm) E-beam evaporation and lift-off were carried out to form the gate electrode. Schematic of the AlGaN/GaN FinFETs is shown in Fig. 1(a). The devices feature a gate width of 50 μm, a gate length of 0.5 μm, and a source–drain space of 4 μm. The nano-channel of the device is observed by scanning electron microscopy (SEM), shown in Fig. 1(b).

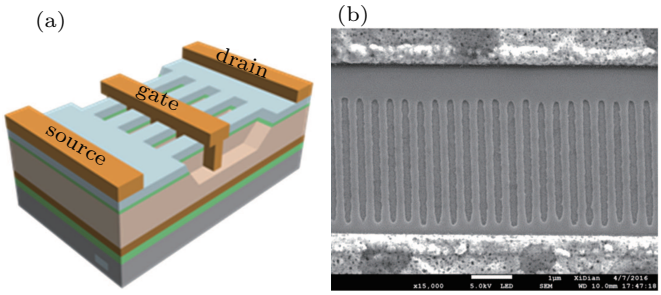


Fig. 1. (color online) (a) 3D schematic of AlGaN/GaN FinFETs. (b) SEM cross-sectional nanowire channel image of FinFETs.

3. Experimental results and discussion

Figure 2(a) shows the transfer characteristics of conventional devices (C-HEMT) and FinFET devices with different fin widths ($V_{DS} = 10$ V). The results show that the threshold voltage of the FinFET devices is shifted positively compared to that of the conventional device. With the fin width decreasing, there is an obvious shift of threshold voltage along the positive direction. It is because the side gate Schottky contact of the FinEFT device has a depletion effect on the channel, so that the 2DEG concentration is reduced.[8] As the fin width decreases, the ratio of the depletion layer width to the total channel width becomes larger and the threshold voltage is further shifted positively.[9]

It can be seen that the saturation current of FinFETs with 160 nm are higher than that of conventional HEMT device at $V_G = 2$ V. The phenomenon mainly stems from the reduction of the source access resistance.[10] While the formation of AlGaN/GaN nano-fins only in the gate opening was reported, the source access region appears as a more ideal source access resistance and the saturation current increases obviously.[11] Transconductance characteristics curves are shown in Fig. 2(b). It can be seen that transconductance peaks of the 120 nm, 140 nm, and 160 nm FinFET devices are larger than the conventional HEMT, because the control ability of the gate to the channel carrier is enhanced by the tri-gate structure of FinFET. As the fin width decreases, the transconductance peak increases, but the transconductance peaks of 120 nm and 100 nm FinFETs devices is significantly reduced, which can be attributed to the influence of the etching damage on the gate sidewall, and the mobility of electrons in the channel is reduced obviously in narrow-fin-width devices. While tetramethylammonium hydroxide (TMAH) solution was used in sidewall wet etch and made damage-free sidewall surface of fin.[4]

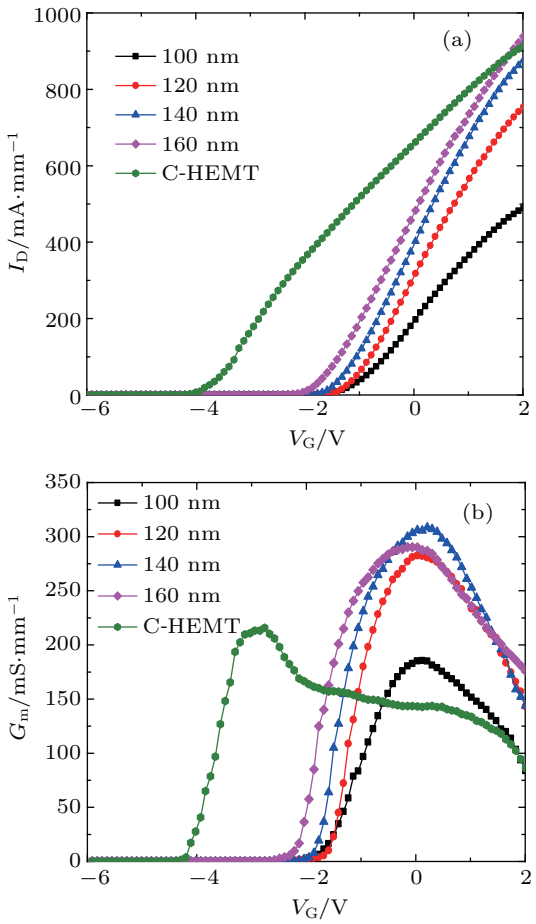


Fig. 2. (color online) (a) Transfer and (b) transconductance characteristics of C-HEMT and FinFETs at $V_{DS} = 10$ V ($W_{fin} = 100$, 120, 140, and 160 nm).

Figure 3 shows the DC characteristics of conventional HEMT and recessed-gate FinFETs, in which the etch depth of recessed gate is 5 nm. It can be seen that the threshold voltage values of both the conventional device and the FinFET device after the recessed-gate etching are shifted positively. The thickness of AlGaN barrier layer under the gate is reduced by recessed-gate etching process, so that the Schottky depletion is enhanced and the polarization effect of the heterojunction becomes weaker, which results in the decrease of the 2DEG concentration.[12] Therefore, the recessed-gate etching causes the device threshold voltage to shift positively. The threshold voltage variation and the specific transconductances change are presented in Table 1.

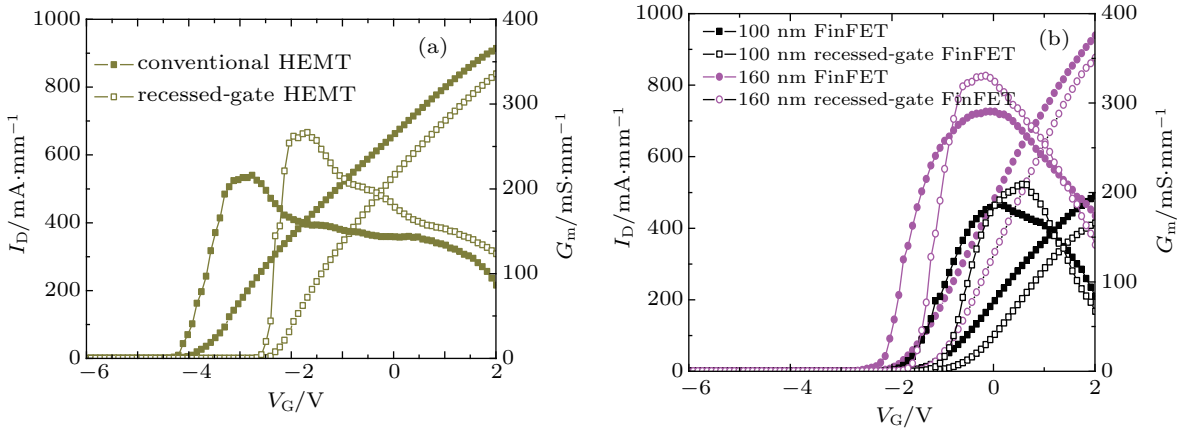


Fig. 3. (color online) DC characteristics of (a) C-HEMT and (b) FinFETs with recessed gate.

Table 1. Threshold voltage and transconductance of C-HEMT and recessed-gate FinFETs.

Samples	V_{th}/V			G_m/mS·mm^{-1}		
	Non-recessed	Recessed	Variation	Non-recessed	Recessed	Variation
100 nm FinFET	–1.12	–0.56	+0.56	187	209	+22
120 nm FinFET	–1.20	–0.57	+0.63	283	313	+30
140 nm FinFET	–1.38	–0.72	+0.66	305	338	+33
160 nm FinFET	–1.75	–1.07	+0.68	290	330	+40
C-HEMT	–3.8	–2.36	+1.44	213	266	+53

With the fin width increasing, both the variation of threshold voltage and the transconductance after recessed-gate etching increase. FinFET has triple gate electrode structure, including a top gate and two side gates, with depletion occurring in both lateral and vertical directions. After recessed-gate etching, the threshold voltage of device shifts positively and the transconductance increases. As the fin width decreases, the depletion effect of the side gate of the FinEFT device has been enhanced, which results in a lower contribution of the top gate to the channel after recessed-gate etching. Therefore, the larger the fin width is, the greater the improvement of transconductance and positive shift of the threshold voltage are after recessed-gate etching.

4. Simulation and modeling

Simulation software Silvaco is used to investigate the effect of fin width and recessed depth on the characteristics of FinFETs. Transfer characteristics of the recessed-gate FinFETs with different fin widths at $V_{DS} = 10$ V are depicted in Fig. 4, where the etch depth is 5 nm. Compared to the experimental results, the simulation results agree with the transfer characteristic of the recessed-gate with different fin widths. It is found that the saturation current of the 100 nm FinFET at $V_G = 2$ V is much lower than simulation results, which can be attributed to the etching damage of the gate sidewall.

In the experiment, the nanowire channel was performed by using Cl_2 plasma dry etching in ICP system with 10 W bias power, and the recessed-gate etching was performed on the AlGaN barrier layer of devices in ICP system with 7 W bias power. The depth of the etched nanowire channel is deeper and the etching is performed at a relative high power, so the etching rate is fast, the depth of the recessed-gate is shallow, lower power etching is conducted, and the rate etching is slow with low etching damage. Moreover, the shallow recessed depth of 5 nm under the gate could avoid the impact of severe etching damage on channel mobility, and the saturation current is determined by electron mobility and the 2DEG density in specific device structure.[13] Therefore, the recessed-gate etching damage does not show significant behavior, i.e., the reduction in saturation current is not significant.

Figure 5 shows the transfer characteristics of FinFETs with different recessed-gate depths. The recessed-gate depths are set to 0 nm, 5 nm, 10 nm, 15 nm, 20 nm, 25 nm, 27 nm, and 27.5 nm, respectively. It is indicated that the increase of recessed-gate depth is accompanied with the positive shift of threshold voltage. The AlGaN barrier layer thickness under the gate reduced, i.e., the distance between the top gate and channel is reduced, and then the depletion of gate Schottky contact is enhanced. Meanwhile, the polarization effect of the heterojunction has been weakened, which results in the decrease of the 2DEG concentration. In addition, when the AlGaN thickness is reduced to a certain thickness, the GaN conduction band at the heterojunction interface is already above the Fermi level or upward completely, which indicates that the 2DEG at the heterojunction interface has been depleted without gate voltage application, so that the device presents enhancement mode features. It can be seen from Fig. 5(a) that the 100 nm FinFET with 20 nm recessed depth has positive

threshold voltages of +0.04 V, which indicates that the channel has been completely pinched off. Similar to 100 nm FinFET, the 160 nm FinFET with 25 nm recessed depth exhibits threshold voltages of +0.28 V, as shown in Fig. 5(b), due to the increase of fin width, and the depletion effect of the side gate to the channel becomes weaker.

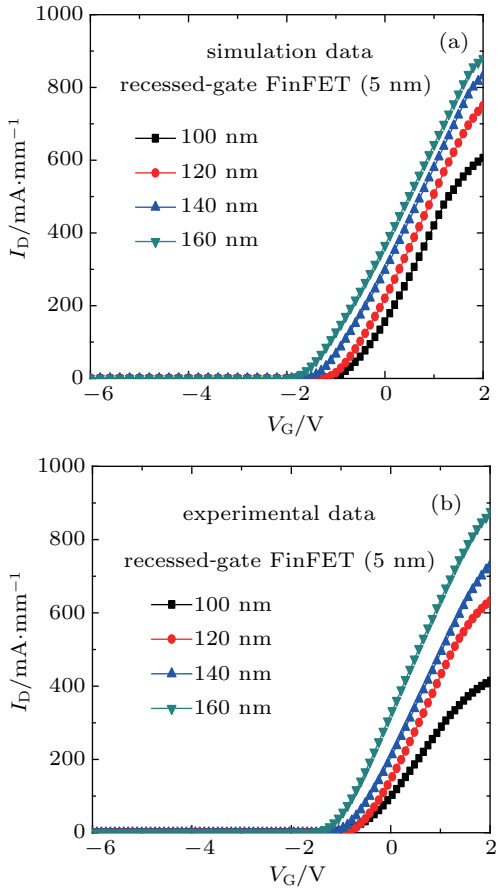


Fig. 4. (color online) Transfer characteristics of recessed-gate FinFETs at $V_{DS} = 10$ V ($W_{fin} = 100$, 120, 140, and 160 nm): (a) simulation data and (b) experimental data.

Saito *et al.*[14] reported that the relationship between the threshold voltage and the recessed AlGaN layer thickness of AlGaN/GaN HEMT, that is,

$$V_{th} = 2\Phi_B - \frac{\Delta E_C}{e} - \frac{qN_{2D}}{\varepsilon} t_{RA}, \tag{1}$$

where $e\Phi_B$ is the Schottky barrier height, N_{2D} is the 2DEG density at the non-recessed region, ΔE_C is the conduction band discontinuity, t_{RA} is the AlGaN layer thickness under the gate, and ε is the dielectric constant for AlGaN layer. From Eq. (1), the relationship between V_{th} and t_{RA} of AlGaN/GaN HEMT is linear. As shown in Fig. 6, it can be seen that the relationship between the threshold voltage and the AlGaN layer thickness of C-HEMT is linear, and the equation $V_{th} = 0.71 - 0.14 t_{RA}$ can be obtained by the extrapolation, which is good agreement with V_{th} expression. It also can be found that as the etch depth increases, the threshold voltage shifts positively and the slope of C-HEMT is the steepest, because its channel width is wider compared to FinFETs. Moreover, with the fin width increasing, the variation of threshold voltage after recessed-gate is increasing, which agrees with the experimental data in the Table 1.

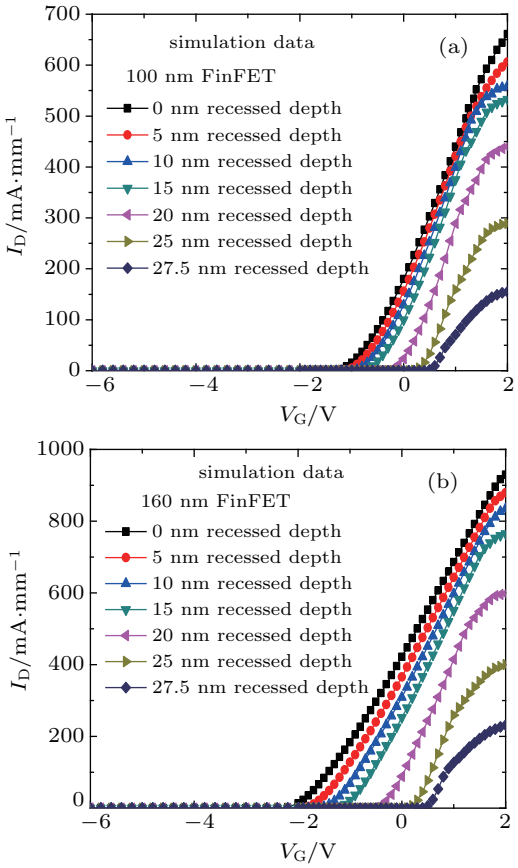


Fig. 5. (color online) Transfer characteristics of (a) 100 nm FinFET and (b) 160 nm FinFET with different recessed depths.

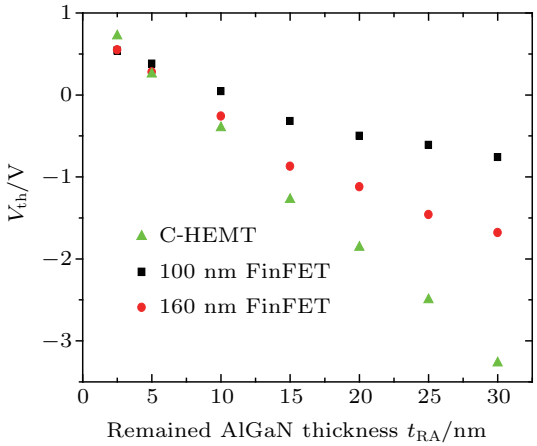


Fig. 6. (color online) Relation between the threshold voltage and the AlGaN layer thickness of C-HEMT and FinFETs ($W_{fin} = 100$ nm and 160 nm).

Taking into account the effect of side gate to the channel, the N_{2DR} of FinFET can be given by[9]

$$N_{2DR} = N_{2D}\left(\frac{W_{fin} - 2W_{Dep}}{W_{fin}} + \alpha\right), \tag{2}$$

where α is defined to determine the effect of fin height on electron concentration in FinFETs, and W_{Dep} is the width of depletion layer which formed by the sidewall of channel and gate metal. Equation (1) can be written as

$$V_{\mathrm{th}} = 2\Phi_{\mathrm{B}} - \frac{\Delta E_{\mathrm{C}}}{e} - \frac{qN_{2\mathrm{D}}}{\varepsilon}\left(\frac{W_{\mathrm{fin}} - 2W_{\mathrm{Dep}}}{W_{\mathrm{fin}}} + \alpha\right)t_{\mathrm{RA}}. \quad (3)$$

With the increase of fin width, the piezoelectric polarization effect of channel will be enhanced, which results in higher 2DEG concentration. Therefore, the polarization effect should be taken into consideration. A new simplified model of threshold voltage for recessed-gate FinFET is built as

$$\begin{aligned} V_{\mathrm{th}} = {} & 2\Phi_{\mathrm{B}} - \frac{\Delta E_{\mathrm{C}}}{e} - \left\{\frac{qN_{2\mathrm{D}}}{\varepsilon}\left(\frac{W_{\mathrm{fin}} - 2W_{\mathrm{Dep}}}{W_{\mathrm{fin}}} + \alpha\right)\right. \\ & - \frac{(\sigma + P_{\mathrm{PZ}}(\mathrm{AlGaN}))}{\varepsilon}\beta\left[1 + \exp\left(-\frac{W_{\mathrm{fin}}}{2\lambda}\right)\right] \\ & \left.\times \exp\left(-\frac{W_{\mathrm{fin}}}{\lambda}\right)\right\}t_{\mathrm{RA}}, \end{aligned} \quad (4)$$

where P_{PZ}(AlGaN) denotes piezoelectric polarization in AlGaN, σ is the total polarization charge density of C-HEMT, and β and λ are the fitting parameters.

For Eq. (4), when the fin height is a constant, it indicates that α is a constant. It can be seen that with the fin width increasing, $\frac{W_{\mathrm{fin}}-2W_{\mathrm{Dep}}}{W_{\mathrm{fin}}}$ increases and $\frac{qN_{2\mathrm{D}}}{\varepsilon}\left(\frac{W_{\mathrm{fin}}-2W_{\mathrm{Dep}}}{W_{\mathrm{fin}}} + \alpha\right)$ increases. While $\exp\left(-\frac{W_{\mathrm{fin}}}{2\lambda}\right)$ and $\exp\left(-\frac{W_{\mathrm{fin}}}{\lambda}\right)$ decreases and

$$\frac{(\sigma + P_{\mathrm{PZ}}(AlGaN))}{\varepsilon}\beta\left[1 + \exp\left(-\frac{W_{\mathrm{fin}}}{2\lambda}\right)\right]\exp\left(-\frac{W_{\mathrm{fin}}}{\lambda}\right)$$

decreases,

$$\begin{aligned} & \frac{qN_{2\mathrm{D}}}{\varepsilon}\left(\frac{W_{\mathrm{fin}} - 2W_{\mathrm{Dep}}}{W_{\mathrm{fin}}} + \alpha\right) - \frac{(\sigma + P_{\mathrm{PZ}}(\mathrm{AlGaN}))}{\varepsilon}\beta \\ & \times\left[1 + \exp\left(-\frac{W_{\mathrm{fin}}}{2\lambda}\right)\right]\exp\left(-\frac{W_{\mathrm{fin}}}{\lambda}\right) \end{aligned}$$

increases, which indicates that as the fin width increases, the slope of recessed-gate FinFETs increases, i.e., the trend of the curve becomes steeper and the variation of threshold voltage after recessed-gate etching increases. Model shows agreement with both the experimental results and simulation results.

5. Conclusion

The DC characteristics of the recessed-gate FinFET devices are analyzed. After the recessed-gate etching, both the conventional HEMT device and the FinFET devices show positively shifted threshold voltages and higher transconductance. Furthermore, it is also found that the variations of threshold voltage decrease with the fin width reducing. The transfer characteristics of the recessed-gate with different fin widths and recessed-gate depths are simulated by Silvaco software, and the simulation results agree well with the experiment results. Finally, a new simplified threshold voltage model for recessed-gate FinFET has been established, which can provide valuable theoretical reference for the recessed-gate FinFET design.

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