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Chin. Phys. B . 2012, 21(5): 057304. **doi:** 10.1088/1674-1056/21/5/057304

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# Key technologies for dual high-$k$ and dual metal gate integration*

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The key technologies for the dual high-$k$ and dual metal gate, such as the electrical optimization of metal insert poly-Si stack structure, the separating of high-$k$ and metal gate of n/pMOS in different regions of the wafer, and the synchronous etching of n/pMOS gate stack, are successfully developed. First, reasonable flat-band voltage and equivalent oxide thickness of pMOS MIPS structure are obtained by further optimizing the HfSiAlON dielectric through incorporating more Al–O dipole at interface between HfSiAlON and bottom $SiO_x$. Then, the separating of high-$k$ and metal gate for n/pMOS is achieved by SC1 ($NH_4OH$:$H_2O_2$:$H_2O$ = 1 : 1 : 5) and DHF-based solution for the selective removing of nMOS TaN and HfSiON and by $BCl_3$-based plasma and DHF-based solution for the selective removing of pMOS TaN/Mo and HfSiAlON. After that, the synchronous etching of n/pMOS gate stack is developed by utilizing optimized $BCl_3$/$SF_6$/$O_2$/Ar plasma to obtain a vertical profile for TaN and TaN/Mo and by utilizing $BCl_3$/Ar plasma combined with DHF-based solution to achieve high selectivity to Si substrate. Finally, good electrical characteristics of CMOS devices, obtained by utilizing these new developed technologies, further confirm that they are practicable technologies for DHDMG integration.

**Keywords:** high-$k$, metal gate, metal insert poly-Si stack (MIPS), dual high-$k$ and dual metal gate (DHDMG) integration

**PACS:** 73.40.Qv, 73.50.Mx, 73.90.+f **DOI:** 10.1088/1674-1056/27/9/097306

## 1. Introduction

Over more than the last ten years, there have been lots of studies of high-$k$/metal gate technologies, such as the suitable threshold voltage ($V_t$) control and process integration.[1–3] For example, a suitable $V_t$ under gate-first process can be achieved by engineering the work function through the introduction of a lanthanide based element (e.g., Yb, La, Gd, or Er) into metal gate.[4–8] or the implementation of a thin capping layer below or above the Hf-based dielectric.[9,10] Moreover, among a variety of high-$k$/metal gate integration strategies, the dual high-$k$ and dual metal gate (DHDMG) method is a practical scheme to achieve a reasonable $V_t$ by optimizing the high-$k$ and metal gate process for n/pMOS separately.[11] Although our previous studies of nMOS TaN/HfSiON and pMOS MoAlN/HfSiAlON gate stack under gate-last process could achieve a suitable $V_t$,[12,13] their metal insert poly-Si stack (MIPS) structures of DHDMG integration still need further verification, especially for pMOS due to its Mo thickness reduction and adding TaN barrier layer to avoid reacting poly-Si with Mo metal gate. In addition, excluding $V_t$ control, forming two different high-$k$/metal gate stacks, including the separating of high-$k$ and metal gate of n/pMOS in different regions of the wafer and the synchronous etching of n/pMOS MIPS structure, is also a challenge. Some studies have already been performed on dual metal gate integration[14] and MIPS structure etching,[15] but to our knowledge, the separating of TaN/HfSiON (nMOS) and TaN/Mo/HfSiAlON (pMOS) MIPS structure and the dry etching of two different thickness and composition gate-stacks at the same time have not been explored before.

In this research, electrical optimization of n/pMOS MIPS structure is first demonstrated. Then, the separating of high-$k$ and metal gate of n/pMOS in different regions of the wafer and the synchronous etching of n/pMOS gate stack for DHDMG integration process are presented. Finally, good CMOS device electrical characteristics, such as excellent drive currents, symmetric $V_t$ values, and good short channel effect (SCE) control, are obtained by utilizing these new developed technologies.

## 2. Experiment

CMOS process flow chart under DHDMG process with MIPS structure is shown in Fig. 1. After the formation of N/P well and local oxidation of silicon process (LOCOS), super-steep retrograde channel doping was performed using heavy ion implantation ($B^+$+$In^+$ for nMOS and $P^+$+$Sb^+$ for pMOS). Then, $V_t$ control through different high-$k$ and metal gate stack for n/pMOS separately was achieved by using the DHDMG process. After the 1st high-$k$ (HK), metal gate (MG) and a-Si hardmask (HM) for nMOS were sequentially deposited on the $SiO_x$ interfacial layer, they were selectively removed from the PMOS region. Then, the 2nd HK and MG for pMOS were deposited on the exposed PMOS region and on the remaining a-Si HM, followed by the 2nd a-Si HM deposited and patterned to remove the 2nd high-$k$ and 2nd metal gate in the NMOS area. After separating the HK and MG on n/pMOS regions, a-Si HM was removed, followed by 1000 Å poly-Si capping. After gate patterning, a thin $Si_3N_4$ side-

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wall was made beside the gate stack and ultra-shallow S/D extension regions were formed by low energy ion implantation (I/I). Before S/D implantation, an oxide sidewall was made to form a double sidewall structure to improve the SCE. Then, 1000 °C spike annealing was used to activate S/D dopants after n/pMOS S/D implantation. After a Ni-silicidation process, a standard CMOS integration was employed for the remaining process steps.

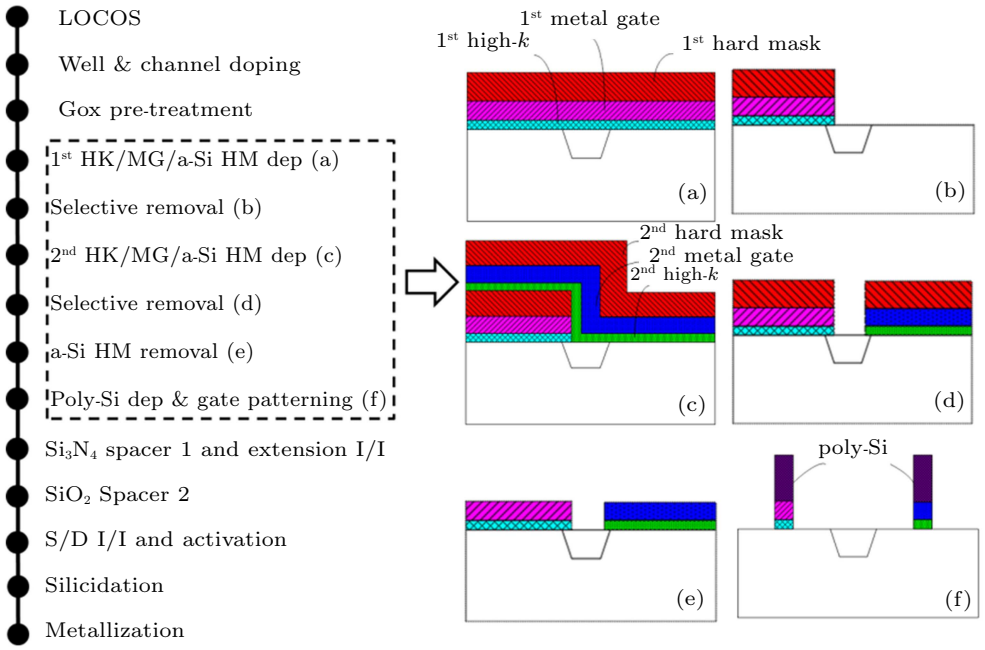



**Fig. 1.** (color online) Process flow of CMOS device with DHDMG process.

## 3. Results and discussion

In this part, the development of key technologies, such as the electrical optimization of n/pMOS MIPS structure, the separating of high-*k* and metal gate of n/pMOS, and the synchronous etching of n/pMOS gate stack, for DHDMG integration process and the electrical evaluation of CMOS device will be discussed in detail.

### 3.1. Electrical optimization of n/pMOS MIPS gate stack

The first challenge of DHDMG integration is to control the effective workfunction (EWF) of a MIPS structure after high temperature processing, so n/pMOS MIPS structure capacitors under similar DHDMG process and the same thermal budget are checked and optimized first. For example, high-*k* post deposition annealing (PDA, 900 °C, 30 s) and S/D activation annealing (1000 °C, 5 s) are used for nMOS TaN/HfSiON MIPS structure capacitor to simulate a real process of nMOS device. Comparing with that of optimized pure TaN/HfSiON stack, the flat-band voltages ($V_{fb}$) of 140 Å and 300 Å TaN MIPS structures only increase by 0.05 V and 0.1 V, respectively, and neither of their equivalent oxide thickness (EOT) has obvious improvement, as shown in Fig. 2. This result indicates that an nMOS MIPS structure after high temperature annealing has little impact on electrical characteristics of TaN/HfSiON even chose 300 Å TaN for nMOS MIPS structure.

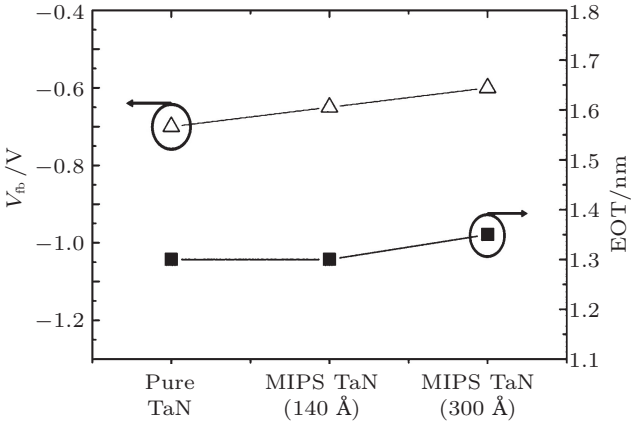



**Fig. 2.** $V_{fb}$ and EOT of nMOS TaN/HfSiON and its MIPS structure capacitors.

Figure 3 shows $V_{fb}$ and EOT of pMOS capacitors with Mo/HfSiAlON stack (notation A) and its MIPS structures (notations B–F). For pMOS TaN/Mo/HfSiAlON MIPS structures capacitors, HfSiAlON PDA (600 °C, 60 s) and S/D activation annealing (1000 °C, 5 s) are adopted to simulate the pMOS device fabrication in DHDMG process. It is found that notation B of poly-Si/TaN(50 Å)/Mo(120 Å)/HfSiAlON MIPS structure has an obvious influence on EWF due to its $V_{fb}$ decreasing from 0.6 V to 0.2 V. The decrease of $V_{fb}$ can be ascribed to Mo metal thickness decreasing to 120 Å and Ta element of TaN barrier layer interdiffusion and piling up at the interface between Mo and HfSiAlON during S/D activation annealing. More Al atoms' incorporation into high-*k* layer is proposed to

improve $V_{fb}$ and EWF of pMOS MIPS structures, as a result of more Al–O dipole formation at the interface between the high-$k$ layer and bottom $SiO_x$ after S/D activation annealing.[13] However, comparing with notation B condition, capping 11 Å and 30 Å $AlN_x$ on HfSiAlON (notations C and D) achieve only 0.12 V and 0.2 V of $V_{fb}$ gain, but with unacceptable 2 Å and 5 Å of EOT increasing, respectively. This signature indicates that the AlN capping layer already transforms into dielectric and induces EOT to increase, but cannot provide enough Al–O dipole formation at the high-$k$ layer and bottom $SiO_x$ interface to improve $V_{fb}$. So, the further optimization of Al atom concentration in HfSiAlON near the high-$k$ layer and bottom $SiO_x$ interface (notations E and F) is proposed to improve $V_{fb}$. Moreover, in order to maintain the EOT performance, the AlN capping layer is not employed for notation E or F condition. It is found that notation E and F condition could be effective in modulating $V_{fb}$ to 0.45 V and 0.6 V while keeping the increase of EOT minimal (0.5 Å and 1 Å). So, notation F condition is finally selected as a pMOS final MIPS structure in terms of electrical optimization to meet the requirement for DHDMG process.

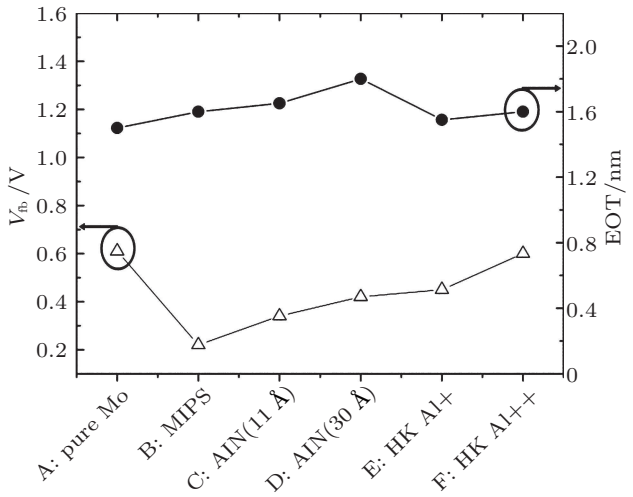



**Fig. 3.** $V_{fb}$ and EOT of pMOS Mo/HfSiAlON and its MIPS structure capacitors.

### 3.2. Separating of high-$k$ and metal gate for n/pMOS

The next challenge of DHDMG process is to form two different metal/high-$k$ stacks for n/pMOS in different regions of the wafer. Our proposed strategy is that the nMOS gate stack is selectively removed from the PMOS region by wet etching first and then the pMOS gate stack is selectively removed by dry etching combined with the wet etching method.

Figure 4(a) presents pMOS a-Si HM/TaN/Mo/HfSiAlON which is deposited sequentially on the exposed PMOS region and on the Si hardmask in the NMOS region after selectively removing the nMOS TaN by SC1 etchant at 60 °C and selectively removing the HfSiON dielectric by DHF/HCl/alcohol (1 : 10 : 89) solution. The SC1 is employed to remove TaN selectively due to its reasonable etch rate (26.3 Å/min) and high selectivity to HfSiON dielectric (202 : 1) and a-Si hardmask(51 : 1).[16] Meanwhile, compared with 1% DHF used to remove HfSiON dielectric, DHF/HCl/alcohol solution could achieve not only a high etch rate (from 6.1 nm/min to 11.9 nm/min) but also high selectivity of HfSiON to $SiO_2$ (from 3.47 : 1 to 20.5 : 1).[17] In addition, it is found that the pMOS high-$k$ PDA process not only affects first deposited nMOS thermal budget but also influences the a-Si hardmask removal of nMOS since a-Si may change into poly-Si under high temperature and cannot be removed by $NH_4OH$ solution. So, lower HfSiAlON PDA(600 °C, 60 s) is a practicable method for DHDMG process without obviously electrical influence since S/D activation annealing can provide enough thermal quantity to form Al–O dipoles at the interface between high-$k$ and bottom $SiO_x$ (already verified by the pMOS MIPS structure capacitor in Subsection 3.1). Figure 4(b) shows that the TaN/Mo gate stack is selectively removed by $BCl_3$-based plasma first[18] and then HfSiAlON dielectric is selectively removed by DHF/HCl/alcohol solution in the nMOS region. Dry etching is used to implement the Mo metal gate selective removal because SC1 wet etching for a Mo metal gate suffers a high lateral etch rate (1.7 μm/min), which is limited by the design rule for isolation space from metal to isolation ($<$ 100 nm). In addition, due to underlying Si hardmask in the nMOS area, the TaN/HfSiON gate stack has no influence during pMOS gate stack selective removal. Figure 4(c) shows the remaining a-Si hardmask on n/pMOS, which is removed completely with an $NH_4OH$ (1 : 10) solution at 60 °C, with high selectivity to below layers.[16] After separating the high-$k$ layer and metal gate in the n/pMOS region, a 1000 Å poly-Si capping is deposited to form an MIPS structure as shown in Fig. 4(d).

### 3.3. Synchronous etching of an n/pMOS gate stack

After fabricating the n/pMOS MIPS structure, the next challenge of DHDMG integration is to synchronously etch the n/pMOS gate stack with vertical profile and little Si loss. MIPS gate stack etching strategy and etching oxide HM and poly-Si layer could be found in our previous study.[18] In this work, we will focus on the synchronous etching of the metal gate/high-$k$ in MIPS structure.

Based on previous study on the etching of an MIPS structure, the $BCl_3/Cl_2/O_2/Ar$ plasma is first investigated for synchronously etching the n/pMOS metal gates.[18] Although optimized $BCl_3/Cl_2/O_2/Ar$ plasma could achieve a vertical profile for nMOS TaN and pMOS TaN/Mo stack respectively, plasma etching conditions, such as top/bottom power and ratio of $BCl_3/Cl_2$ flow, are different. A tapered profile of TaN can be obtained if optimized TaN/Mo etching condition is used for synchronously etching TaN and TaN/Mo stacks as shown in Fig. 5. So, there is no identical $BCl_3/Cl_2/O_2/Ar$ plasma condition for synchronously etching TaN and TaN/Mo.

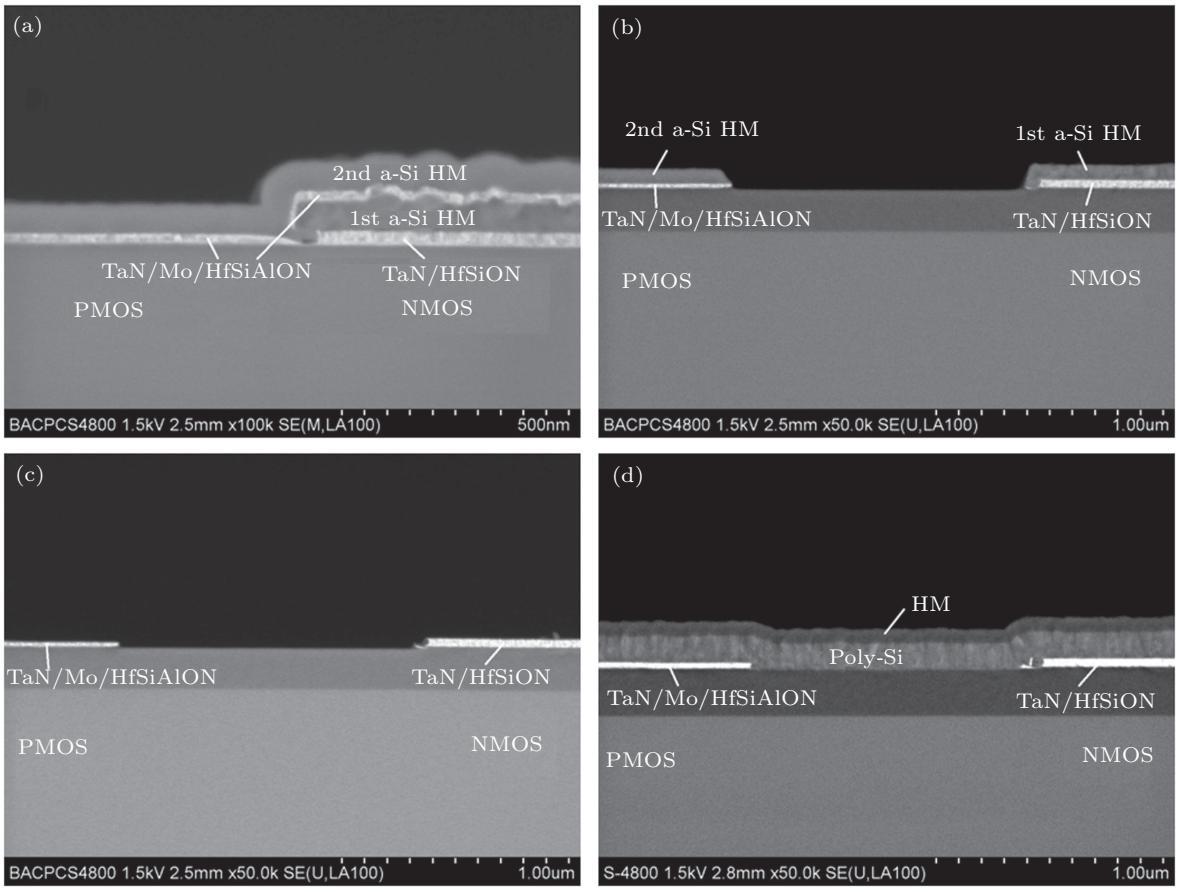



**Fig. 4.** Separating of high-*k* and metal gate for n/pMOS. (a) TaN/Mo/HfSiAlON deposition after selectively removing TaN/HfSiON, (b) TaN/Mo/HfSiAlON selectively removing, (c) a-Si hardmask removing, and (d) Poly-Si capping.

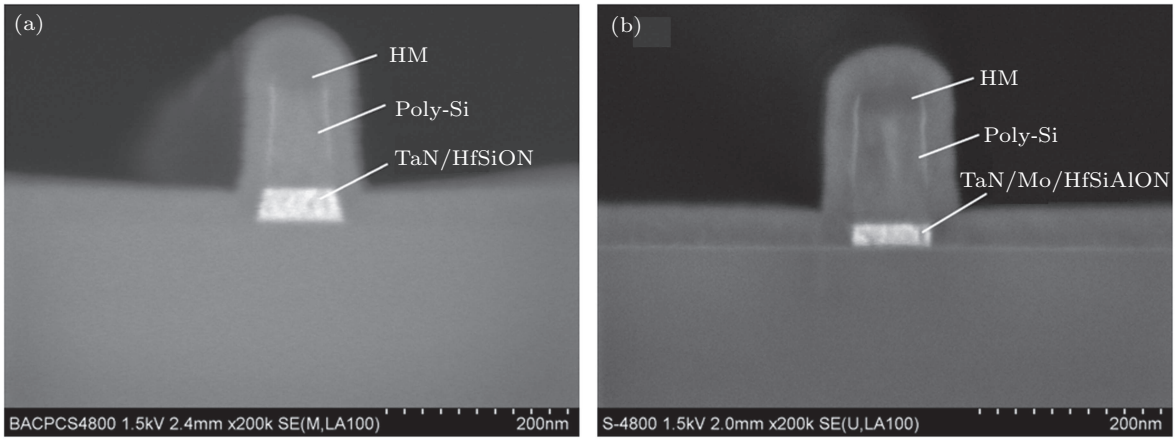



**Fig. 5.** (a) Tapered TaN and (b) vertical TaN/Mo profiles obtained under optimized $BCl_3/Cl_2/O_2/Ar$ plasma for TaN/Mo stack.

Then, optimized $BCl_3/SF_6/O_2/Ar$ plasma, obtained not by simply replacing $Cl_2$ with $SF_6$, is finally developed to etch TaN and TaN/Mo simultaneously under the identical process condition since more isotropic $SF_6$ could obtain more space to optimize top/bottom power and gas ratio in terms of vertical profile and high selectivity. In order to etch off n/pMOS gate stack simultaneously, 300 Å TaN is chosen as an nMOS MIPS structure for optimized pMOS notation F condition since TaN etching rate is twice that of Mo under optimized $BCl_3/SF_6/O_2/Ar$ plasma. Figure 6 shows that the TaN(300 Å) and TaN(50 Å)/Mo(120 Å) in MIPS structure are simultaneously etched off by optimized $BCl_3/SF_6/O_2/Ar$ plasma with a vertical profile and no Si loss.

In order to achieve a high selectivity to Si substrate, optimized $BCl_3/Ar$ plasma combined with following DHF/HCl/alcohol solution clean is employed to remove HfSiON and HfSiAlON dielectric after synchronously etching TaN and TaN/Mo. Figure 7 shows the XPS analysis result

for high-$k$ dielectric removed by $BCl_3$/Ar plasma of 4 s and $BCl_3$/Ar plasma of 4 s combined with DHF/HCl/alcohol solution of 6 s. The peaks of Hf 4f in curve $A$ indicate that the high-$k$ dielectric still exists on Si substrate and the peaks of Hf 4f under extra DHF/HCl/alcohol solution of 6 s in curve $B$ have disappeared, implying that they are completely removed without Si substrate loss.

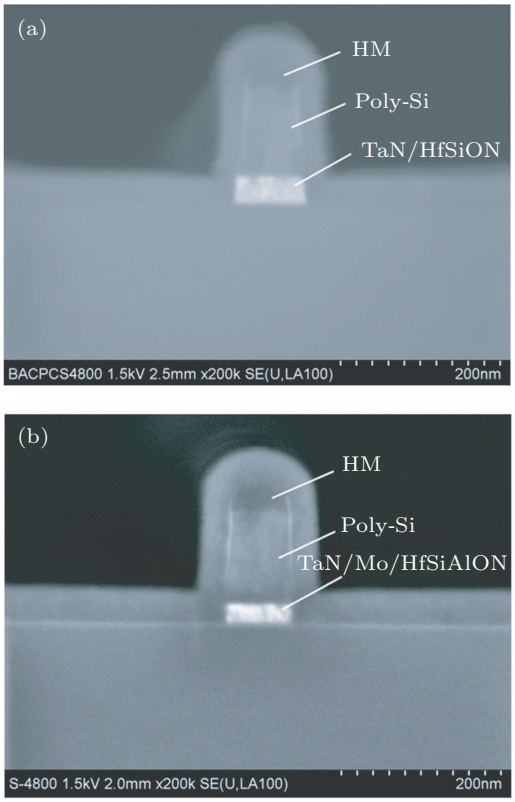



**Fig. 6.** SEM image of (a) TaN and (b) TaN/Mo synchronously etched by optimized $BCl_3/SF_6/O_2$/Ar plasma in MIPS structure for DHDMG process.

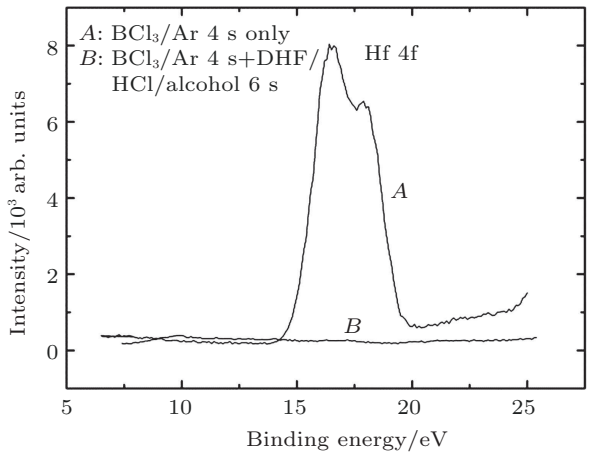



**Fig. 7.** Hf 4f XPS spectrum analysis under $BCl_3$/Ar plasma only and $BCl_3$/Ar plasma combined with following DHF/HCl/alcohol solution clean.

### 3.4. Device verification

The new developed key technologies for DHDMG integration are successfully used for fabricating the 40 nm gate length CMOS devices. The $I_{DS}$–$V_{DS}$ and $I_{DS}$–$V_{GS}$ characteristics of nMOS with 300 Å TaN MIPS structure and pMOS with notation F condition are shown in Figs. 8(a) and 8(b). Excellent drive current $I_{DS}$ of 271/150 μA/μm for n/pMOS under $V_{DS} = V_{GS} = 1$ V are obtained without using any strain-induced mobility enhancement technology. Symmetric $V_t$ of n/pMOS extracted at $I_{DS}$ of 1 μA/μm is 0.36/−0.39 V. Also, good SCE, such as the subthreshold slope of 94/105 mV/decade and drain induced barrier lowering (DIBL) of 85/110 mV/V, is obtained for n/pMOS.

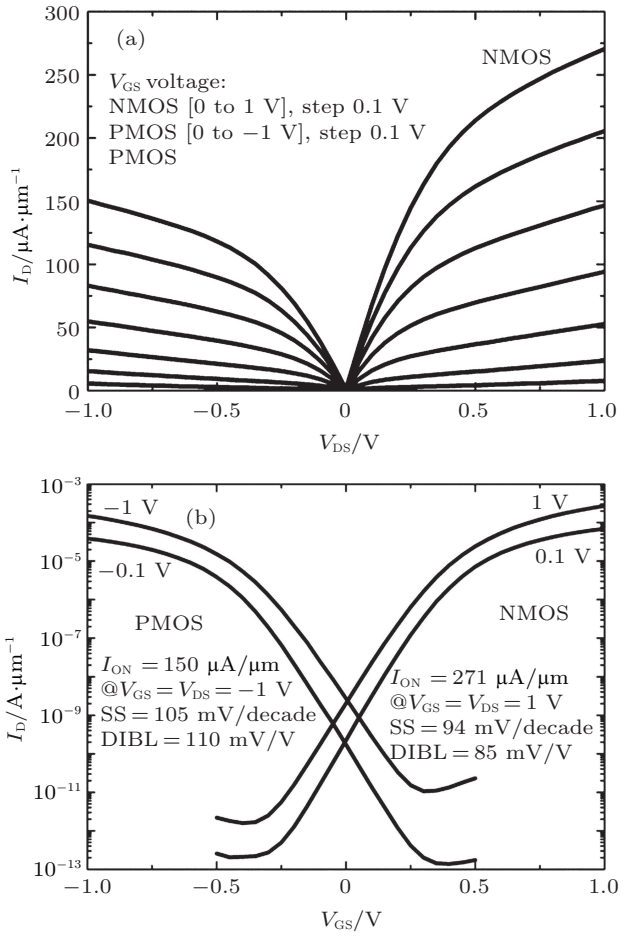



**Fig. 8.** (a) $I_{DS}$–$V_{DS}$ and (b) $I_{DS}$–$V_{GS}$ curves of a CMOS device using these newly developed key technologies for DHDMG integration.

## 4. Conclusion

In this work, key technologies, such as the electrical optimization of n/pMOS MIPS structure, the separating of high-$k$ and metal gate for n/pMOS, and the synchronous etching of n/pMOS gate stack, are successfully developed. Moreover, good electrical characteristics of CMOS device obtained by utilizing these key technologies further prove that they are practical in DHDMG integration.

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