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Modeling capacitance–voltage characteristic of TiW/p-InP Schottky barrier diode*

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The capacitance–voltage (C–V) characteristic of the TiW/p-InP Schottky barrier diodes (SBDs) is analyzed considering the effects of the interface state (N_{ss}), series resistance (R_s), and deep level defects. The C–V of the Schottky contact is modeled based on the physical mechanism of the interfacial state and series resistance effect. The fitting coefficients α and β are used to reflect the N_{ss} and R_s on the C–V characteristics, respectively. The α decreases with the increase of frequency, while β increases with the increase of frequency. The capacitance increases with the increase of α and the decrease of β. From our model, the peak capacitance and its position can be estimated. The experimental value is found to be larger than the calculated one at the lower voltage. This phenomenon can be explained by the effect of deep level defects.

Keywords: Schottky barrier diode, interface state, series resistance

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1. Introduction

Metal–semiconductor (MS) junctions can be considered as the basis of all semiconductor devices. According to different operational principles, MS junctions can be divided into Ohmic and Schottky types. The InP is the III–V compound semiconductor, and has been extensively used in many areas recently.[1,2] Compared with Si and GaAs,[3–5] metal film deposited on InP material has attracted a great deal of attention because of its high electron mobility, high-saturation drift velocity, direct energy band gap, and radiation hardness. The interface of the MS contact is very important for the device performances. However, it is difficult to achieve the ideal interface due to the environmental pollution in the manufacturing process of the devices, wafer inbuilt defects, vacancies and their complexes, formation of residual native oxide, etc. These factors lead to the interface trap states at the junction. The interface trap states can influence the performance, reliability, and stability of Schottky barrier diodes (SBDs), such as switching speed and frequency response of SBDs used in lots of switching and frequency applications.[6,7] Furthermore, the common ways to study the interfacial characteristics of SBDs are the capacitance–voltage (C–V) and current–voltage (I–V) methods, which have been used to study the interface state (N_{ss}) and series resistance (R_s) of TiW/p-InP.[8,9] The TiW is one of the widely used alloys in silicon CMOS technology as the diffusion blocking layer. In addition, TiW has been reported as the Schottky contact metal with Si substrate.[10,11] The TiW silicide gate has been used as the gate material for ultra-high-speed GaAs MESFET.[12] In this paper, we study the C–V characteristics of TiW alloy (in which the titanium fraction is 10% and the tungsten fraction is 90%)/p-InP SBD by establishing the physical model. A good interface contact is essential for SBDs. Better interface characteristics can be obtained by choosing the proper annealing temperature. To obtain a good interface of TiW/InP SBD, we choose 300 °C as the annealing temperature.[13]

Under the applied voltage and frequency, the existence of N_{ss} produces an anomaly in the forward-bias C–V curve of the SBD. In the past few years, many researchers have found anomalous peaks in the C–V characteristics of SBD, and explained that the phenomenon is related with the N_{ss}.[14–20] The interface trap states have an influence on the carrier transport, which induces the constraint in switching speed. The variation of R_s with the frequency and applied voltage is very important for C–V characteristics.

In this paper, the main task is to study the C–V characteristics of the TiW/p-InP SBD by establishing the physical model. According to the carrier confinement effect, the interface state, series resistance, and deep level defects, we can obtain the factors that affect the C–V characteristics by quantitative analysis.

2. Experiment

The substrate wafer was a p-InP wafer with a carrier concentration of 5.2×10^{17} cm^{-3}. The InP wafer was first degreased in acetone and methanol, and rinsed in deionized (DI) water. Then, HF:H_2O (1:10) was used to remove the native oxides from the wafer surface. The Ohmic contact and Schottky contact were both formed by sputtering. Ti(20 nm)/Pt(30 nm)/Au(150 nm) was used as the Ohmic con-

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tact on the bottom surface and TiW alloy was deposited as the Schottky contact on the front surface. Finally, the wafer was annealed at 300 °C for 1 min under N_2 atmosphere by rapid thermal annealing (RTA). These contact patterns with a diameter of 1 mm were all defined by photolithography and formed by the lift-off process. The *C*–*V* measurement was conducted by using an Agilent E4980A LCR meter.

3. Results and discussion

The structure of the TiW/p-InP SBD is shown in Fig. 1(a). In fact, the surface of InP is easily oxidized, and there will be an additional layer oxidation between TiW and InP. The energy-band diagram of the TiW/p-InP SBD under the applied voltage is shown in Fig. 1(b). In this model, the capacitance can be divided into depletion capacitance C_T and diffusion capacitance C_D. The depletion capacitance is caused by the depletion area of SBD, and is expressed as

$$C_T = \sqrt{\frac{\varepsilon_s q N_A A^2}{2(V_{bi} - V)}}, \tag{1}$$

where V_{bi} is the built-in potential, q is the electronic charge, N_A is the carrier concentration, ε_s is the permittivity of the InP material, and A is the diode area. Equation (1) shows that C_T increases with increasing A and N_A.

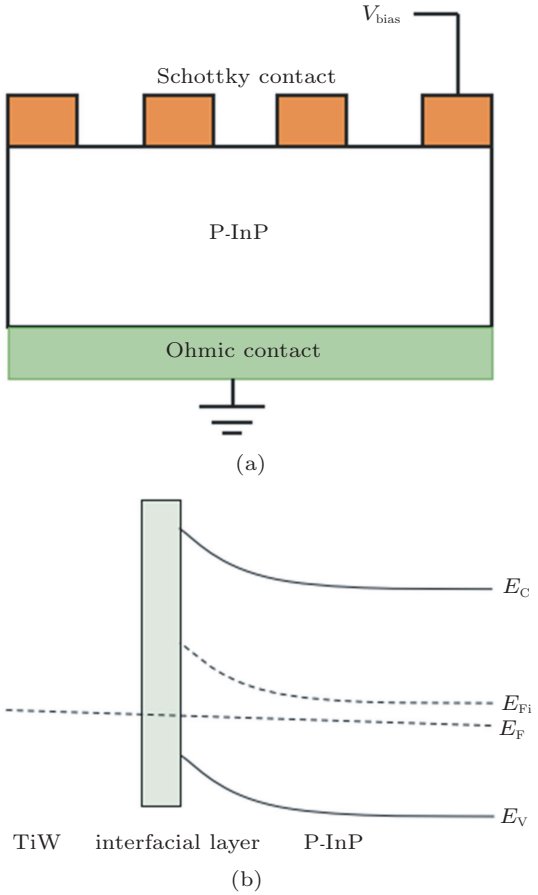


Fig. 1. (color online) (a) Structure of TiW/p-InP SBD, and (b) energy band diagram of the TiW/p-InP structure.

The diffusion capacitance of SBD appears due to the interface states and series resistance. Some factors relating to the interface states have been extracted and calculated.[8] First, in order to simplify the model, we only take into account the interface state. When the carriers pass through the interface of TiW/p-InP, they will participate in the capture-emission process due to the interface state. Then, the effective carrier density (n_d) is

$$n_d(V) = \frac{N_{ss}}{1 + \exp(\alpha(E_g - E_{ss} + E_V - qV)/KT)}, \tag{2}$$

where E_{ss} is the interface state from the valence band (E_v) edge, N_{ss} is the density of the interface states,[8] and the parameter α is given by[16,21,22]

$$\alpha = \frac{qN_{ss}\delta}{\varepsilon_i}, \tag{3}$$

where δ is the thickness of the interfacial layer oxide, which may exist between the InP substrate and TiW contact due to organic contamination or oxidation in laboratory conditions,[9,23–26] and ε_i is the permittivity of the interfacial layer oxide.[27,28]

The E_{ss} is dependent on frequency f[16]

$$\frac{E_{ss}}{q} = \frac{kT}{q} \ln\left(\frac{v_{th}\sigma_n N_A}{f}\right), \tag{4}$$

where v_{th} is the thermal velocity of the majority charge carriers and σ_n represents the capture cross-section of the interface traps. The diffusion capacitance C_D can be obtained from

$$C_D = q\frac{dn_d(V)}{dV}. \tag{5}$$

Substituting Eq. (2) into Eq. (5), C_D can be obtained as follows:

$$C_D = \frac{q^2 N_{ss}\alpha}{kT}\left(\frac{1}{1 + \exp(\alpha(E_g - E_{ss} + E_V - qV)/kT)}\right)^2 \times \exp(\alpha(E_g - E_{ss} + E_V - qV)/kT). \tag{6}$$

Accordingly, the total capacitance is

$$C = C_T + C_D. \tag{7}$$

In Fig. 2, the fitting result (curve *a*) is not consistent with the experimental result. The series resistance must be taken into account in the model. The value of R_s varies with the applied voltage and frequency, and R_s varies from 0 Ω to 7000 Ω at the frequency range from 10 kHz to 200 kHz.[9] The β is used to reflect the R_s on the *C*–*V* characteristics. The carrier density n_d is obtained as follows:

$$n_d(V) = \frac{N_{ss}}{1 + \exp((\alpha + \beta)(E_g - E_{ss} + E_V - qV)/KT)}. \tag{8}$$

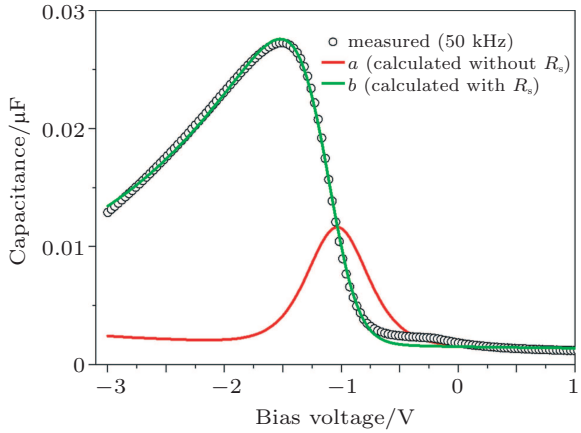


Fig. 2. (color online) Calculated and experimental capacitance–voltage curves with R_s and without R_s.

And C_D is calculated as follows:

$$C_D = \frac{q^2 N_{ss}(\alpha+\beta)}{kT} \times \left(\frac{1}{1+\exp((\alpha+\beta)(E_g-E_{ss}+E_V-qV)/kT)}\right)^2 \times \exp((\alpha+\beta)(E_g-E_{ss}+E_V-qV)/kT). \quad (9)$$

Under low bias voltage, the interface states play an important role in the capture-emission process of carriers, and the R_s can be ignored. With the increase of the voltage, the role of the R_s cannot be ignored. Combined with the physical mechanism, equation (9) can be changed into

$$C_D = \frac{q^2 N_{ss}(\alpha+\beta)}{kT} \times \left(\frac{1}{1+\exp(\alpha(E_g-E_{ss}+E_V-qV)/kT)}\right)^2 \times \exp(\beta(E_g-E_{ss}+E_V-qV)/kT). \quad (10)$$

The fitting result (curve b) in Fig. 2 is consistent with the experimental result. Therefore, the presence of R_s is inevitable and has a great influence on the C–V characteristics.

When f is 50 kHz, the calculated curves and experimental data are plotted in Fig. 3, where $T = 300$ K, $E_g - E_{ss} + E_v = 1.035$ eV, $\alpha = 0.147$, and $N_{ss} = 4\times10^7$ eV^{-1}·cm^{-2}. In Fig. 3, the calculated result fits well with the experimental result under mid-ranges and high bias voltages, but the calculated results are smaller than the experimental data at small bias voltage due to the deep level defects. From the calculated results of C_T and C_D, it can follow that the phenomenon of peak capacitance is mainly caused by the diffusion capacitance (C_D). The C_T is related to the depletion region. The C_D is caused by the effects of interface trap and series resistance. The voltage V_d corresponding to the peak capacitance can be obtained by the derivation of Eq. (10),

$$V_d = \frac{E_g - E_{ss} + E_V}{q} - \frac{kT}{\alpha q}\ln\frac{\beta}{2\alpha-\beta}. \quad (11)$$

From Eq. (11), the position of the peak capacitance can be calculated. The V_d decreases with the decrease of α. According to Eq. (3), we can reduce the thickness of the interfacial layer oxide or use a higher permittivity of the interfacial layer oxide to obtain a smaller V_d.

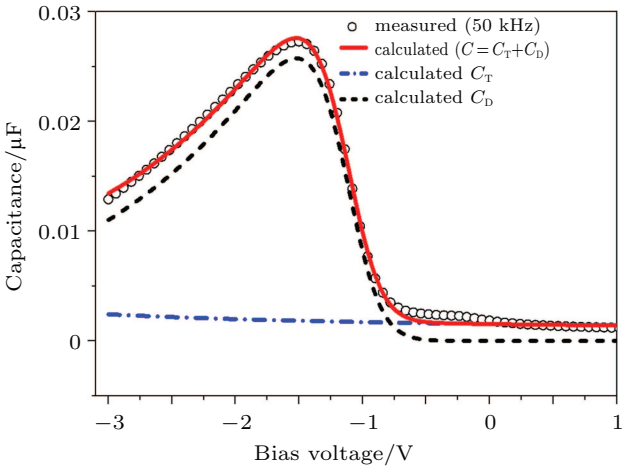


Fig. 3. (color online) Calculated and experimental capacitance–voltage curves at 50 kHz.

As the frequency increases, the capacitance reduces, because the emission-escape time of carriers is less than $1/f$, which leads to the decrease of the N_{ss}. From Fig. 4, it is obvious that the capacitance peaks shift with frequency increasing. This phenomenon can be explained by Eq. (4). The E_{ss} decreases with the increase of f. Therefore, the peak capacitance shifts to higher voltage with the increase of frequency. In addition, the fitting coefficients α and β are also very important. As the frequency increases, α decreases. While the smaller the α coefficient is, the less the carriers are limited by the interface states. So, the peak capacitance is a decreasing function of frequency. The β is used to reflect the influence of the series resistance on the C–V characteristic. Here, the value of β can be extracted by this model. From Table 1 it follows that β increases with frequency increasing. When the fitting coefficient β is greater, the C–V curves decrease slowly.

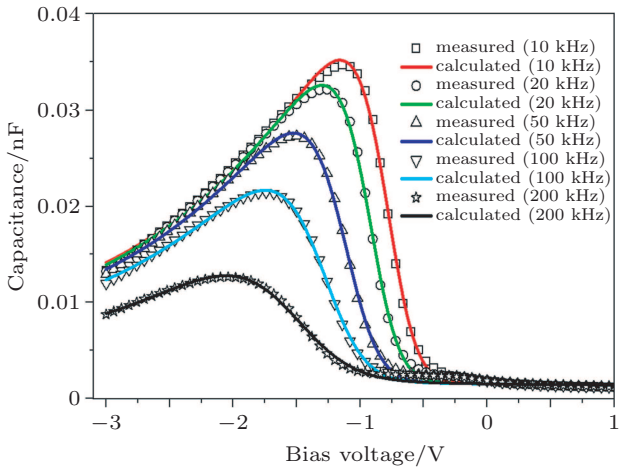


Fig. 4. (color online) Several groups of experimental data and fitting curves.

Table 1. Frequency dependent α and β from the model.

f/ kHz	10	20	50	100	200
α	0.175	0.172	0.151	0.124	0.0858
β	0.01612	0.01654	0.01694	0.01721	0.02073
V_d/V	1.157	1.298	1.521	1.743	2.044

4. Conclusion

The physical model based on the effect of the interface state and series resistance is established to study the frequency and voltage dependence of the C–V characteristic of the TiW/p-InP SBDs. It shows that the effective carriers, which appear above the interface trap energy states, participate in the capture-emission process. The position of the peak capacitance at the corresponding frequency can be estimated by this physical model.

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