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Influences of total ionizing dose on single event effect sensitivity in floating gate cells*

Ya-Nan Yin(殷亚楠)[1,2], Jie Liu(刘杰)[1,†], Qing-Gang Ji(姬庆刚)[1,2], Pei-Xiong Zhao(赵培雄)[1,2], Tian-Qi Liu(刘天奇)[1,2,3], Bing Ye(叶兵)[1], Jie Luo(罗捷)[1,2,3], You-Mei Sun(孙友梅)[1], and Ming-Dong Hou(侯明东)[1]

[1] *Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou* 730000, *China*
[2] *University of Chinese Academy of Sciences, Beijing* 100049, *China*
[3] *Lanzhou University, Lanzhou* 730000, *China*

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The influences of total ionizing dose (TID) on the single event effect (SEE) sensitivity of 34-nm and 25-nm NAND flash memories are investigated in this paper. The increase in the cross section of heavy-ion single event upset (SEU) in memories that have ever been exposed to TID is observed, which is attributed to the combination of the threshold voltage shifts induced by γ-rays and heavy ions. Retention errors in floating gate (FG) cells after heavy ion irradiation are observed. Moreover, the cross section of retention error increases if the memory has ever been exposed to TID. This effect is more evident at a low linear energy transfer (LET) value. The underlying mechanism is identified as the combination of the defects induced by γ-rays and heavy ions, which increases the possibility to constitute a multi-trap assisted tunneling (m-TAT) path across the tunnel oxide.

Keywords: flash memories, heavy ions, synergistic effect, total ionizing dose

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1. Introduction

Flash memories are the most popular non-volatile memories in the semiconductor market. They have been widely used not only in commercial applications but also in many space systems due to their high density and non-volatility.[1] The space radiation environment is characterized by a mixture of the particles trapped in the Earth's radiation belts, which include protons, electrons, and heavy ions, and also the transient particles, which include protons and heavy ions from galactic cosmic rays (GCRs) and solar particle events.[2] The single event effect (SEE) and total ionizing dose (TID) effect caused by the radiation can threaten the operation and service life of flash memory during space missions.

In the past, the most radiation-sensitive part of flash memory was the complex peripheral circuitry, while the floating gate (FG) cell array was not sensitive to radiation.[3,4] With the miniaturization of technology, the quantity of charge stored in FG cells decreases continuously. The FG cell array has become increasingly more sensitive to radiation.[5–7] Currently, the response of FG cells to SEE and TID become an important issue. The responses to these effects have been investigated separately.[8–12] The influence of a combination of SEE and TID on FG single event upset (SEU) has also been studied.[13,14]

In addition to the soft errors in FG cells induced by irradiation, the reliability of flash memory after being irradiated has aroused the interest of researchers. The influence of TID on the retention of flash memory has been studied,[15–17] showing that the retention error occurs after being exposed to 200 krad (Si) and baked at high temperature (100 °C). Some studies have been published about the influence of heavy ion irradiation on the retention,[18–20] reporting that the heavy ions with a sufficiently high LET can generate the retention errors in the FG cells. These studies examined the effect of TID and heavy ion irradiation separately. To our knowledge, the influence of a combination of TID and SEE on the retention of FG cells has not been studied to date.

In this paper, the influence of TID on the SEU of FG cell is investigated, and the influence of TID on the retention error of FG cell after being ever exposed to heavy ions is also studied. The cross sections of the FG cell upsets and retention errors induced by heavy ions are presented, for FG cells with and without ever experienced TID irradiation. The influences of TID on the cross section and the LET threshold ($\mathrm{LET_{th}}$) of heavy-ion induced upsets and retention errors are analysed and the underlying mechanisms are discussed.

2. Experimental details

2.1. Devices under test

In the experiments, two kinds of commercial single level cell (SLC) NAND flash devices manufactured by micron technology are studied: 34-nm and 25-nm flash. The details of the devices studied are summarized in Table 1. The FG cell is

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†Corresponding author. E-mail: j.liu@impcas.ac.cn
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a special type of metal–oxide–semiconductor field-effect transistor (MOSFET) with a programmable threshold voltage (V_{th}) depending on the quantity of trapped charge in the FG. When the cell V_{th} is lower than the read voltage, the cell is on ('1'), otherwise it is off ('0'). The sketch of SLC flash cell V_{th} distribution is shown in Fig. 1.

Table 1. Micron technology NAND flash memories under study.

Part number	Density/Gb	Date code	Feature size/nm
MT29F1G08ABADA	1	1340	34
MT29F16G08ABACA	16	1446	25

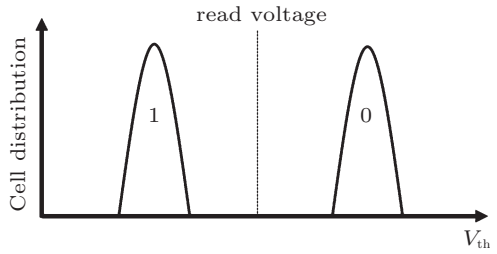


Fig. 1. Sketch for V_{th} distribution in SLC flash memories.

2.2. Experiment setup

The TID irradiations were performed using ^{60}Co γ-rays at Xin Jiang Technical Institute of Physics and Chemistry, Chinese Academy of Sciences, with a dose rate of 100 rad (Si)/s. The 34-nm devices were irradiated by 40 krad (Si), and the 25-nm devices were irradiated by 30 krad (Si). Heavy ion irradiations were performed at the Heavy Ion Research Facility in Lanzhou (HIRFL). Three types of heavy ions (^{86}Kr, ^{129}Xe, and ^{209}Bi) were used to irradiate the flash memories and the Al degraders with different thickness values were used to obtain different energies in order to change the ion LET. An ion fluence of approximately 10^6 ions/cm^2 was achieved and peripheral circuitries of the memory were shielded. The parameters of heavy ions used in the experiments are calculated by the SRIM 2013 code, and the results are listed in Table 2.

Table 2. Parameters of heavy ions used in experiment.

Ion	Ion energy at device surface/MeV	Ion LET at device surface /(MeV·cm^2/mg)	Ion range in silicon/μm
^{86}Kr	1818.1	20.7	268.7
^{86}Kr	1007.5	29.1	92.4
^{86}Kr	479.8	37.6	58.5
^{129}Xe	711.0	67.1	54.1
^{209}Bi	923.2	99.8	53.7

All the tests were carried out in air at room temperature using a normal incident beam. During all irradiations, the devices were kept unbiased. Three samples of flash memories were tested under their corresponding different experimental conditions. The error correction codes in NAND memories were not implemented. The experimental procedure can be described in detail as follows.

(i) All devices were programmed with all '0' prior to the experiment.

(ii) Some of the devices were irradiated with γ-rays at a given dose. The number of errors was recorded after irradiation.

(iii) About ten days later, all devices were exposed to heavy ions, without any program and erase operations. The number of errors was recorded before and immediately after the irradiation.

(iv) All devices were kept unbiased at room temperature for thousands of hours after irradiation.

(v) All devices were programmed with all '0' once again. Then they were kept unbiased at room temperature and the number of errors was measured periodically for thousands of hours.

3. Results and discussion

3.1. Floating gate single event upset (SEU)

Owing to the low-dose γ-ray irradiation, no error is detected in the NAND memories after the TID irradiation or before heavy ion irradiation. The error is observed only after heavy ion irradiation. Figures 2 and 3 show the cross sections of FG errors measured immediately after heavy ion irradiation as a function of LET in the fresh samples and in the samples exposed to TID before heavy ion irradiation for 34-nm devices and 25-nm devices respectively. The device with smaller feature size memories has a larger SEU cross section than that with the larger feature size memories. The cross section of FG SEU in the sample ever irradiated with TID is larger than that in the unirradiated sample. The enhancement factor values in SEU of the samples ever exposed to TID range from 1.3 to 3.1 for 34-nm devices and from 1.5 to 2.7 for 25-nm devices. The influence of previous TID is not strong and it does not change significantly with the increase of ion LET either. An order of magnitude increase of the SEU cross section

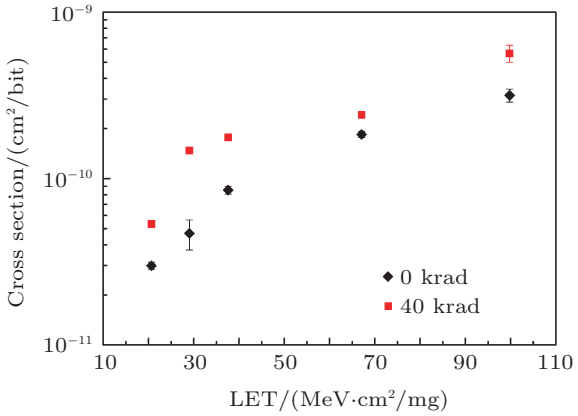


Fig. 2. (color online) Plots of cross section of FG cell upsets induced by heavy ions in 34-nm devices versus LET in fresh samples and in samples ever exposed to 40 krad(Si). No program/erase operation is performed between total-dose and heavy-ion irradiation.

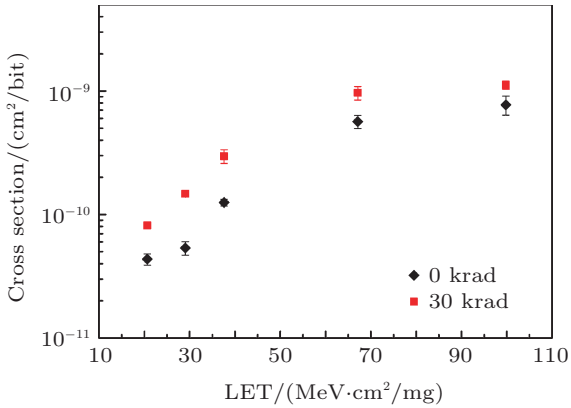


Fig. 3. (color online) Plots of cross section of FG cell upsets induced by heavy ions in 25-nm devices versus LET in fresh samples and in samples ever exposed to 30 krad(Si). No program/erase operation is performed between total-dose and heavy-ion irradiation.

is observed in none of the samples ever exposed to TID, but it is observed in each of the 90-nm samples ever exposed to 20 krad (Si) with Si irradiations (LET∼10 MeV·cm^2/mg).[13] This is because the significant increase of the SEU cross section in the FG cells with TID tends to occur at smaller LET with scaling[11] and the smallest LET used in our experiments is 20.7 MeV·cm^2/mg. Unlike the scenario in the previous work,[13] the difference between the samples ever exposed to TID and the unirradiated samples is still present for the highest LET.

On the basis of the address of the error, it was discovered that some errors gather in clusters of different sizes, i.e., with various numbers of errors. In the experiments, the number of ions that hit the chip is several orders of magnitude smaller than the number of FG cells. It is reasonable to think that the clustered errors are mostly multiple cell upsets (MCUs) caused by a single ion. If the number of clustered errors is N ($N > 1$), it is called MCU (N). Figures 4 and 5 show the average percentages of the different error patterns under different LET ion exposures in fresh samples and in samples exposed to TID for 34-nm and 25-nm memories, respectively. For all the cases, the percentage of MCUs increases with the ion LET increasing. The level of error multiplicity is higher in the sample ever exposed to TID than that in fresh sample under the same conditions.

The increase of the FG SEU cross section in the sample ever exposed to TID is attributed to the $V_{\rm th}$ shift of the FG cell induced by the combination of γ-ray and heavy ion irradiation, which is inconsistent with previous result.[13] The effect of γ-ray irradiation is to shift the $V_{\rm th}$ of FG cell programmed with the '0' towards lower $V_{\rm th}$. The shift is attributed to the radiation-induced injection of carriers from the surrounding oxides into the floating gate, photoemission of electrons in the FG cell, and charge trapped in the tunnel oxide.[21] The effect of heavy ion irradiation is to shift the $V_{\rm th}$ of the FG cell directly hit by ion and other adjacent cells.[22] This is ascribed to charge loss from the FG due to a transient conductive path

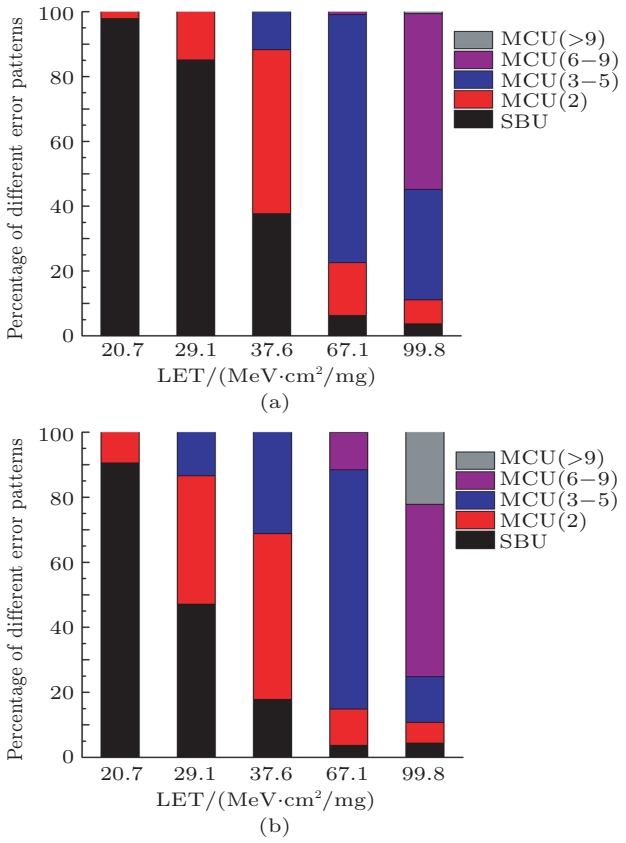


Fig. 4. (color online) Average percentages of different error patterns in 34-nm memories under different LET ion exposures in (a) fresh samples and (b) samples ever exposed to 40 krad (Si).

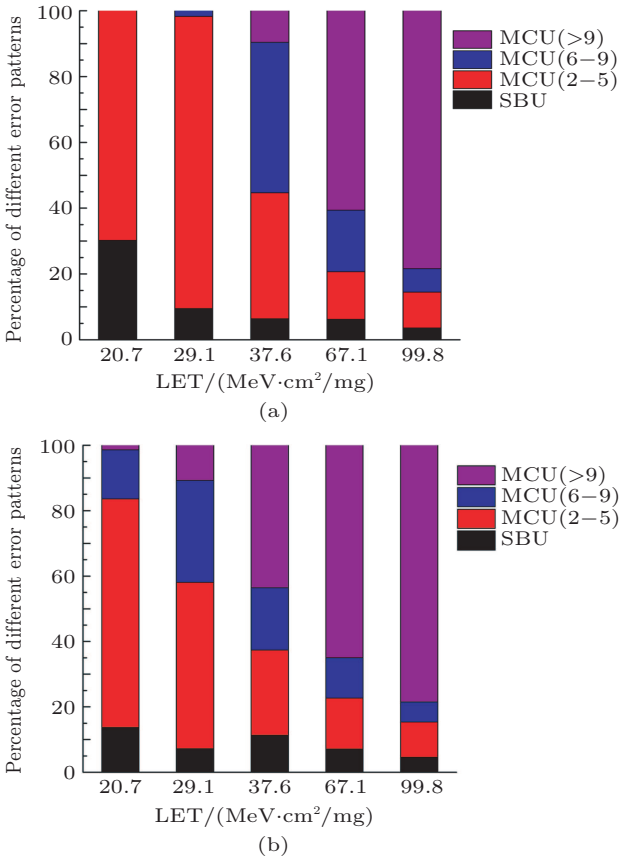


Fig. 5. (color online) Average percentages of different error patterns in 25-nm memories under different LET ion exposures in (a) fresh samples and (b) samples ever exposed to 30 krad (Si).

across the tunnel oxide[23] or the transient carrier flux over the oxide barriers[24] and charges trapped in the tunnel oxide.[25] Owing to the combined effect of γ-ray and heavy ion irradiation, when a sample ever irradiated with γ-rays is irradiated with heavy ions the V_{th} shift of FG cell is larger than that in the sample only irradiated with heavy ions. The cell which would not upset only with heavy ion irradiation may upset after being irradiated by γ-ray and heavy ions owing to a larger V_{th} shift induced by these two irradiation effects. Therefore, the sample ever exposed to TID has a higher percentage of MCUs and a larger SEU cross section than the sample without being ever irradiated by γ-rays.

3.2. Retention errors in floating gate

Having been exposed to heavy ions, all the devices are kept unbiased at room temperature for thousands of hours. Then the samples are erased and programmed again. They are kept unbiased at room temperature and the number of errors is measured periodically for thousands of hours. The evolutions of retention error cross section in 34-nm NAND memories with time after programming under different LET ion exposures in fresh samples and in samples ever exposed to TID are shown in Fig. 6. The cross sections of retention errors show an increasing trend in a few hundred hours after the programming and still increase but slowly after thousands of hours. For the fresh samples, no errors are observed immediately after programming. Approximately 10 min after programming, the retention error appears when the ion LET is 99.8 MeV·cm^2/mg. The retention error appears after approximately 20 hours when the ion LET is 67.1 MeV·cm^2/mg. No error is observed in a reasonable time when the ion LET is 37.6 MeV·cm^2/mg. The LET_{th} value of the retention errors for 34-nm devices is in a range between 37.6 MeV·cm^2/mg and 67.1 MeV·cm^2/mg. For each of the samples exposed to TID, a similar phenomenon is observed albeit with a larger cross section.

The retention errors in 25-nm devices are slightly different. Figure 7 shows the evolutions of the retention error cross section for 25-nm NAND memories with time after programming under different LET ion exposures in fresh samples and in samples that were exposed to TID. For fresh samples, retention errors are observed immediately after programming when the ion LET is high. When the ion LET is 29.1 MeV·cm^2/mg, the retention errors are observed after hundreds of hours. No errors are observed in a reasonable time when the ion LET is 20.7 MeV·cm^2/mg. The LET_{th} value of retention errors for 25-nm devices is in a range between 20.7 MeV·cm^2/mg and 29.1 MeV·cm^2/mg, which is smaller than that in the 34-nm devices. Different results are obtained for the samples ever exposed to TID. The retention errors are observed when the ion LET is 20.7 MeV·cm^2/mg, which means that the LET_{th} value of retention errors is smaller than 20.7 MeV·cm^2/mg. The cross sections of retention errors in the samples ever exposed to TID are larger than those in fresh samples for all situations. When the ion LET is low, only a few retention errors are detected. The number of retention errors increases with the ion LET increasing. Therefore, the error bars are large when the ion LET is low and they tend to be smaller with the ion LET increasing.

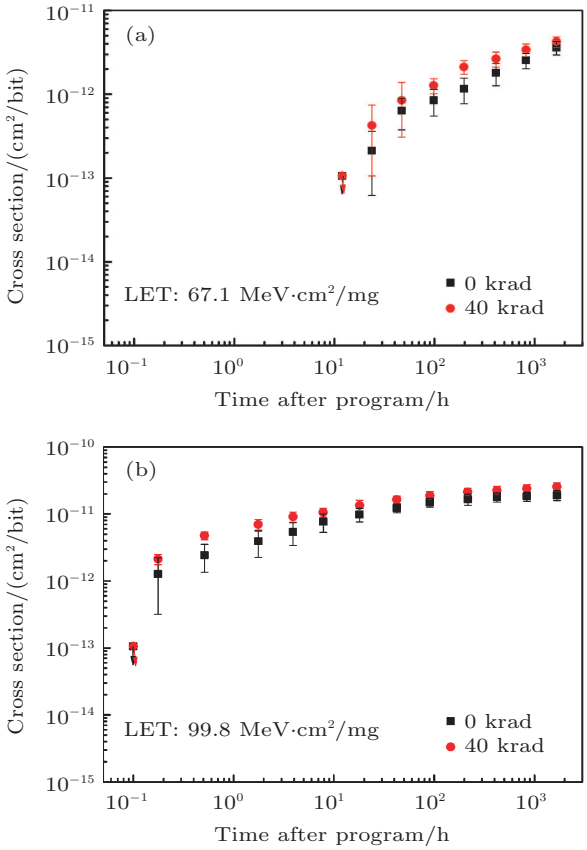


Fig. 6. (color online) Plots of cross section of retention errors in 34-nm NAND memories versus time after programming under different LET ion exposures in fresh samples and in samples ever exposed to TID, with a vertical arrow indicating that no errors are observed, and at ion LET of (a) 67.1 MeV·cm^2/mg and (b) 99.8 MeV·cm^2/mg.

It is noted that the cross section of retention error varies greatly after irradiation with different LET ions. Figure 8 shows the plots of the cross section of retention errors in 25-nm and 34-nm devices detected approximately 1600 h after programming versus ion LET in fresh samples and in samples ever exposed to TID. As the ion LET increases, the cross section of the retention error increases. The cross section of the retention error is about several orders of magnitude lower than that for the FG error. The cross section of the retention error in the 25-nm device is larger than that in the 34-nm device under the same conditions. For the 25-nm device, when the ion LET is 20.7 MeV·cm^2/mg, the influence of previous TID is greater than one order of magnitude and changes the LET_{th} of retention error. As the ion LET increases, the influence of previous TID becomes increasingly weaker. The enhancement factor is only approximately 1.6 for the highest LET. For the 34-nm device, the influence of the previous TID is also small at high LET.

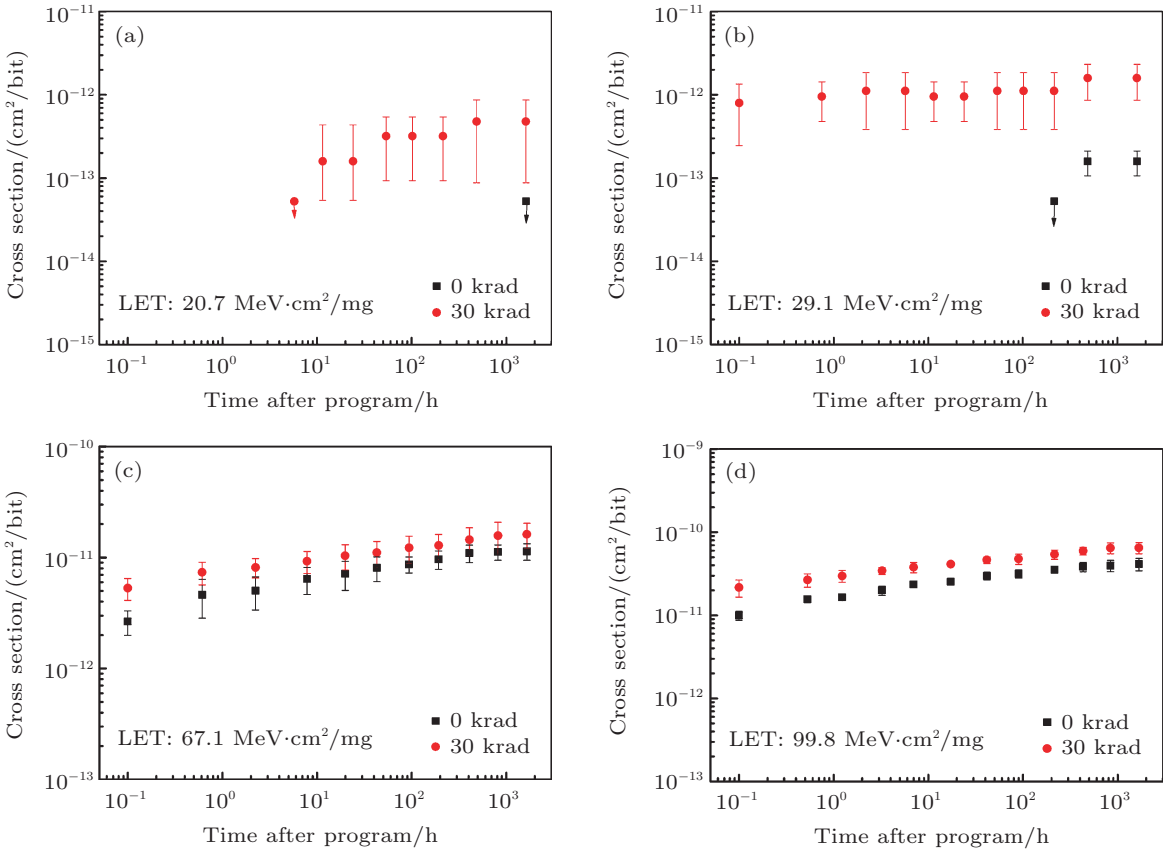


Fig. 7. (color online) Plots of cross section of retention errors in 25-nm NAND memories versus time after programming under different LET ion exposures in fresh samples and in samples ever exposed to TID, with a vertical arrow indicating that no errors have been observed, at ion LETs: (a) 20.7 MeV·cm^2/mg, (b) 29.1 MeV·cm^2/mg, (c) 67.1 MeV·cm^2/mg, and (d) 99.8 MeV·cm^2/mg.

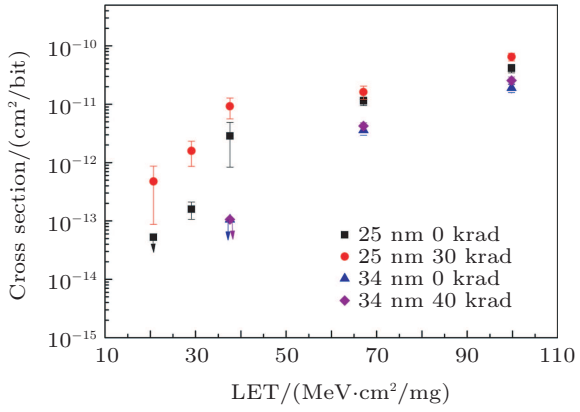


Fig. 8. (color online) Plots of the cross section of retention errors in 25-nm and 34-nm devices detected about 1600 h after program versus ion LET in fresh samples and in samples ever exposed to TID, with a vertical arrow indicating that no errors are observed.

It is generally known that the charge will be generated in the oxides surrounding the FG after irradiation. For a fresh sample, some defects are created in the tunnel oxide by the recombination of the carriers generated by heavy ions.[19] These defects are randomly distributed in the ion track area to construct a multi-trap assisted tunneling (m-TAT) conductive path, which would discharge the FG cell.[19] This is shown schematically in Fig. 9. When the ion LET is low, the number of defects may be too small to leak enough current to discharge an FG cell. However, the density of the carriers induced by heavy ions increases significantly with the ion LET increasing. The heavy ions with higher LET can induce a larger number of defects and a denser defect track, thereby increasing the probability for constructing the path that can generate a measurable error of the FG cell in a reasonable time. Therefore, the cross section of the retention error in FG cell increases with the ion LET increasing. The quantity of charge in the FG cell has kept on decreasing with the ongoing technology miniaturization. The number of defects necessary to create a leakage path to discharge an FG cell is smaller in memory with a smaller feature size, increasing the probability of creating a path that can discharge the FG cell. Therefore, the memory with a smaller feature size has a larger cross section and a smaller $\mathrm{LET_{th}}$.

The defects can also be generated by holes trapped in the tunnel oxide after being irradiated by the γ-rays, which induces the leakage current associated with trap assisted tunneling (TAT).[26] For the sample after being irradiated by the γ-rays and heavy ions, their effects are cumulative. The number of defects in the oxide (N_{de}) is determined by the number of defects induced by both TID (N_{TID}) and heavy ions (N_{HI}). We assume that N_{de} can be approximated as

$$N_{\mathrm{de}} = N_{\mathrm{TID}} + N_{\mathrm{HI}}.$$

The cross section of the retention error after heavy ion exposure is closely related to the number of defects in the

oxide.[19] The cross section of the retention error increases with the number of defects increasing. Therefore, the influence of previous TID is determined by the relative weights of N_{TID} and N_{HI}. The N_{TID} larger than N_{HI} leads to a higher influence of the previous TID on the retention error after heavy ion irradiation. As the ion LET increases, N_{HI} becomes larger, and N_{TID} makes a smaller contribution to N_{de}. Therefore, the influence of the previous TID on the retention error with the low LET ions is larger than that with the higher LET ions.

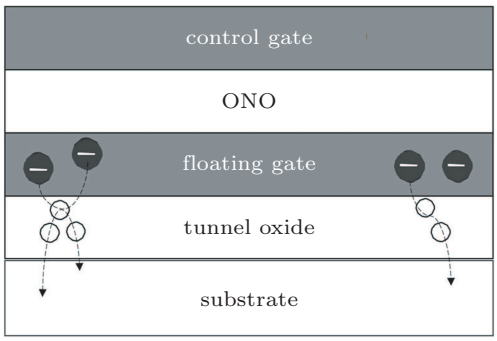


Fig. 9. The sketch of leakage current path induced by defects in tunnel oxide.

4. Conclusions

In this paper, the influences of total ionizing dose on single event effect sensitivity of 34-nm and 25-nm NAND flash memories have been studied. It is found that the cross section of FG error increases and the MCU fraction is higher for memories ever exposed to relatively low TID. This phenomenon is attributed to the combination of the shifts induced by TID and heavy ions. The retention error is observed after the memories have been irradiated by heavy ions with high LET, even though its cross section is about several orders of magnitude lower than that for the FG error. The $\mathrm{LET_{th}}$ of the retention error decreases with the decrease of the feature size, which is unlike the findings of previous work.[18] The cross section of the retention error increases if the memory has been exposed to TID. This is more evident at low ion LET. In addition, the $\mathrm{LET_{th}}$ of the retention error is smaller in the sample ever exposed to TID. The mechanism for the influence of TID on the retention error is identified as the combination of the defects induced by TID and heavy ions, which induces a larger number of defects in the oxide and increases the likelihood of obtaining the m-TAT path across the oxide.

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