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Ge/Si heterojunction L-shape tunnel field-effect transistors with hetero-gate-dielectric*

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A Ge/Si heterojunction L-shaped tunnel field-effect transistor combined with hetero-gate-dielectric (GHL-TFET) is proposed and investigated by TCAD simulation. Current–voltage characteristics, energy-band diagrams, and the distribution of the band-to-band tunneling (BTBT) generation rate of GHL-TFET are analyzed. In addition, the effect of the vertical channel width on the ON-current is studied and the thickness of the gate dielectric is optimized for better suppression of ambipolar current. Moreover, analog/RF figure-of-merits of GHL-TFET are also investigated in terms of the cut-off frequency and gain bandwidth production. Simulation results indicate that the ON-current of GHL-TFET is increased by about three orders of magnitude compared with that of the conventional L-shaped TFET. Besides, the introduction of the hetero-gate-dielectric not only suppresses the ambipolar current effectively but also improves the analog/RF performance drastically. It is demonstrated that the maximum cut-off frequency of GHL-TFET is about 160 GHz, which is 20 times higher than that of the conventional L-shaped TFET.

Keywords: tunnel field-effect transistors, Ge/Si heterojunction, hetero-gate-dielectric, ambipolar effect

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1. Introduction

As the metal–oxide–semiconductor field-effect transistor (MOSFET) is scaled down remarkably for the low power consumption, the power supply voltage V_{dd} should also be reduced simultaneously.[1] However, the MOSFET cannot have a subthreshold swing *SS* below 60 mV/dec at room temperature, which is necessary to maintain a high ON-state current in spite of V_{dd} reduction.[2] Recently, the tunnel field-effect transistor (TFET) has attracted a great deal of attention for its sub-60 mV/dec subthreshold behavior.[3] By modulating the band-to-band tunneling (BTBT) current between the source and channel, TFET does not suffer from the fundamental subthreshold swing limitation, thus has a high ON–OFF ratio at a low V_{dd}.[4] For this reason, TFET has been regarded as one of the most promising candidates in future low-power and high-frequency applications.[5–7] However, the conventional planar silicon-based TFET has an inherent disadvantage of low ON-state current I_{ON} because of silicon's relatively large band gap.[8] In order to boost I_{ON}, various techniques have been reported with simulation and experimental results.[9–22] Among them, an L-shaped TFET (L-TFET) has been proposed to increase the tunneling area by transforming the point-tunneling (parallel to channel) into line-tunneling (perpendicular to channel).[21,22] Recently, Kim *et al.* experimentally demonstrated that an L-shaped TFET can provides more than 1000 times higher ON-current than a conventional planar TFET due to the larger tunnel junction area.[23] Nonetheless, this Si-based L-TFET still has much lower I_{ON} (10^{-2} μA/μm) than the state-of-the-art MOSFET due to the relatively high band gap and tunneling effective mass of silicon.[8] The low I_{ON} of L-TFET means a relatively small transconductance (g_m), which leads to poor radio frequency (RF) performance.[24] In addition, the ambipolar behavior of the L-TFET also remains a challenge, which needs further optimizations for enhancing the application of the L-TFET in integrated circuits.[23]

In order to further boost I_{ON}, suppress ambipolar current, and improve RF performance of the L-TFET simultaneously, a Ge/Si heterojunction L-TFET combined with hetero-gate-dielectric (GHL-TFET) is proposed in this paper. Compared with Si-based TFET, the TFET with Ge-source can achieve much higher I_{ON} due to the low band gap and effective-mass of Ge.[25–30] GHL-TFET has a Ge/Si heterostructure at the interface between the source and channel with a small tunneling barrier, which can boost I_{ON} effectively. What is more, by employing a hetero-gate-dielectric (HGD) structure, GHL-TFET can not only suppress the ambipolar current by increasing the tunneling barrier at the drain/channel interface, but also improve the RF performance by reducing the gate/drain capacitance.[31–37] TCAD simulation results show that our proposed GHL-TFET significantly enhances I_{ON} while effectively suppressing ambipolar current and achieves better RF performance than the conventional L-TFET.

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2. Device structure and simulation parameters

The proposed GHL-TFET structures are illustrated schematically in Fig. 1.

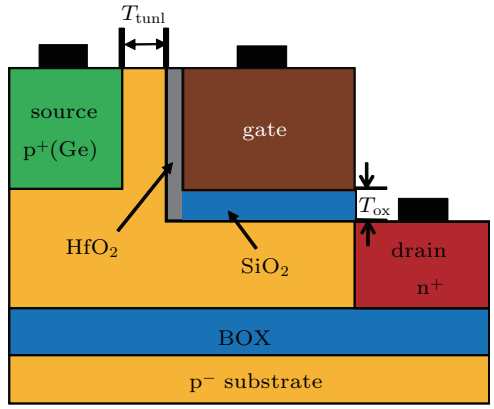


Fig. 1. (color online) Schematic of the proposed Ge/Si heterojunction L-shaped TFET with hetero-gate-dielectrics (GHL-TFET).

Based on the L-TFET, the GHL-TFET is an optimized structure that uses germanium in the source region and employs hetero-gate-dielectrics engineering with a low-κ dielectric (SiO_2) on the drain side whereas high-κ dielectric (HfO_2) on the source adjacent section. For the GHL-TFET, the source region is heavily p-doped (1×10^{20} cm^{-3}), the channel region is lightly n-doped (1×10^{17} cm^{-3}), and the drain region is moderately n-doped (1×10^{18} cm^{-3}). The body thickness (T_{SOI}) and the underlying buried oxide layer thickness (T_{BOX}) are 10 nm, the lengths and heights of the source and drain sections are 20 nm and 25 nm, the gate length (L_g) is 40 nm, and the gate dielectric HfO_2 thickness at the source side is 2 nm. The gate material is metallic with a work function of 4.17 eV. By default, the thickness (T_{tunl}) of the vertical intrinsic channel region is 2 nm and the low-κ dielectric (SiO_2) thickness (T_{ox}) is 3 nm.

The process flow of the proposed GHL-TFET is similar to the fabrication of the L-TFET[23] and the key process steps are shown in Fig. 2. First, the source region is recessed into silicon-on-insulator (SOI) substrate by an etching process. Then, the heavily p-doped germanium source layer is grown by epitaxy for a uniform doping and an abrupt junction, and a hard oxide mask layer is deposited to protect the elevated source region. Afterwards, the intrinsic Si-channel layer is deposited by selective epitaxial growth (SEG) to suppress dopants diffusion from the source into the channel region. Following this, the high-κ gate dielectric (HfO_2) is deposited by atomic layer deposition (ALD). Next, the HfO_2 on the left is protected by a hard oxide mask to selectively etch away the rest of HfO_2. After that, the low-κ gate dielectric (SiO_2) is deposited to form a heterogeneous gate dielectric and the gate region is formed by using a conventional gate-stack technology. Finally, the drain region is formed by ion implantation and contacts are defined.

Performance of the GHL-TFET is investigated by using Sentaurus TCAD simulation tools. To calculate the band-to-band tunneling (BTBT) current, a dynamic nonlocal BTBT model is used. The dynamic nonlocal BTBT model takes into account the spatial variation of the energy band, and therefore can model the tunneling process more accurately. Moreover, due to the presence of high doping concentrations, the OldSlotboom band-gap narrowing model is included and the Shockley–Read–Hall recombination model is also used in the simulation. Specially, two calibrated Kane's tunneling model coefficients $A = 1.46 \times 10^{17}$ cm$^{-3} \cdot$ s^{-1} and $B = 3.59 \times 10^6$ V $\cdot$ cm^{-1} for the Ge from Ref. [27] are utilized in this work.

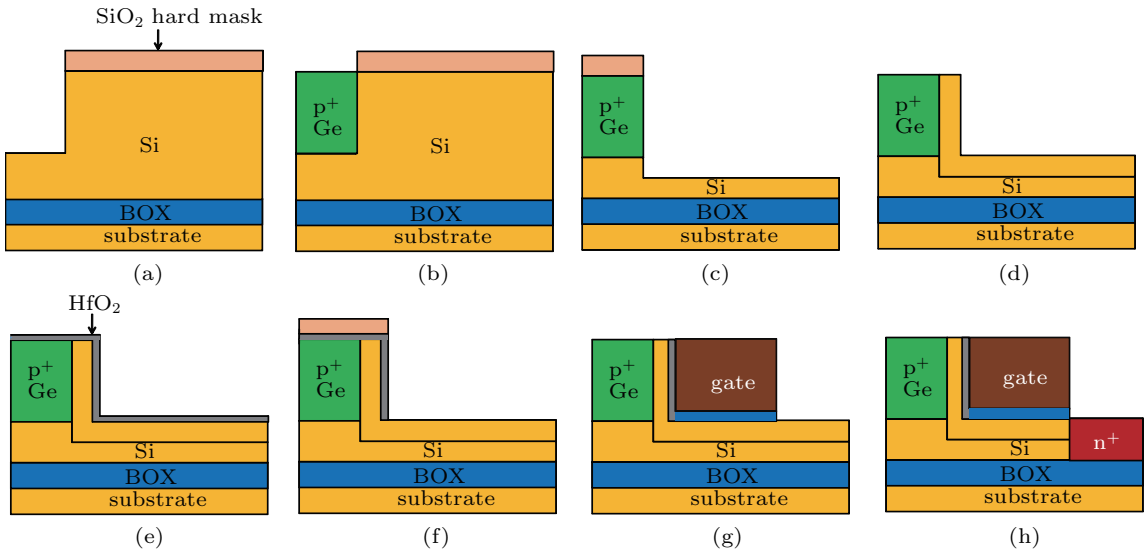


Fig. 2. (color online) Virtual fabrication process flow of the GHL-TFET. (a) Recessing the silicon layer. (b) Growing Ge epitaxial layer for the source region with *in situ* doping. (c) Depositing oxide hard mask. (d) Depositing thin silicon channel by SEG. (e) Depositing HfO_2 by ALD. (f) Etching away the HfO_2 on the right. (g) Depositing SiO_2 by ALD and forming the gate by a high-κ metal stack process. (h) Forming the drain region by ion implantation.

3. Results and discussion

The transfer characteristics of the GHL-TFET compared with those of the conventional L-TFET, L-TFET with Ge-source (GL-TFET), and L-TFET with hetero-gate-dielectric (HL-TFET) are exhibited in Fig. 3. It can be obviously found from Fig. 3 that the GHL-TFET has the better performance than the other L-TFET structures. Compared with the conventional Si-based L-TFET, the I_{ON} of the GHL-TFET is improved by about three orders of magnitude at the same gate overdrive voltage. Although the OFF-current (I_{OFF}) also increases slightly at the same time as the I_{ON} is improved, the GHL-TFET shows a more abrupt ON/OFF transition than the other L-TFET and achieves the minimum SS (28.6 mV/dec) at $V_{gs} = 0.2$ V. The average SS (SS_{avg}), defined as the average inverse slope of the $\log(I_{ds})$–V_{gs} curve over three orders of magnitude change in I_{ds},[23] is 48.7 mv/dec for the GHL-TFET. In addition, the GHL-TFET can effectively suppress the ambipolar current (I_{ambi}) in contrast with the convention L-TFET and the GL-TFET.

For better understanding the unique features of the proposed GHL-TFET, we show in Fig. 4 the diagrams of the nonlocal BTBT tunneling rate, the current density, the potential, and the electric field of the GHL-TFET at $V_{gs} = 1.5$ V and $V_{ds} = 1.0$ V.

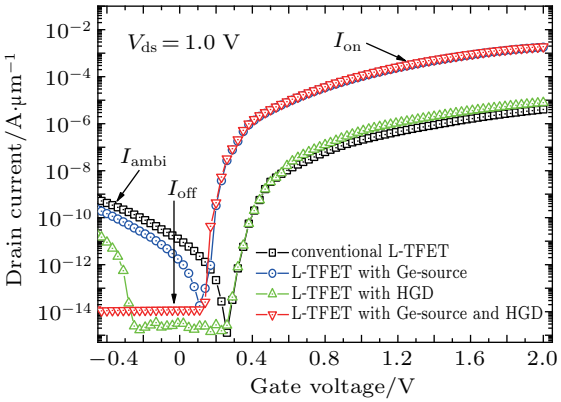


Fig. 3. (color online) Simulated transfer characteristics of the convention L-TFET, L-TFET with Ge-source (GL-TFET), LTFET with heterogeneous gate dielectrics (HL-TFET), and GHL-TFET.

The tunneling electrons are mainly generated in the vertical intrinsic channel as shown in Fig. 4(a). It can be obviously seen from Fig. 4(b) that the current is flowing along the L-shaped channel. Further, because of the asymmetric structure of the GHL-TEFT, which has the L-shaped gate with hetero-gate-dielectric, the OFF-state leakage tunneling (ambipolar) current from the source to drain is suppressed. As shown in Fig. 4(c), the L-shaped body produces the potential contour. Figure 4(d) indicates that the electric field is mainly distributed in the source-channel tunneling junction and the ON-state tunneling current is further increased.

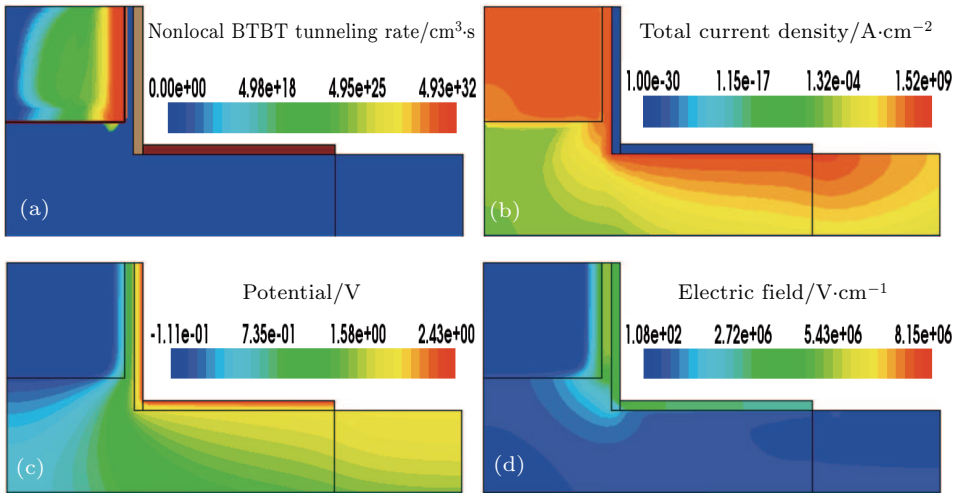


Fig. 4. (color online) Simulated diagrams of (a) BTBT electron tunneling rate, (b) current density, (c) potential, and (d) electric field of the GHL-TFET at $V_{gs} = 1.5$ V and $V_{ds} = 1.0$ V.

3.1. ON-state current performance

The ON-state current of the TFET is related to the material parameters of the source region and the gate dielectric. The transfer characteristics of the L-TFET with low-κ dielectric, L-TFET with high-κ dielectric, L-TFET with Ge-source and low-κ dielectric, and L-TFET with Ge-source and high-κ dielectric are shown in Fig. 5 and the I_{ds}–V_{gs} curves are shifted horizontally to allow easier comparison.

It can be observed in Fig. 5 that the L-TFET with the Ge-source and the high-κ gate dielectrics achieves the largest I_{ON} and the conventional Si-based L-TFET with the low-κ gate dielectrics has the lowest I_{ON}. The most important reason for the enhanced I_{ON} is the introduction of the Ge-source, which forms the Ge/Si heterostructure at the interface between the source and channel to achieve a smaller tunneling barrier. To clearly understand the working mechanism, the energy band diagrams of the GL-TFET and the conventional L-TFET are

presented in Fig. 6.

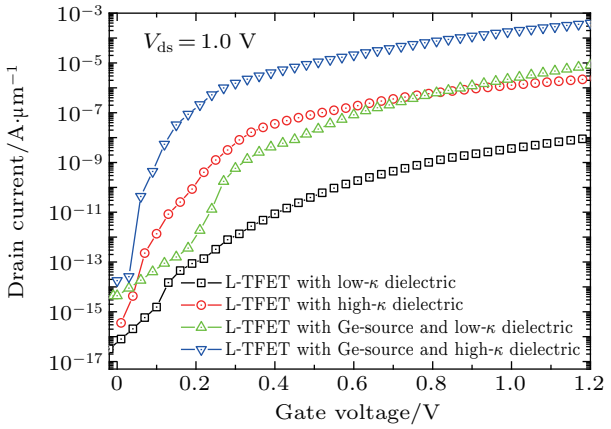


Fig. 5. (color online) Simulated transfer characteristics of the L-TFET with low-κ dielectric, L-TFET with high-κ dielectric, L-TFET with Ge-source and low-κ dielectric, and L-TFET with Ge-source and high-κ dielectric. The curves are shifted so that the gate voltage where the steepest sub-threshold slope occurs is at the origin.

In the ON-state ($V_{gs} = 1.0$ V, $V_{ds} = 1.0$ V), the increased gate voltage makes the energy bands overlap between the source region and channel region and produces a tunneling current. Due to the low band gap of Ge, the Ge-source design reduces the tunneling barrier width as shown in Fig. 6. The smaller tunneling width in GL-TFET ensures more probability of tunneling of charge carrier and larger tunneling area, thereby, higher I_{ON}. The distributions of BTBT tunneling rate of the GL-TFET and L-TFET shown in Fig. 7 further demonstrate the enhanced performance.

In addition, the application of the high-κ dielectric can further improve I_{ON} as shown in Fig. 5. Using the high-κ gate dielectric in the GL-TFET can increase the electric field at the source-channel tunneling junction because of the improved control capability of the gate voltage, which results in the reduction of the tunneling width at the source/channel

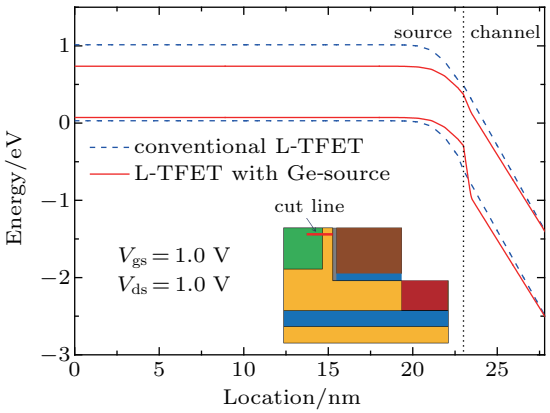


Fig. 6. (color online) Simulated energy band diagrams of the conventional L-TFET and GL-TFET cutting from the source to the channel region.

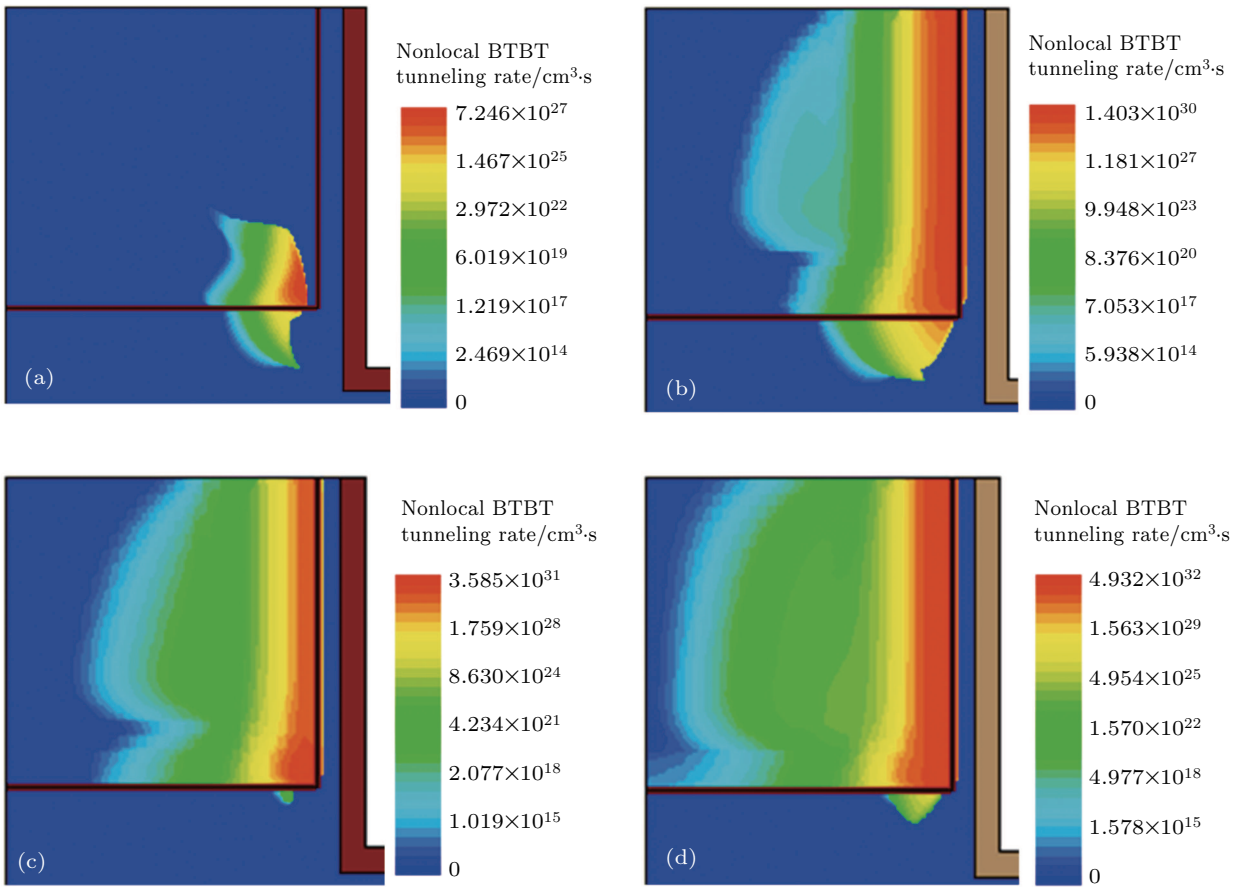


Fig. 7. (color online) Simulated distributions of BTBT tunneling rate of (a) L-TFET with low-κ dielectric, (b) L-TFET with high-κ dielectric, (c) L-TFET with Ge-source and low-κ dielectric, (d) L-TFET with Ge-source and high-κ dielectric at $V_{ds} = 1.0$ V and $V_{gs} = 1.0$ V.

interface.[33] The high-κ dielectric favors an increased tunneling rate that leads to enhancement in I_{ON}, which can be seen in Fig. 7. Therefore, the GL-TFET with high-κ dielectric achieves a further significant improvement in I_{ON} due to the combined effort made by the Ge-source and high-κ dielectric gate material.

In order to further improve the ON-state current, we investigate the impact of variations in the thickness of the vertical intrinsic Si channel (T_{tunl}). There are two necessary conditions to induce band-to-band tunneling in TFET. First, the E_V of the source region should be aligned with E_C of the channel. Second, the tunneling barrier width (W_t) between E_V and E_C should be small enough to achieve band-to-band tunneling because the tunneling probability exponentially depends on W_t.[38] Different from the conventional TFETs whose W_t is determined by the junction depletion width, the W_t of the L-TFET is determined by T_{tunl} that the thickness of an intrinsic or lightly doped tunnel region located between the source and gate dielectrics once the E_V of the source region is aligned with the E_C of the channel region.[22] It means that the I_{ON} of the GL-TFET is related to T_{tunl} which is controlled by the fabrication process. In order to analyze the effect of T_{tunl} on the performance of the GL-TFET in more detail, the I_{ds}–V_{gs} curves for different T_{tunl} are shown in Fig. 8.

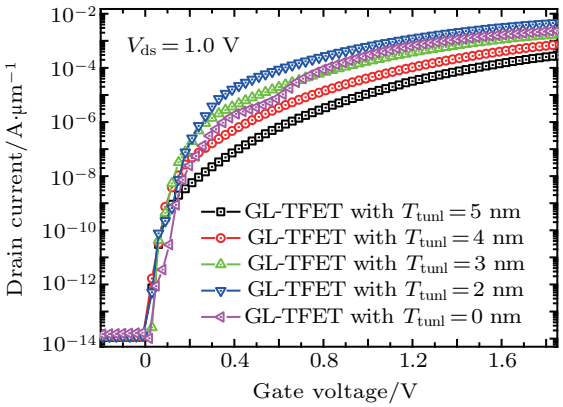


Fig. 8. (color online) Simulated transfer curves of the GL-TFET with different channel thicknesses T_{tunl} at $V_{ds} = 1.0$ V. The curves are shifted so that the gate voltage where the steepest sub-threshold slope occurs is at the origin.

It can be clearly seen from Fig. 8 that the I_{ON} improves as T_{tunl} decreases from 5 nm to 0 nm. When T_{tunl} is large, even if the E_V of the source region is aligned with the E_C of the channel region, W_t is still large, which leads to low tunneling rate and ON-current. With T_{tunl} decreasing, W_t becomes smaller as long as the E_V is aligned with the E_C, thereby, higher ON-current and lower *SS* can be obtained. However, when T_{tunl} further reduces, it becomes more difficult to make the E_V of the source region aligned with the E_C of the channel region.[22] Especially, when T_{tunl} is 0 nm, the large gate–source overlap results in the formation of an inversion layer in the heavily doped Ge-source as the V_{gs} increases, which leads to a high vertical tunneling current.[39] Unfortunately, the heavily doped Ge-source also has an adverse effect on the carrier mobility. As shown in Fig. 8, although the GL-TFET has the higher ON-current at $T_{tunl} = 0$ nm than that at $T_{tunl} > 3$ nm, it still cannot reach the performance at $T_{tunl} = 2$ nm. Therefore, it is determined that the optimum T_{tunl} is 2 nm.

3.2. Ambipolar effect

The introduction of the hetero-gate-dielectric in the GHL-TFET can help suppress the ambipolar effect. Figure 9 compares the transfer characteristics among the GHL-TFET, the GL-TFET with only SiO_2 gate dielectric, and the GL-TFET with only HfO_2 gate dielectric.

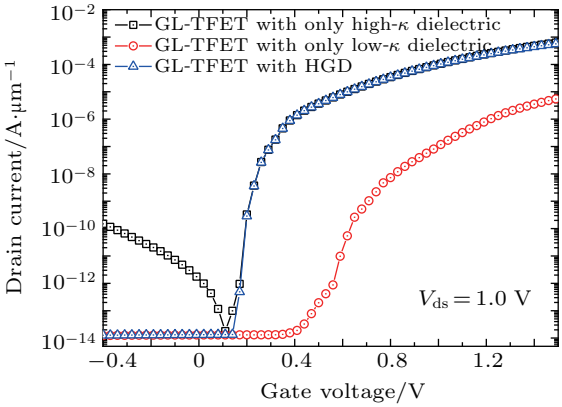


Fig. 9. (color online) Simulated transfer characteristics of the GL-TFET with HGD (GHL-TFET), the GL-TFET with only low-κ gate dielectric, and the GL-TFET with only high-κ gate dielectric.

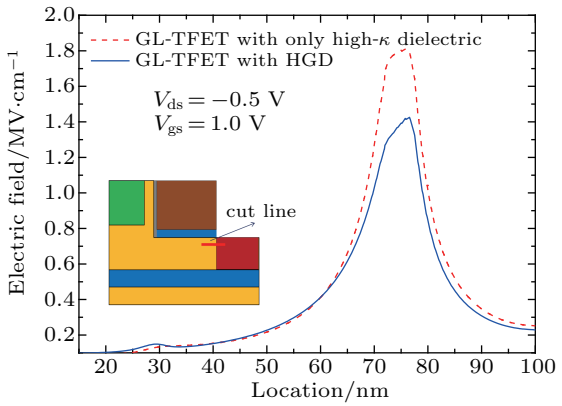


Fig. 10. (color online) Simulated electric fields diagrams of the GHL-TFET and GL-TFET with high-κ dielectric cutting from the channel to drain region.

It is obvious that the GHL-TFET follows the GL-TFET with SiO_2 dielectric at low V_{gs} and the GL-TFET with HfO_2 dielectric at high V_{gs}. It is because the ON-state is determined at the source-to-channel region with the HfO_2 gate dielectric, whereas the OFF-state ambipolar behavior is determined at the drain-to-channel region overlapped by SiO_2. Figure 10 shows the electric field variations along the lateral position

of the GHL-TFET and GL-TFET with high-κ dielectric at $V_{gs} = -0.5$ V and $V_{ds} = 1$ V.

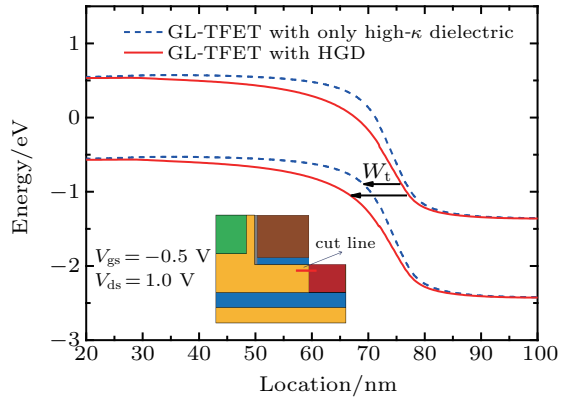


Fig. 11. (color online) Simulated energy band diagrams of the GHL-TFET and GL-TFET with high-κ dielectric cutting from the channel to drain region.

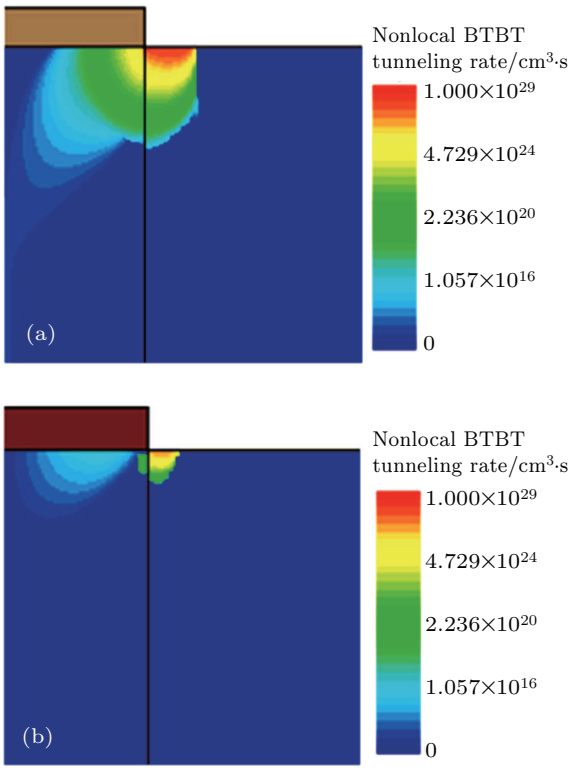


Fig. 12. (color online) Simulated distributions of BTBT tunneling rate of (a) GL-TFET with high-κ dielectric, (b) GHL-TFET at $V_{ds} = 1.0$ V and $V_{gs} = -1.0$ V.

It indicates that using the hetero-gate-dielectric in the GL-TFET can reduce the electric field intensity at the drain adjacent section of the channel region and then modify the band energy structure. Therefore, as shown in Fig. 11, the GHL-TFET has larger tunneling barrier width at the drain/channel interface than the GL-TFET with high-κ dielectric, which will suppress the flow of minority carriers from the conduction band of the drain to the valence band of the source. To further explain this performance, the distribution of BTBT tunneling rate in the OFF-state is compared between the GHL-TFET and the GL-TFET with high-κ dielectric in Fig. 12, which exhibits that the GHL-TFET has a smaller BTBT tunneling rate by using SiO_2 whose relative permittivity is as low as the gate insulator at the drain side. Therefore, the GHL-TFET achieves the lower ambipolar current.

In addition, adjusting the thickness of the gate dielectric can further suppress the ambipolar behavior of the GHL-TFET by effecting the control of the gate over the channel. The tunneling probability is related to the thicknesses of the gate oxides, so we can keep constant the high-κ gate dielectric to maintain the high I_{ON} while modifying the thickness of the low-κ gate oxide T_{ox} to alleviate the ambipolar behavior.[9] Figure 13 shows the I_{ds}–V_{gs} characteristic of the measured GHL-TFETs whose T_{ox} are implemented from 1 nm to 4 nm. Especially, the 6.4 nm HfO_2 gate dielectric which means the 1 nm equivalent oxide thickness (EOT) is used in this simulation.

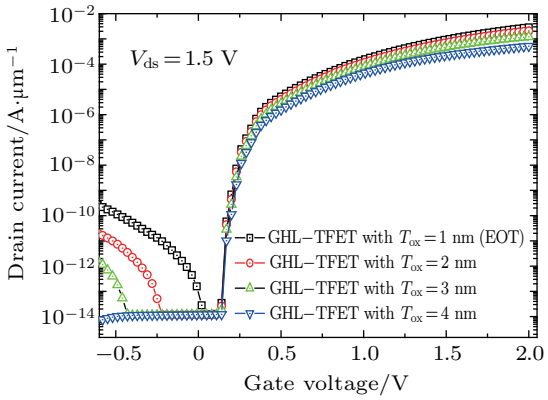


Fig. 13. (color online) Simulated transfer curves of the GHL-TFET with different SiO_2 gate dielectric thicknesses (T_{ox}) at $V_{ds} = 1.5$ V.

It can be seen that the GHL-TFET with small T_{ox} exhibits a high ambipolar current because of the large gate leakage current. When T_{ox} increases, the ambipolar current is significantly suppressed, which is attributed to the reduced electrical coupling between the gate and the drain due to the decreased gate-to-drain capacitance. However, the ON-current also declines slightly at the same time as the ambipolar current decreases. Therefore, there is a trade-off between the ON-current and ambipolar current with the variation of T_{ox} which are suitable for low operating power applications. When T_{ox} is 4 nm, the GHL-TFET can further suppress the ambipolar behavior with a relatively large ON-current.

3.3. RF performance

For analog circuit applications, transconductance g_m is a key parameter to represent the amplification ability of a device and is defined as the slope of the I_{ds}–V_{gs} characteristics. The g_m of a device strongly depends on the drain current, and the TFET with the higher drain current has a higher g_m.[35] Figure 14 shows the g_m characteristics of the L-TFET, GL-TFET,

HL-TFET, and GHL-TFET as a function of the gate bias at $V_{ds} = 1.0$ V.

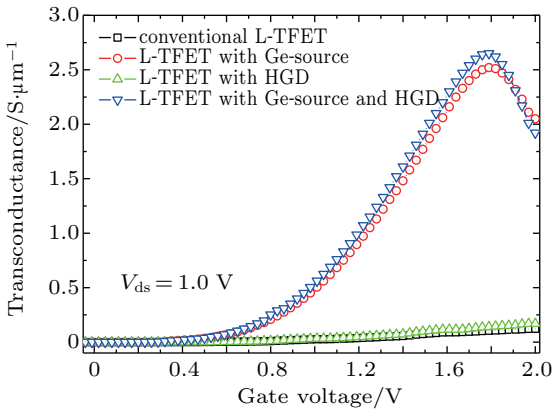


Fig. 14. (color online) Variation of transconductance in the L-TFET, GL-TFET, HL-TFET, and GHL-TFET at $V_{ds} = 1.0$ V.

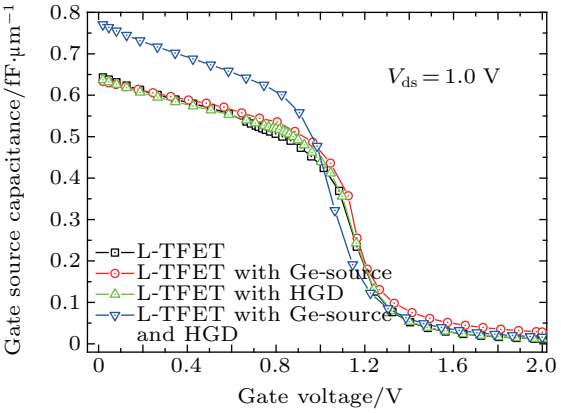


Fig. 15. (color online) Variation of the gate-to-source capacitance in the L-TFET, GL-TFET, HL-TFET, and GHL-TFET at $V_{ds} = 1.0$ V.

Because the GHL-TFET has the maximum drain current shown in Fig. 3, it has the largest g_m. The gate–source capacitance (C_{gs}) and gate–drain capacitances (C_{gd}) are other important parameters for improving the RF performance, which determine the amplification ability of the analog circuits and the switching frequency of the digital circuits. For TFETs, in the ON-state, the C_{gd} represents the entire gate capacitance and the C_{gs} remains very small due to the tunneling barrier of the source. Figures 15 and 16 show the C_{gs} and C_{gd} capacitances characteristics of the GHL-TFET and other L-TFETs. The C_{gs} decreases and keeps very small due to the presence of the tunnel barrier of the source-to-gate region as V_{gs} increases. However, because of the smaller tunneling barrier and largely increasing tunneling rate, the C_{gs} of the GHL-TFET is slightly higher than that of the other L-TFETs shown in Fig. 15. Figure 16 indicates that the C_{gd} increases with V_{gs} for all the measured TFETs, which is attributed to the reduction in the channel-to-drain potential barrier. Consequently, C_{gd} is the dominant gate capacitance component. In addition, the GHL-TFET has smaller C_{gd} by employing the heterogeneous gate dielectric to reduce the capacitive coupling between the drain and gate.

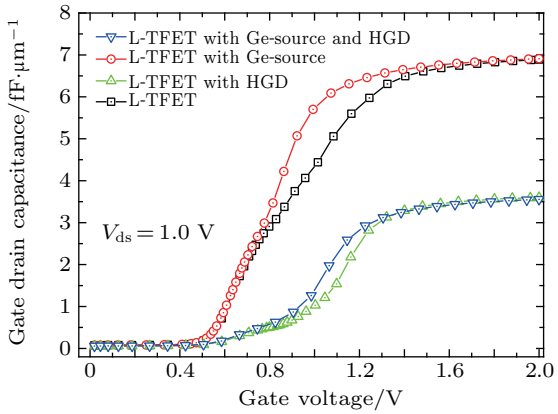


Fig. 16. (color online) Variation of the gate-to-drain capacitance in the L-TFET, GL-TFET, HL-TFET, and GHL-TFET at $V_{ds} = 1.0$ V.

Additionally, cut-off frequency f_T and gain bandwidth product W_{GB} are also vital figures of merit to evaluate the frequency performance of the GHL-TFET for RF applications. The f_T determines the maximum frequency that the device can amplify and is defined as

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)}. \tag{1}$$

The f_T entirely depends on the ratio of transconductance and total capacitance. It can be observed from Fig. 17 that the GHL-TFET has significantly enhanced f_T due to its larger g_m and lower gate capacitances ($C_{gs} + C_{gd}$) compared with those of the other L-TFET.

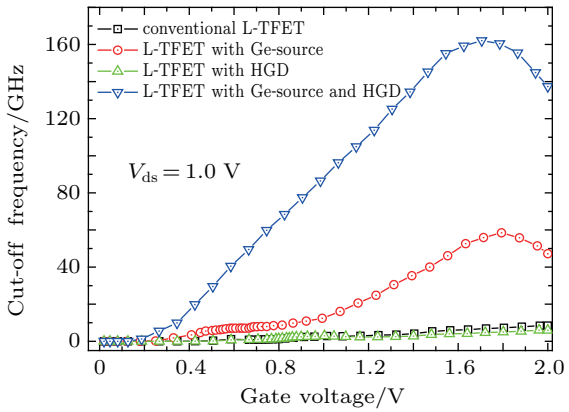


Fig. 17. (color online) Variation of the cut-off frequency in the L-TFET, GL-TFET, HL-TFET, and GHL-TFET at $V_{ds} = 1.0$ V.

For a certain DC voltage gain of 10, the W_{GB} is defined as

$$W_{GB} = \frac{g_m}{2\pi 10 C_{gd}}, \tag{2}$$

which is directly proportional to g_m/C_{gd}. As shown in Fig. 18, the variation tendencies of the W_{GB} are the same as that of f_T, which increases with increased V_{gs} due to a significant improvement in g_m while decreases at higher V_{gs} due to parasitic

capacitances. The GHL-TFET achieves the largest W_{GB} because of the larger g_m and smaller C_{gd}.

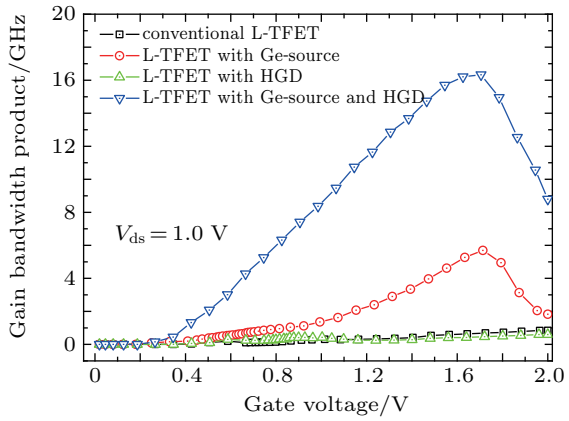


Fig. 18. (color online) Variation of the gain bandwidth product in the L-TFET, GL-TFET, HL-TFET, and GHL-TFET at $V_{ds} = 1.0$ V.

4. Conclusion

In this paper, a Ge/Si heterojunction L-shaped tunnel FET combined with hetero-gate-dielectric is proposed and investigated. For the GHL-TFET, the Ge/Si heterojunction between the source and channel reduces the tunneling barrier, resulting in an increased tunneling rate and a significantly enhanced ON-current. The hetero-gate-dielectric can effectively suppress the ambipolar current of the GHL-TFET. Moreover, the proposed GHL-TFET shows superior RF performance, in terms of the higher g_m, f_T, and W_{GB} as well as lower parasitic capacitances. In conclusion, GHL-TFET exhibits larger ON-current, better suppression of ambipolar effect, and better analog/RF performance compared with conventional L-TFET, which makes GHL-TFET a more promising alternative for low-power and high-frequency integrated circuits.

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