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Enhancement of off-state characteristics in junctionless field effect transistor using a field plate*

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In this paper, a novel junctionless field effect transistor (JLFET) is proposed. In the presence of a field plate between gate and drain, the gate-induced drain leakage (GIDL) effect is suppressed due to the decrease of lateral band-to-band tunneling probability. Thus, the off-state current I_{off}, which is mainly provided by the GIDL current, is reduced. Sentaurus simulation shows that the I_{off} of the new optimized JLFET is reduced by ~ 2 orders and its sub-threshold swing can reach 76.8 mV/decade with little influence on its on-state current I_{on}, so its I_{on}/I_{off} ratio is improved by 2 orders of magnitude compared with that of the normal JLFET. Optimization of device parameters such as Φ_{fps} (the work difference between field plate and substrate) and L_{FP} (the length of field plate), is also discussed in detail.

Keywords: lateral band to band tunneling, GIDL, off-state current, field plate

PACS: 74.55.+v, 85.30.Tv, 85.30.De **DOI:** 10.1088/1674-1056/27/6/067402

1. Introduction

In the down-scaling approach, conventional Si metallic-oxide semiconductor field-effect transistors (MOSFETs) are approaching towards the end of the technology roadmap.[1–3] One of the main reasons is that the rapid down-scaling of conventional bulk MOSFETs below 45 nm requires an ultrasteep doping profile at the metallurgical junction and a high thermal budget corresponding to the post-anneal dopant activation,which leads to extreme troubles in device fabrication.[4,5] To overcome this limitation, various alternative devices are being proposed, and a new class of field effect device called the junctionless field-effect transistor (JLFET) has attract lots of research attention in recent years.[6–14]

The basic structure of a JLFET consists of a uniformly highly doped silicon channel controlled by at least an on gate electrode. Unlike "regular" junction-based FETs, in JLFET, both the source and the drain have the same type of doping as the channel, and there is no pn junction. The principle of JLFET operation is also quite different as it counts on majority carriers instead of minority carriers. Moreover, the current flows mainly in the volume and is no longer confined at the Si/SiO_2 interface. Based on these specific conduction mechanisms, JLFET has a large on-state current I_{on} and an excellent drive capability, which could be improved by increasing the doping concentration.

However, high doping will increase not only the on-state current I_{on} but also the off-state current I_{off}, thus affecting the ratio of I_{on} over I_{off}.[15–17] Furthermore, above certain doping levels, the device could not be switched off even at the off state of the device. As in conventional MOSFET, the off-state current I_{off} in JLFET is mainly caused by the gate-induced drain leakage (GIDL) effect at the gate edge between gate and drain.[18–20] Since the efficient gate control over the channel region leads to a considerable overlap of the valence band with the conduction band at the channel–drain interface, a lateral band-to-band tunneling (L-BTBT) of electrons from the channel region to the drain region in the off-state ($V_{GS} = 0$ V), which is a dominant mechanism for GIDL in JLFET. In order to reduce I_{off}, several device structures have been designed, such as JLFET with dielectric pocket double gate,[21] JLFET with hybrid channel,[22] JLFET with core-shell architecture,[23] etc.

In this paper, we propose a novel JFELT with field plate structure to reduce the high field effect at the gate edge, finally suppressing the GIDL effect and I_{off}. The TCAD simulation indicates that I_{off} of the new optimized JLFET is reduced by ~ 2 orders and its sub-threshold swing can reach 76.8 mV/decade with little affection on its I_{on}, so its I_{on}/I_{off} ratio is improved by 2 orders of magnitude over the normal JLFET. Optimization of device parameters such as Φ_{fps} (the work difference between field plate and Si) and L_{FP} (the length of field plate) is also discussed in detail.

2. Device structure and simulation parameters

The schematic views of the conventional MOSFET, the normal JLFET, and the novel JFLET (FP JLFET) are shown

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in Figs. 1(a)–1(c), respectively. The length of the gate, length of the field plate, thickness of the oxide, and thickness of channel are denoted as L_{ch}, L_{FP}, t_{ox}, and t_{ch}. The channels of the JLFET and the FP JLFET are lightly doped (1×10^{17} cm^{-3}), the drain and source are heavily doped (1×10^{19} cm^{-3}). The metal of the gate electrode is Cr/Au for ensuring the device to be fully depleted at $V_{GS} = 0$ V. The high-k material of HfO_2 is used as gate dielectric and field plate dielectric. The field plate in FP JLET shown in Fig. 1(c) is located between gate and drain electrodes. In order not to affect the device size, the length of field plate L_{FP} cannot be longer than the distance between gate and drain electrodes.

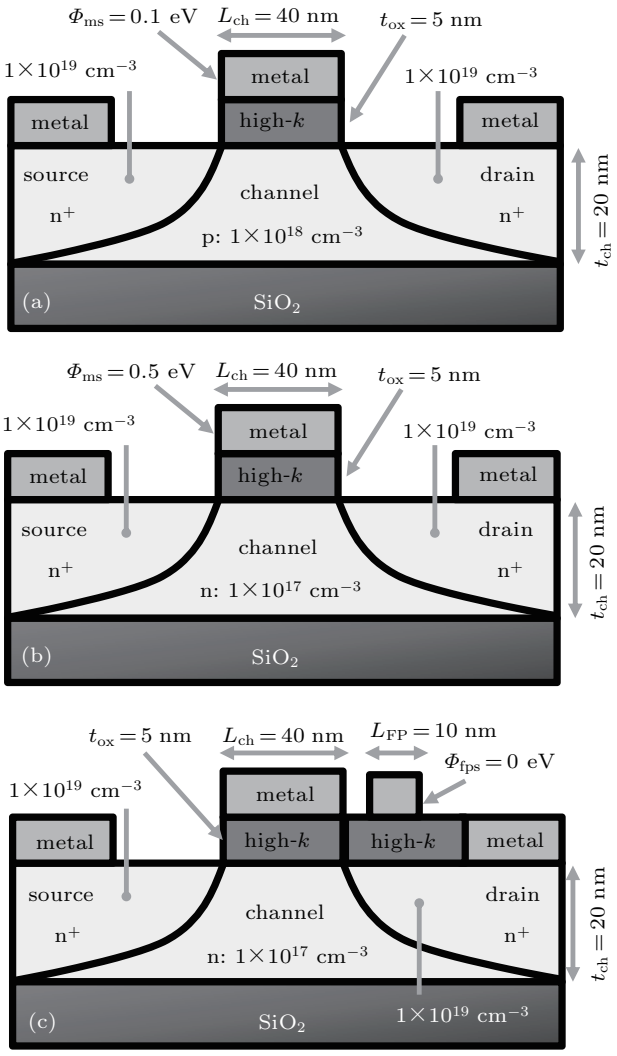


Fig. 1. Cross sections of (a) conventional MOSFET, (b) normal JLFET, and (c) FP JLFET.

Sentaurus TCAD was used to perform the device simulations. The field-dependent and doping dependent mobility degradations were considered using the Philips unified mobility model and Lombardi mobility model. Bandgap narrowing, Shockley–Read–Hall, the Auger recombination model, and Fermi–Dirac statistics were also involved. A nonlocal BTBT model was used to account for the lateral tunneling of the GIDL effect. A temperature of 300 K was employed in simulations.

3. Simulation results and discussion

Figure 2 shows the electric field underneath the gate of normal JLFET and FP JLFET. To make a comparison, the electric field curve of conventional MOSFET is also given in this experiment. Owing to the capacitive coupling effect,[24–26] the peak of the electric field at the edge of the gate decreases significantly and a relatively low peak of electric field is created at the edge of the field plate, thus leading to a larger tunneling width in FP JLFET as shown in Fig. 3.

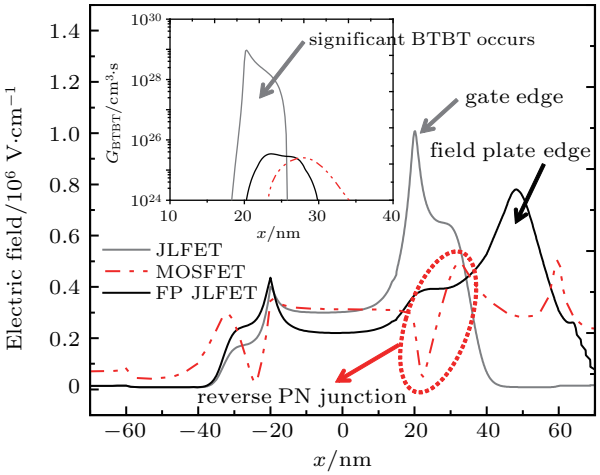


Fig. 2. (color online) Plots of electric field along the vertical direction of the channel underneath the gate in the off-state ($V_{DS} = 1.0$ V, $V_{GS} = 0$ V), with inset showing G_{BTBT} near the gate edge.

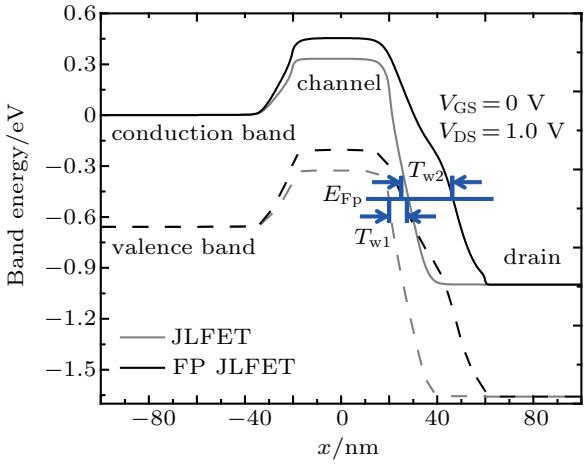


Fig. 3. (color online) Energy bands along the parallel directions of channels of JLFET and FP JLFET underneath the gate, in off-state ($V_{DS} = 1.0$ V, $V_{GS} = 0$ V).

Figure 3 shows a comparison of energy band structure along the parallel channel direction between normal JLFET and FP JLFET at the surface. The E_{Fp}, T_{w1}, and T_{w2} represent the Fermi energy level, and the tunneling width of normal JLFET and FP JLFET respectively. As discussed above, the electric field between gate and drain in FP JLFET is more uniform by employing the field plate structure, leading to the decrease of band bending of FP JLFET compared with that of JLFET.Therefore, T_{w2} is larger than T_{w1}. An enhanced tunneling width leads to the decrease of the electrons tunneling

from the channel region to the drain region, resulting in a significantly reduced BTBT generation rate in the new FP JLFET compared with that in the normal JLFET as shown in the inset of Fig. 2.

The transfer characteristics of the new FP JLFET and normal JLFET ($V_{DS} = 1$ V) are shown in Fig. 4. To show the advantages of FP JLFET more obviously, the I_D–V_G curve of conventional MOSFET is also given in this experiment. We can observe that the off-state current I_{off} of normal JLFET with the BTBT model increases more than 3 orders of magnitude (from 9.25×10^{-11} A/μm to 5.7×10^{-7} A/μm), indicating that I_{off} is mainly caused by the GIDL effect. With the field plate employment, the I_{off} is drastically reduced in the FP JLFET by 2 orders of magnitude compared with that of normal JLFET, resulting in an improvement in its sub-threshold swing SS as shown in Fig. 4(b).

Also from Fig. 4, we can observe that the values of on-state current I_{on} of JLFET and FP JLFET are at the same level, since the field plate structure has little effect on the on-state current I_{on}, which is mainly composed of the drifting current of majority carriers. Thus, the I_{on}/I_{off} ratio of FP JLFET has a more apparent improvement than that of JLFET, almost being at the level of a conventional MOSFET and manifesting the advantages of FP JLFET.

To study the influence of Φ_{fps} on GIDL and the electrical characteristics of FP JLFET, the I_D–V_G curves with various values of Φ_{fps} were simulated as shown in Figs. 5(a) and 5(b). Since the increase of Φ_{fps} enhances the repelling effect on electrons, the electron density decreases at the surface of FP JLFET with Φ_{fps} increasing, finally reducing the on state current I_{on} of the device.

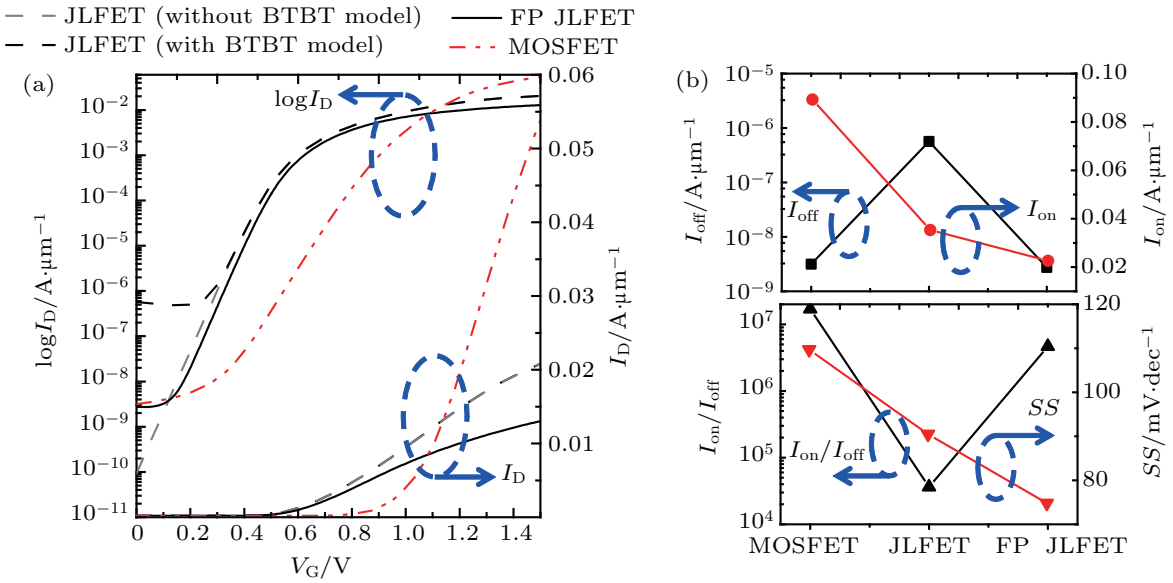


Fig. 4. (color online) (a) I_D–V_G characteristics of conventional MOSFET, normal JLFET, and FP JLFET at $V_{DS} = 1.0$ V. (b) Comparisons of I_{on}, I_{off}, I_{on}/I_{off}, and SS among conventional MOSFET, normal JLFET, and FP JLFET.

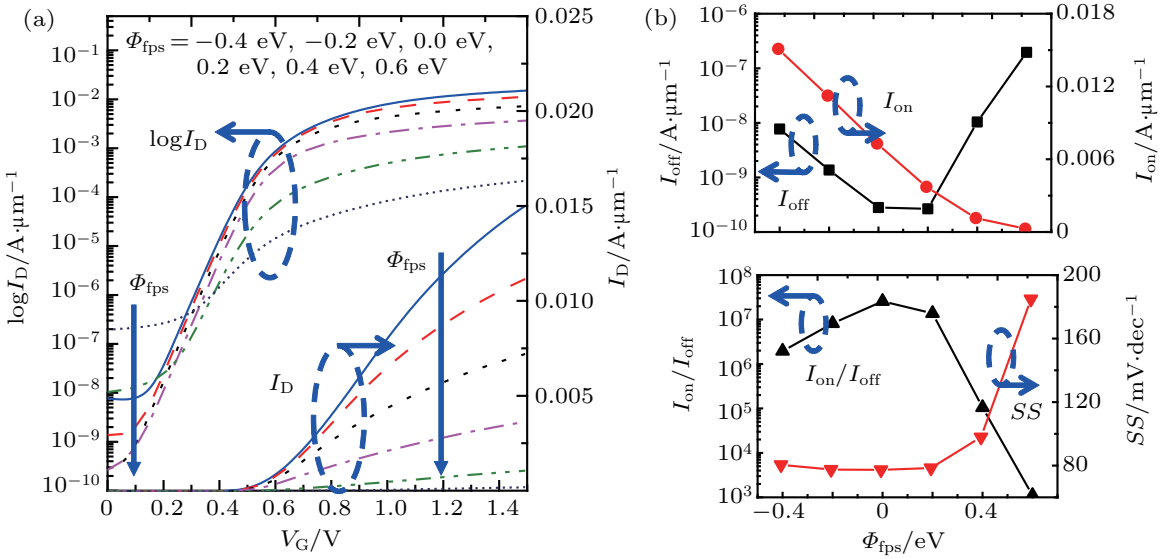


Fig. 5. (color online) (a) I_D–V_G characteristics of the FP JLFET with various values of Φ_{fps} ($\Phi_{fps} = -0.4$ eV, -0.2 eV, 0.0 eV, 0.2 eV, 0.4 eV, 0.6 eV) at $V_{DS} = 1.0$ V. (b) Comparisons of I_{on}, I_{off}, I_{on}/I_{off}, and SS of the FP JLFET with various values of Φ_{fps}.

Also from Fig. 5, we can see that I_{off} first decreases and then increases with Φ_{fps} increasing. As Φ_{fps} increases from -0.4 eV to 0.0 eV, I_{off} decreases from 7.71×10^{-9} A/μm to 2.81×10^{-10} A/μm, and as Φ_{fps} increases from 0.0 eV to 0.6 eV, I_{off} increases about 3 orders of magnitude (from 2.81×10^{-10} A/μm to 1.96×10^{-7} A/μm). Therefore, the I_{on}/I_{off} ratio first increases and then decreases with Φ_{fps} increasing, and the optimal I_{on}/I_{off} and SS are achieved when $\Phi_{fps} = 0.0$ eV as shown in Fig. 5(b).

To understand the phenomenon above, the energy bands along the parallel direction of the FP JLFET with various values of Φ_{fps} ($\Phi_{fps} = -0.4$ eV, 0.0 eV, and 0.4 eV) in the off-state are examined as shown in Fig. 6. T_I, T_{II}, and T_{III} are the width of the tunneling barrier of the GIDL effect with $\Phi_{fps} = -0.4$ eV, 0.0 eV, and 0.4 eV, respectively. It is obvious that the T_{II} is largest, which ensures the optimal value of off state current I_{off}. Besides, the position of the tunneling barrier shifts from gate edge to field plate edge with Φ_{fps} increasing. The reason is as follows. The density of electrons under the field plate decreases with Φ_{fps} increasing and finally the holes will be accumulated at the surface under the field plate, resulting in the p+ region extending from the gate edge to the floating plate edge, which is shown in the inset of Fig. 6. Thus, the tunneling position shifts. Owing to the two reasons discussed above, the optical value for Φ_{fps} is chosen to be 0 eV in our simulations.

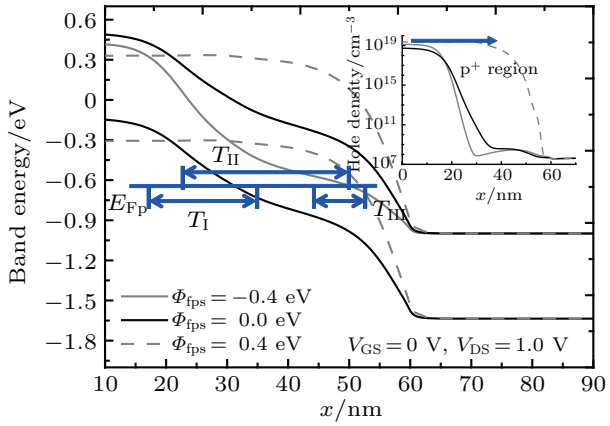


Fig. 6. (color online) Energy bands along the parallel direction of FP JLFET with various values of Φ_{fps} ($\Phi_{fps} = -0.4$ eV, 0.0 eV, 0.4 eV underneath the gate, in the off-state ($V_{DS} = 1.0$ V, $V_{GS} = 0$ V), with inset showing hole density along the parallel direction.

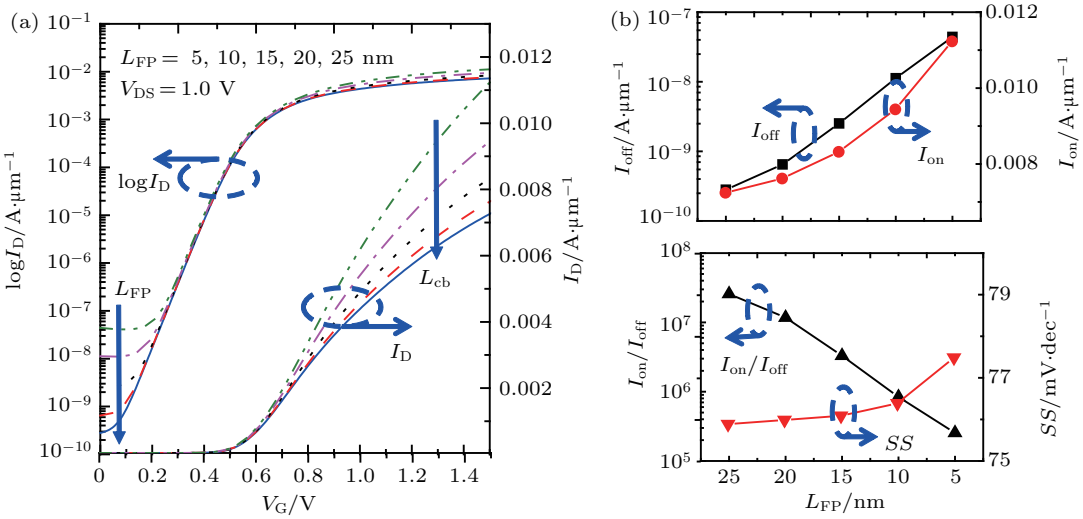


Fig. 7. (color online) (a) I_D–V_G characteristic curves of FP JLFET with various values of L_{FP} at $V_{DS} = 1.0$ V. (b) Comparisons of I_{on}, I_{off}, I_{on}/I_{off}, and SS of the FP JLFET with various values of L_{FP}.

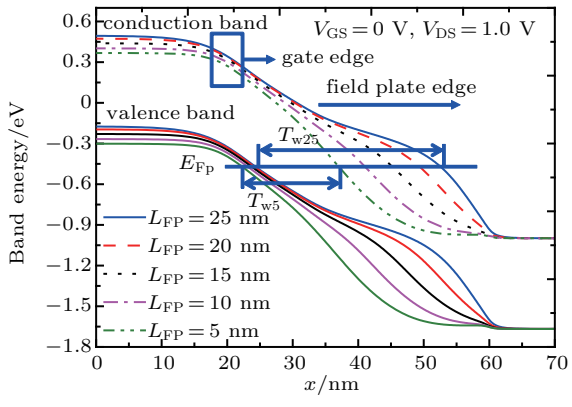


Fig. 8. (color online) Energy bands along the parallel direction of the FP JLFET with various values of L_{FP} underneath the gate, in the off-state ($V_{DS} = 1.0$ V, $V_{GS} = 0$ V).

Another important parameter affecting the off-state current of the FP JLFET is L_{FP}. Figure 7 shows the I_D–V_G curves of FP JLFET with L_{FP} values of 5 nm, 10 nm, 25 nm, 20 nm, and 25 nm. The off-state current I_{off} decreases more than 2 orders of magnitude as L_{FP} increases from 5 nm to 25 nm, resulting in a significant improvement in I_{on}/I_{off} and SS. The reason is shown in Fig. 8. Figure 8 gives the energy band along the parallel direction of the FP JLFET with various values of L_{FP} underneath the gate in the off-state. It is shown obviously that the tunneling width is enlarged with the L_{FP} increasing and reaches its largest value at $L_{FP} = 25$ nm, thus the BTBT tunneling and GIDL effect are restricted, reducing the I_{off} significantly.

4. Conclusions

In this work, we have proposed a JLFET with a field plate for significantly improving the off-state performance. Using Sentaurus simulations, we demonstrate that the field plate in the new device can effectively broaden the tunneling barrier width at the drain-channel interface, resulting in the occurrence of insufficient band bending for L-BTBT and thus restricting the GIDL effect in the new JLFET. Therefore, the proposed device architecture provides the off-state current reduced by 2 orders of magnitude without deteriorating the on-state current, resulting in a significant I_{on}/I_{off} ration enhancement compared with the scenario of the conventional JLFET. Our results may promote the experimental realization of this structure.

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