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Mechanisms of atmospheric neutron-induced single event upsets in nanometric SOI and bulk SRAM devices based on experiment-verified simulation tool*

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In this paper, a simulation tool named the neutron-induced single event effect predictive platform (NSEEP^2) is proposed to reveal the mechanism of atmospheric neutron-induced single event effect (SEE) in an electronic device, based on heavy-ion data and Monte-Carlo neutron transport simulation. The detailed metallization architecture and sensitive volume topology of a nanometric static random access memory (SRAM) device can be considered to calculate the real-time soft error rate (RTSER) in the applied environment accurately. The validity of this tool is verified by real-time experimental results. In addition, based on the NSEEP^2, RTSERs of 90 nm–32 nm silicon on insulator (SOI) and bulk SRAM device under various ambient conditions are predicted and analyzed to evaluate the neutron SEE sensitivity and reveal the underlying mechanism. It is found that as the feature size shrinks, the change trends of neutron SEE sensitivity of bulk and SOI technologies are opposite, which can be attributed to the different MBU performances. The RTSER of bulk technology is always 2.8–64 times higher than that of SOI technology, depending on the technology node, solar activity, and flight height.

Keywords: atmospheric neutron, single event effects, soft error rate, Monte-Carlo simulation

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1. Introduction

Atmospheric neutron-induced single event effects (SEE) in avionics and key ground electronics are gaining increasing attention, due to the fact that the SEE performance of an integrated circuit (IC) becomes worse as the feature size shrinks.[1] Hence, the prediction of real-time neutron-induced SEE sensitivity in the applied environments, especially for nanometric ICs, can be very important for the system reliability insurance.

Based on the JEDEC JESD89A standard,[2] the atmospheric neutron-induced real-time soft error rate (RTSER) can be predicted by real-time (unaccelerated and high-altitude) measurements, accelerated high-energy neutron tests and accelerated thermal neutron tests. Accelerated tests using spallation neutron source, reactor, 14-MeV neutron source, etc. have been widely performed by the community to quickly extrapolate the RTSER of semiconductor devices under ambient conditions. However, there are limited available facilities and also beam time for conducting such accelerated tests, especially for a spallation neutron source as the most convenient one. For the real-time measurements, few publications have been reported by Xilinx,[3,4] Intel,[5] the French Aerospace Lab,[6] and so on, due to the fact that real-time resting can be very time-consuming, lacking in statistic, and expensive. In fact, a neutron induces error indirectly by creating secondary ions following a nuclear reaction with the nucleus of the target. So, heavy ion test data can be used to predict the neutron induced SEE, when added with the neutron–target interaction information, as an effective complement of RTSER prediction techniques.

A prediction tool named a neutron-induced single event effect predictive platform (NSEEP^2) is presented in this work. This platform is dedicated to predicting the neutron-induced SEE cross sections and rates in semiconductor devices, by combining with heavy ion data and neutron transport simulations. The validity of NSEEP^2 is verified by comparing the predicted results with the real-time measurement results. Based on the NSEEP^2 tool, the sensitivity and inner mechanism of atmospheric neutron-induced SEE in nanometric bulk and silicon on insulator (SOI) static random access memory (SRAM) technologies are investigated.

2. Prediction tool and its verification

Prediction steps of NSEEP^2 includes

Step 1 constructing 3D device model;

Step 2 calculating the neutron spectra in the applied environment;

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Step 3 simulating the neutron transport;

Step 4 calculating the event criterion and rate.

In the following, taking 90-nm and 65-nm bulk SRAM technologies for example, the detailed prediction process of NSEEP[2] is shown and also verified.

2.1. Construction of three-dimensional device model

Primary parts of the three-dimensional (3D) device model for neutron-induced SEE prediction include the top metallization layers, sensitive volume (SV) topology, and the substrate or buried oxide (for SOI technology). The structure of top metallization layers can be obtained from the manufacturer or reverse-analysis technique. Figure 1 shows an example of an SEM photo of the top layers of a 65-nm bulk CMOS SRAM technology. In certain cases, the top metallization layers can be simplified by using silica film with an equivalent thickness as depicted in Fig. 2.

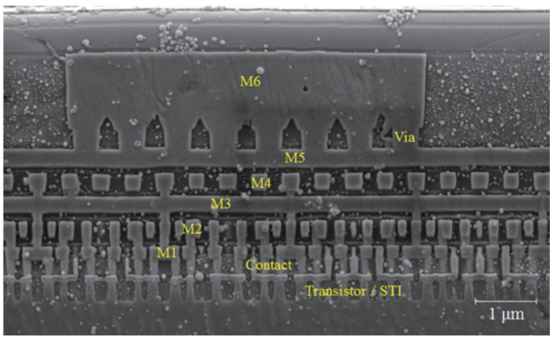


Fig. 1. (color online) Cross section of the metallization of a 65-nm bulk CMOS SRAM technology.

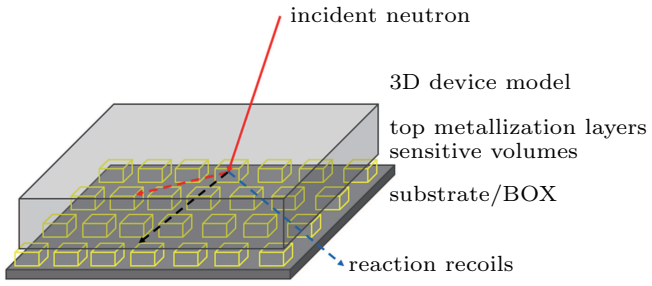


Fig. 2. (color online) Diagram of the NSEEP[2] predictive process.

The 3D topological structure of sensitive volumes, as shown in Fig. 2, can be obtained by heavy-ion data, and verified by using the reverse-analysis results. Main parameters include the length (x), width (y), depth (z), and critical charge (Q_c) of the sensitive volume. Besides, the gap distance between sensitive volumes can be particularly important for multiple-bit upset (MBU) prediction. During the ground heavy-ion accelerator testing, a plot of SEE cross section versus ion LET can be achieved. By further Weibull fitting (see the following formula (1)), four Weibull parameters can be obtained: saturated SEE cross section (σ_{sat}), threshold LET (LET_{th}), width parameter (W), and shape parameter (S). Table 1 presents the Weibull parameters of single event upset (SEU) of BRAMs of the 90-nm and 65-nm bulk FPGAs,[7,8] in which the SRAM architecture is used.

$$\sigma(\mathrm{LET}) = \sigma_{sat}\left(1-\exp\left\{-\left[(\mathrm{LET}-\mathrm{LET}_{th})/W\right]^{S}\right\}\right). \quad (1)$$

Table 1. Weibull parameters of SEU of BRAMs of the 90-nm and 65-nm bulk FPGAs.[7,8]

Technology node	Weibull parameters			
	σ_{sat}/(cm^2/bit)	LET_{th}/(MeV·cm^2/mg)	W/(MeV·cm^2/mg)	S
90 nm	3.5×10^{-8}	0.2	70	0.724
65 nm	1.15×10^{-7}	0.01	200	0.86

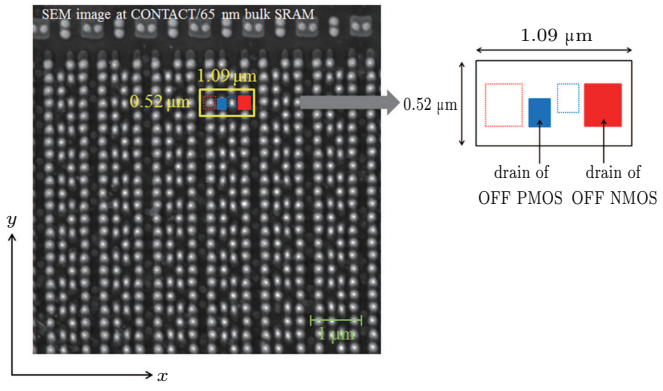


Fig. 3. (color online) SEM image of a 65-nm bulk CMOS SRAM technology at contact layer.

Based on σ_{sat} and LET_{th}, the length, width, and critical charge of sensitive volume can be calculated from the following formulas:

$$x = y = \sqrt{\sigma_{sat}}, \quad (2)$$

$$Q_c = \frac{\mathrm{LET}_{th}\cdot\rho_{Si}\cdot z}{22.5}, \quad (3)$$

where ρ_{Si} denotes the density of the silicon material (232 mg/cm^3), the unit of z is in cm, and the unit of Q_c is in pC. The depth of sensitive volume is usually set to be the thickness of the depletion region.

In addition, dimensions of sensitive volumes can also be extracted by a reverse-analysis technique. As an example, figure 3 shows the SEM image of a 65-nm bulk CMOS SRAM technology at the contact layer. Clear periodical structure can be seen. It can be seen from Fig. 3 that a memory cell is composed of four NMOS transistors and two PMOS transistors. The drains of the off-state PMOS and NMOS transistors are considered to be the sensitive volumes of one memory cell, which have an $x\times y$ scale of 0.2 μm×0.28 μm (NMOS) and

0.12 μm×0.17 μm (PMOS), respectively.

2.2. Calculation of neutron spectrum in applied environment

The neutron spectrum inputting the NSEEP[2] tool can be a mono-energetic neutron spectrum, or atmospheric-neutron spectrum. For the real-time atmospheric soft error rate prediction, the input neutron spectrum should be the actual neutron spectrum in the applied environment. The intensity of an atmospheric-neutron is highly dependent on the altitude, latitude, longitude, and solar activity of the intended location as shown in Figs. 4–6, which is calculated by the Avionics/SE model.[9]

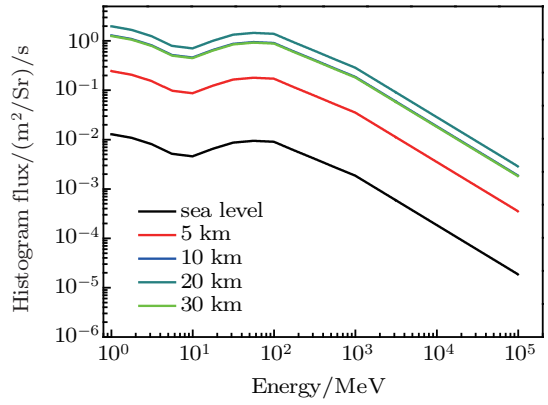


Fig. 4. (color online) Atmospheric neutron spectra of Beijing City in solar minimum condition at different altitudes.

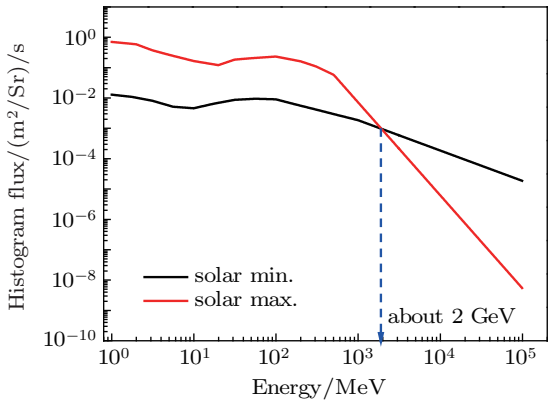


Fig. 5. (color online) Atmospheric neutron spectra of Beijing City at ground, in solar minimum and solar maximum conditions.

In Fig. 4, the atmospheric neutron flux is increased constantly by more than two orders of magnitude as the altitude increases from sea level to 20 km. In Fig. 5, clear difference between atmospheric neutron spectra in solar minimum and solar maximum conditions can be seen. More specifically, for neutron energy below about 2 GeV, neutron flux in the solar maximum condition is obviously higher than that in the solar minimum condition. However, the case is unexpectedly reversed for neutron energy above 2 GeV. This phenomenon can be explained by the fact that compared with the solar minimum condition, the flux of solar protons in the solar maximum condition increases sharply, which results in denser neutron flux after interacting with the atmosphere. While for galactic cosmic rays (GCRs) with higher energy than solar protons, the GCR flux decreases due to the regulation of solar maximum activity. This leads to the decrease of atmospheric neutron flux in the energy range of above GeV. Figure 6 shows the comparison of the atmospheric neutron spectra for different locations in the solar minimum condition, which demonstrates the influences of latitude and longitude on neutron flux.

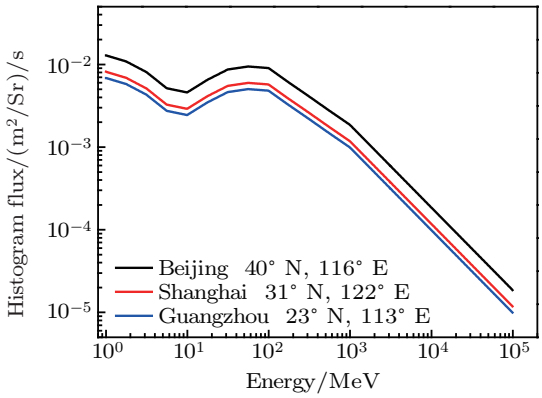


Fig. 6. (color online) Atmospheric neutron spectrums of Beijing, Shanghai, and Guangzhou Cities at ground and in solar minimum condition.

2.3. Neutron transport simulation and event criterion

The interaction of neutrons with the device model is simulated by the Monte-Carlo method. Nuclear processes including elastic and inelastic scattering are considered to extract the interaction recoils, whose transport is further simulated and the energy deposited in sensitive volume, E_d, is recorded. A single event effect occurs when

$$\frac{E_d}{22.5} > Q_c, \tag{4}$$

where the units of E_d and Q_c are MeV and pC, respectively.

2.4. Verification by real-time experiments

Validity of the NSEEP[2] tool is verified by real-time experimental results. Figures 7 and 8 show the simulated RTSERs of BRAMs of the 90-nm and 65-nm FPGAs at the ground of New York City respectively, as a function of the depth of sensitive volume. It can be seen that as the depth of sensitive volume ranges from 0.1 μm to 3 μm, the change of predicted RTSER value is less than one order of magnitude for both 90-nm and 65-nm bulk technologies. This implies the limited influence of depth of sensitive volume on predicted results. Moreover, the real-time experimental results for the 90-nm and 65-nm bulk technologies[4] are indicated in the figures, with a 90% confidence interval. It can be seen that the simulation results of the NSEEP[2] tool agree with the real-time experimental results as the depths of sensitive volume of 90-nm and 65-nm technologies range from 0.49 μm to 0.72 μm, and from 0.28 μm to 0.53 μm, respectively. Note that, to improve the performance of anti-single event latchup, the 90-nm

and 65-nm FPGAs use epitaxial layers, which result into thin sensitive volume. Taking the 65-nm technology for example, the typical depth of sensitive volume is around 0.45 μm, in which the funnel length and diffusion process are also taken into consideration.[10]

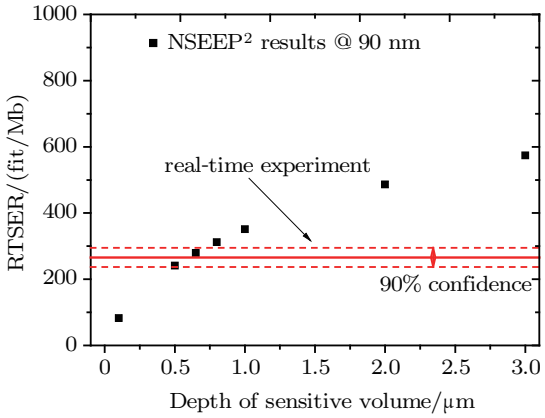


Fig. 7. (color online) RTSER versus depth of sensitive volume of BRAM of 90-nm FPGA at ground of New York City.

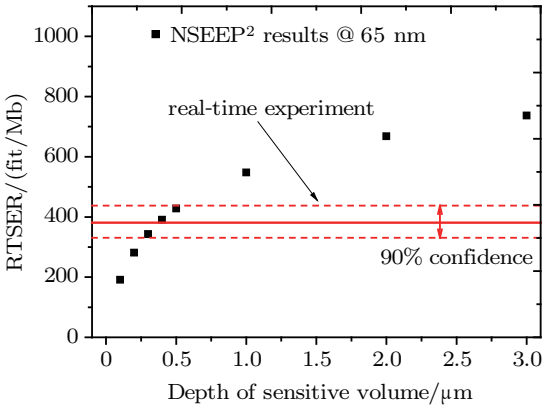


Fig. 8. (color online) RTSER versus depth of sensitive volume of BRAM of 65-nm FPGA at ground of New York City.

3. RTSERs of nanometric bulk and SOI SRAMs

In order to reveal the sensitivities and inner mechanisms of atmospheric neutron-induced SEEs in nanoscale SRAM technologies, the RTSERs under various conditions are predicted and compared with each other for both bulk and SOI technologies. Primary aims are (i) to investigate the change trend of neutron SEE sensitivity with the feature size downscaling, (ii) to compare the neutron SEEs obtained by SOI and bulk technologies, and (iii) to characterize the influences of solar activity and flight height on RTSER quantitatively. Figure 9 shows the plots of RTSER versus technology node of 90-nm–32-nm SOI and bulk SRAMs at ground and 10-km flight height of Beijing City, in solar minimum and maximum conditions. Several conclusions can be drawn as follows.

First, as the technology node shrinks from 90 nm to 32 nm, per-bit RTSER of SOI SRAM decreases continuously by about 97%. However, for bulk technology, it seems that RTSER of 65-nm SRAM is always 31%∼43% higher than that of 90-nm SRAM, depending on the solar activity and flight height. The reason for this different trend lies in the MBU performance. For SOI technology, the existence of shallow trench isolation (STI) and buried oxide (BOX) results in the physical isolation of SVs from each other, which suppresses the charge diffusion process and thus charge sharing effect. In consequence, SOI technology exhibits better MBU resistance than bulk technology. Thus, the constant decrease of neutron SEE sensitivity of SOI technology with feature size downscaling can be attributed to the constant decrease of SV dimensions of SOI SRAMs (see Table 2). However, for bulk technology, the increase of neutron SEE sensitivity with feature size downscaling results from the reduced critical charge and worse MBU performance. This can be concluded from the following: 1) in Table 1, the saturated SEU cross section of 65-nm bulk technology, corresponding to an area of 3.4 μm×3.4 μm, is far larger than the surface area of one SV of 65-nm bulk technology, which implies the MBU effect; 2) the saturated SEU cross section of 65-nm bulk technology is unexpectedly 2.3 times higher than that of 90-nm bulk technology, which implies higher MBU probability of the 65-nm bulk technology; 3) it can be calculated from Table 1 and formula (3) that the critical charge of 65-nm bulk technology (0.1 fC) is more than one order of magnitude smaller than that of 90-nm bulk technology (5×10^{-3} fC).

Table 2. RPP parameters of nanoscale SOI SRAMs.[11–13]

Technology	Surface area of one memory cell/(cm²/bit)	Surface area of SV/(cm²/bit)	Silicon thickness/nm	Critical charge/fC
90 nm/PDSOI	2.4×10^{-8}	1.2×10^{-9}	150	1.5
65 nm/PDSOI	6.25×10^{-9}	3×10^{-10}	60	0.6
45 nm/PDSOI	4×10^{-9}	2×10^{-10}	50	0.5
32 nm/FDSOI	3×10^{-9}	1.4×10^{-10}	40	0.4

Second, the RTSER of bulk technology is always 2.8–64 times higher than that of SOI technology, depending on the technology node, solar activity, and flight height. Comparing Table 1 with Table 2, it can be seen that the inner reasons are smaller SV dimensions (including the surface area and also the depth), larger critical charges, and also better MBU performance of SOI technologies, as previously discussed.

Finally, solar activity and flight height have an obvious influence on the RTSER results, for all feature sizes of SOI and bulk technologies. Depending on the flight height, technology node, and type, the influence of solar activity on the RTSER can be as large as 32–990 times. At 10-km flight height, the

influence of solar activity is magnified. The influence of flight height is also a function of solar activity, technology node, and type, and the influence intensity can be as large as 99–2347 times with the flight height changing from sea level to 10 km.

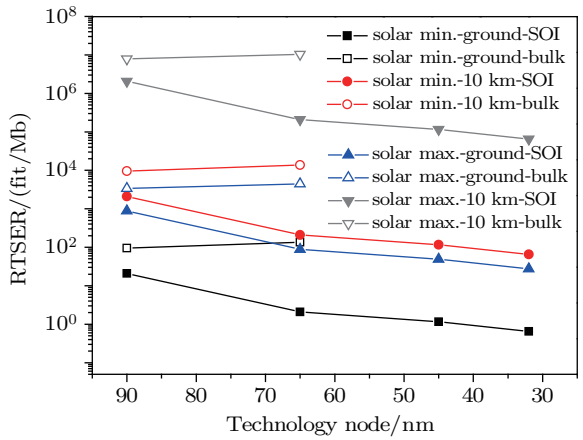


Fig. 9. (color online) Plots of RTSER versus technology node of 90 nm∼32 nm SOI and bulk SRAMs at ground and 10-km flight height of Beijing City, in solar minimum and maximum conditions.

4. Conclusions

In this paper, we present a simulation tool named NSEEP[2], which is dedicated to calculating neutron-induced SEE cross sections and rates in semiconductor devices, by combining heavy ion data with neutron transport simulations. Prediction steps of NSEEP[2] include construction of a 3D device model, obtaining the neutron spectrum in the applied environment, neutron transport simulations, and finally event criterion and rate calculation. The validity of this tool is verified by real-time experimental results.

In addition, the RTSERs of 90 nm–32 nm SOI and bulk SRAMs at ground and 10-km flight height of Beijing City, in solar minimum and maximum conditions, are predicted and analyzed. It is found that with feature size shrinking, the change trends of neutron SEE sensitivity of bulk and SOI technologies are opposite, which can be attributed to different MBU performances. The RTSER of bulk technology is always 2.8–6.4 times higher than that of SOI technology, depending on the technology node, solar activity, and flight height. Moreover, solar activity and flight height have an obvious influence on the RTSER results.

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