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Research on the radiation hardened SOI devices with single-step Si ion implantation

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Silicon-on-insulator (SOI) devices are sensitive to the total ionizing dose effect due to the existence of buried oxide. In this paper, an extra single-step Si ion implantation into buried oxide layer prior to the normal complementary metal–oxide–semiconductor transistor (CMOS) process is used to harden the SOI wafer. The top-Si quality of the hardened SOI wafer is confirmed to be good enough for device manufacturing through various characterization methods. The radiation experiments show that the total ionizing dose tolerance of the Si implanted SOI device is improved significantly. The metastable electron traps introduced by Si implantation is also investigated by electrical stress. The results show that these traps are very instable, and electrons will tunnel into or out of the metastable electron traps quickly after hot-electron-injection or hot-hole-injection.

Keywords: silicon-on-insulator, total ionizing dose, Si ion implantation, metastable electron traps

PACS: 85.30.Tv, 61.80.Ed, 85.40.Ry **DOI:** 10.1088/1674-1056/27/4/048503

1. Introduction

Silicon-on-insulator (SOI) technology was originally developed for space and military applications due to its hardness advantages, such as latch-up effect immunity and less sensitivity to single-event upset from energetic cosmic particles.[1,2] Furthermore, in recent years the SOI technology has evolved into mainstream technology to meet the growing commercial market of communication, fast computers, and consumer electronics for its high performance and low-power consumption. As dimensional scaling of complementary metal–oxide–semiconductor transistors (CMOS) approaches to fundamental limits, with respect to other alternative devices SOI technology is extremely competitive to sustain the historical integrated circuit scaling cadence in the future.[3]

However, the SOI devices face more challenges than conventional bulk-silicon technology in hardened applications due to the total ionizing dose (TID) sensitive buried oxide (BOX). Unless radiation hardened, the radiation-induced positive charges in BOX will reduce the threshold voltage of the back-gate transistor, introducing an additional path for leakage current.[2,4–6] Although the drastically improved SOI quality and thinner BOX layer reduce the number of trapped positive charges, the existence of BOX still threatens the reliability of SOI devices in the radiation environment. It has been confirmed that silicon ion implantation into BOX can effectively improve the TID hardness, which is attributed to the produced deep electron traps with large capture cross section compensating for radiation-induced positive charges.[7–15] Properties of radiation-hardened SOI materials fabricated on separation by implantation of oxygen (SIMOX) wafers with Si implantation have been investigated extensively.[12,15,16] However, less is found in the literature regarding the performances of radiation-hardened SOI using UNIBOND® wafers, which are much more widely used in the present digital SOI device fabrications. Moreover, a number of researches about how to acquire radiation-hardened SOI wafers with good quality have been conducted.[7,11,17,18]

In this work, we use a single-step Si ion implantation to harden the UNIBOND® SOI wafer. Post-implantation annealing is adopted to recover the crystal damage induced by implantation and form the Si nanocrystal at the same time. It is actually equivalent to adding a global implantation step just like well or source/drain implant without photoresist into the normal CMOS process in the beginning, which is simpler and easier to control the SOI wafer quality than other complex hardened methods. Some characterization methods were performed to evaluate the top-silicon quality of the radiation-hardened SOI materials, including transmission electron microscopy (TEM), electrical parameter measurement and gate-oxide-integrity (GOI) test. The anti-radiation capabilities of our hardened SOI devices are confirmed through radiation experiments. According to previous studies, besides the deep

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electron traps introduced by Si ion implantation, a certain number of metastable electron traps are created near the top-Si/BOX interface which can capture or release electrons easily, thus leading to bias instabilities.[12,13,17] The implant-induced metastable electron traps of our hardened SOI devices are also investigated by electrical stress.

2. Experimental details

The initial SOI wafer was standard 200-mm diameter UNIBOND wafer from the SOITEC Corporation. The top Si film was 100-nm thick and the BOX layer was 145-nm thick. A modified 130-nm partially-depleted (PD) SOI technology with hardened shallow trench isolation (STI) was used in this work. Before normal CMOS processing, Si ions were implanted into the initial SOI wafer followed by rapid thermal annealing. The location of an implant peak was targeted at tens of nanometers away from the top-Si/BOX interface in the BOX layer, which was obtained by TRIM calculation. The gate oxide thickness of the input/output (I/O) n-type metal-oxide-semiconductor transistor (NMOSFET) was about 6 nm, and the operating voltage (VDD) was 3.3 V; the gate oxide thickness of CORE NMOSFETs was about 1.8 nm, and the VDD was 1.2 V. The device was 24-pin ceramic packaged. Because I/O devices are more sensitive to the TID effect than the CORE device mainly due to its thicker gate oxide and lower concentration of well implant, this paper focuses on the radiation response of body-tied I/O device.

Radiation experiments were carried out by using a ^{60}Co-γ radiation source at $\sim$ 200 rad(Si)/s dose rate. During radiation exposure, the devices were under Pass-Gate (PG) bias that the drain and source terminals were biased at 1.1 VDD with other terminals (gate, body, and substrate) grounded. The 1.1 VDD is the maximum supply voltage according to the operation voltage with a 10% precision.

3. Results and discussion

In the first section, the results from various characterization methods show the quality of the radiation-hardened SOI materials. Then the TID response of our hardened SOI device is investigated through radiation experiments. In addition, electrical stress is used to investigate the implant-induced metastable electron traps.

3.1. Hardened SOI wafer quality

A TEM image of the hardened SOI wafer after Si implantation and rapid thermal annealing is shown in Fig. 1. The crystalline structure of top-Si is clear and complete, and the top-Si/BOX interface is sharp. It is indicated that the implantation does not cause obvious damage to the lattice of the top-Si layer. To confirm that the extra Si implantation does not affect the top-silicon quality for device manufacturing, the GOI is tested as well. Generally, the intrinsic oxide lifetime is much longer than the required service life, but defects can significantly reduce the oxide lifetime. The GOI test is used to estimate the integrity of a thin oxide and as a tool for driving constant improvement in the thin oxide process. The top-silicon crystal quality affects the gate oxide grown on the Si surface, hence, the GOI result can reflect the top-silicon quality when the device is processed by a qualified technology (that is, the GOI test result is unrelated to the process technology). Moreover, the GOI test is conducted after the processing flow has finished, which can reflect the actual gate oxide quality in devices. It is more meaningful than any other material characterization method to confirm whether the implanted SOI wafer is qualified for device manufacturing.

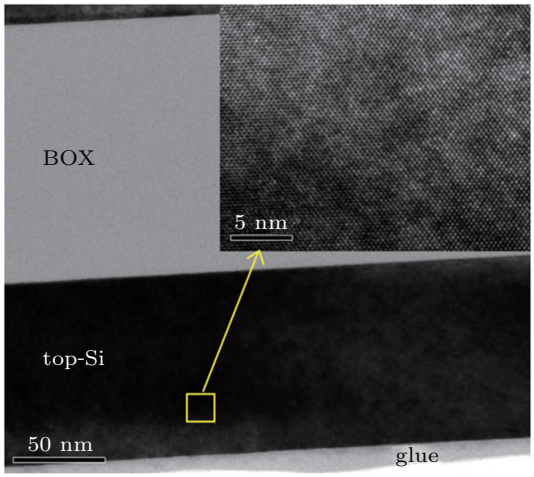


Fig. 1. (color online) TEM images of the hardened SOI wafer.

The tested structure for GOI in this paper is bulk area type, composed of 20×8 MOS capacitor units connected in parallel. The MOS capacitor unit layout is shown in Fig. 2, and the gate oxide area of each MOS capacitor unit is 100 μm×70 μm. The MOS capacitors with thin and thick gate oxide correspond to CORE and I/O device respectively, moreover, both types contain two kinds of capacitors: one is P+ poly/N well (P type) and the other is N+ poly/P well (N type). The procedure of the wafer-level GOI test refers to JEDEC standard JESD35-A.[19] During measurement, the source, drain and body contacts are grounded and the gate terminal is biased with incremental ramp voltage. For the MOS capacitor with thick gate oxide, corresponding to the high-voltage (HV) sample, the breakdown voltage is defined as a critical gate voltage when the gate current exceeds the compliance current ($I_{\rm comp} = 50$ mA) or manifests a large slope change

(more than 2.5 times in I_g–V_g) curve. For the thin one, corresponding to low-voltage (LV) sample, the breakdown voltage is defined as a critical gate voltage when the gate current measured at nominal operation voltage exceeds 1×10^{-4} A after specific voltage stress. Figure 3 shows the gate oxide voltage breakdown voltages of 41 shots in one wafer for each type of capacitor, all the absolute values of breakdown voltages are above 2.3 times the VDD (2.76 V for LV capacitor; 7.6 V for HV capacitor), which meet the use requirements in integrated circuits.[19] Furthermore, except the HVN type MOS capacitor, all the other three types show excellent uniformity within wafers. In order to improve the threshold voltage of parasitic STI-induced transistors, the modified 130-nm PDSOI technology has specific adjustment in body concentration of HV NMOS, leading to worse uniformity in capacitor breakdown voltage than other types. However, it does not affect the device operation.

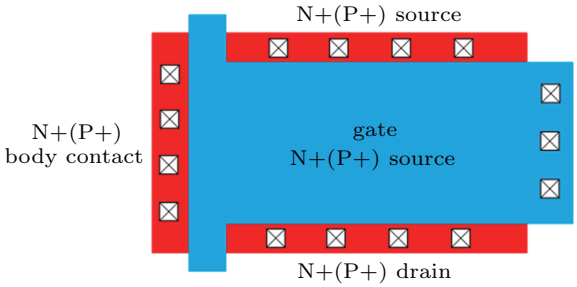


Fig. 2. (color online) Schematic diagram of the MOS capacitor unit used for gate oxide integrity assessment.

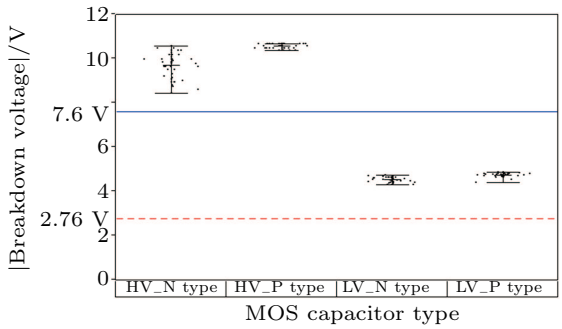


Fig. 3. (color online) Absolute values of gate oxide breakdown voltage for each type of MOS capacitor.

A TEM micrograph of the hardened SOI transistor with $W/L = 10$ μm/0.35 μm is shown in Fig. 4. The transistor structure is clearly visible, and there is nothing abnormal. Figure 5 shows the output curves of the hardened PDSOI NMOS with four typical corner sizes, $W/L = 10/10$, 0.15/10, 10/0.35, and 0.15/0.35. Except that the device with $W/L = 10/0.35$ has a little kink effect at large drain voltage, all of the other devices show perfect typical output characteristic curves. Due to the large $W/L(10/0.35)$ ratio, the body resistance is high so that the accumulated holes in the body area cannot be removed rapidly through body contact. As a result, there is a kink effect in the I_{ds}–V_{ds} curve, which occurs in an unhardened SOI device as well. This phenomenon is process-dependent and unrelated to the unhardened SOI material. The average values and three times standard deviation of threshold voltage (V_{t1}) and saturation current (I_{ds}) of the front transistors of hardened and unhardened SOI devices are summarized in Table 1. A cross pattern of five dies per wafer is used. There is no obvious difference between hardened and unhardened devices, and the uniformity of the hardened device is close to that of the unhardened one. It is indicated that the extra Si implantation with appropriate parameters has not had an influence on the final electrical characteristics of the device. Moreover, the implantation shows a good uniformity on the whole wafer. According to the TEM observation and electrical characterization results, it is indicated that the top-Si crystal quality of the hardened SOI wafer is good enough for device manufacturing.

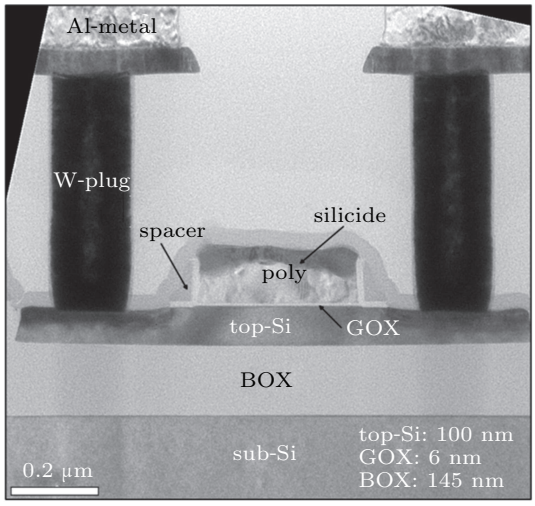


Fig. 4. Cross-section of the hardened SOI I/O NMOS ($W/L =$ 10 μm/0.35 μm) a body tie and shallow trench isolation.

3.2. Radiation-hardened capability

The obvious improvement in radiation hardness of Si implanted SOI device is observed from Fig. 6. In Fig. 6(a), the commercial SOI NMOS has a large leakage current on the order of 100 pA after 500-krad(Si) irradiation, whereas there is no obvious increase in leakage current of the hardened SOI NMOS after 1-Mrad(Si) irradiation as shown in Fig. 6(b). Figure 7 illustrates the corresponding back-gate I–V curves of unhardened and hardened SOI devices after different irradiation doses. Because the back-gate threshold voltage of the hardened device is about 10 V higher than that of the control device before irradiation, the STI-induced parasitic transistor shows up, leading to the hump phenomenon in the transfer I–V curve. According to Fig. 7(a), the subthreshold region of the back-gate transistor of the unhardened SOI device has already crossed zero voltage after 500-krad(Si) irradiation when

the threshold voltage of the hardened device is still larger than 0 V after 1-Mrad(Si) irradiation. The threshold voltage shift of the back-gate main transistor, reflecting the radiation response of BOX essentially, is extracted by the maximum transconductance method and illustrated in Fig. 8. It shows that the hardened device has a smaller negative shift than the unhardened sample, and the threshold voltage shift of the hardened device is saturated with total dose more quickly than that of the unhardened sample. After 300-krad(Si) and 750-krad(Si) irradiation, the back-gate threshold voltage shifts are −15.2 V, −8 V, and −18.4 V, −10.0 V, for unhardened and hardened samples respectively. It is confirmed that implanting Si ions into BOX can effectively reduce the net positive charge quantity built up during irradiation.

Table 1. Pre-radiation threshold voltages and saturation currents of hardened and unhardened SOI devices.

Parameters	CORE NMOS ($W/L = 10$ μm/0.13 μm)		I/O NMOS ($W/L = 10$ μm/0.35 μm)	
	Hardened	Unhardened	Hardened	Unhardened
V_{tl}/V	0.32 ± 0.015	0.3 ± 0.021	0.85 ± 0.018	0.85 ± 0.015
I_{ds}/(μA/μm)	516.92 ± 28.947	557.67 ± 35.16	439.54 ± 10.356	466.31 ± 10.044

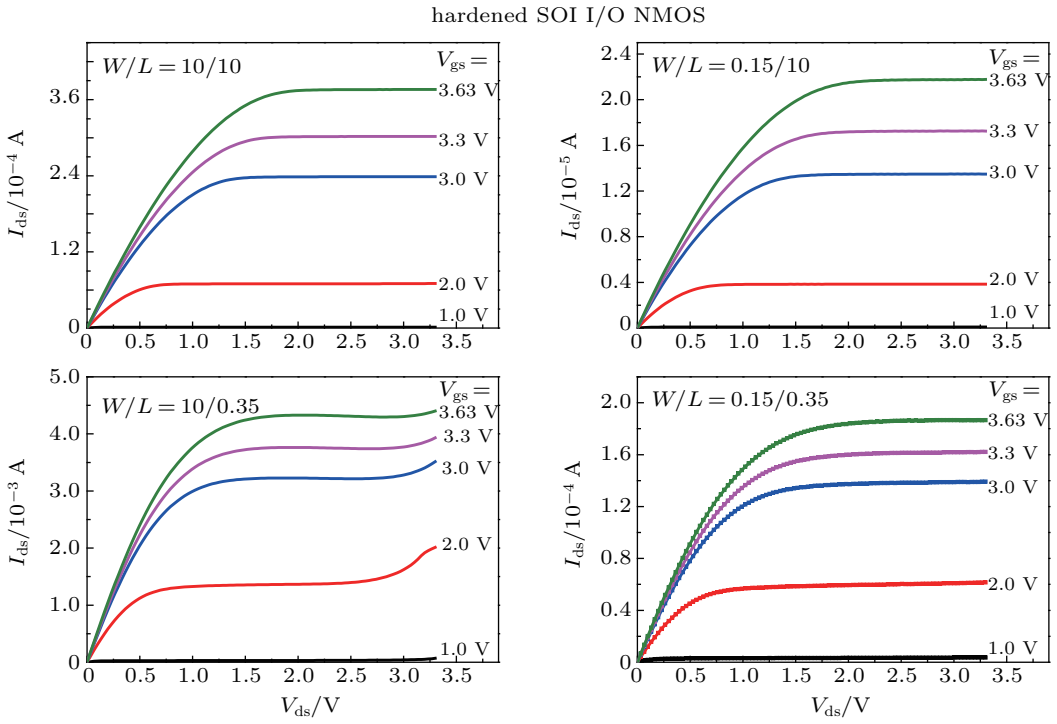


Fig. 5. (color online) Output characteristics of the hardened SOI I/O NMOS ($W/L = 10$ μm/10 μm, 0.15 μm/10 μm, 10 μm/0.35 μm, 0.15 μm/0.35 μm).

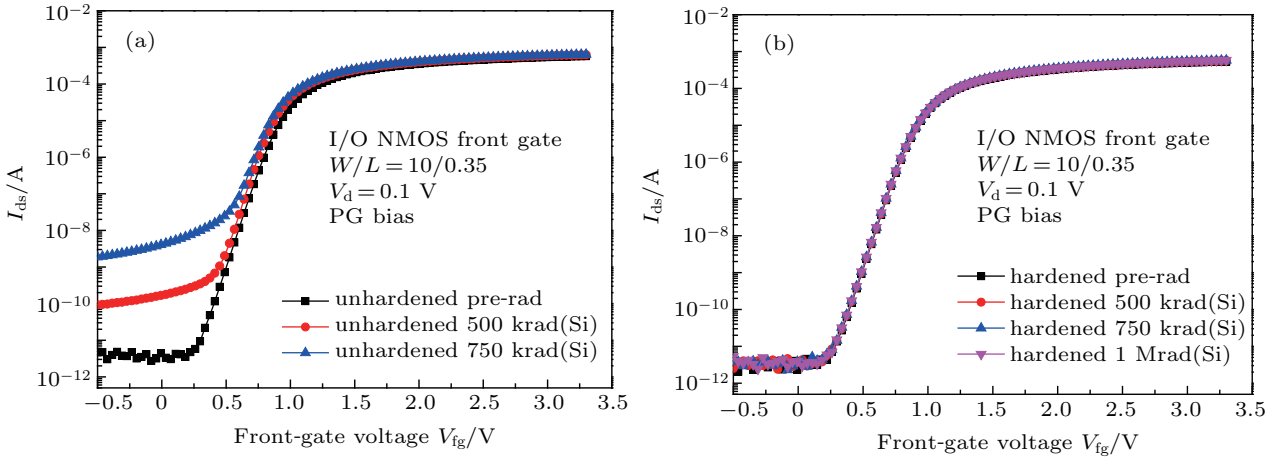


Fig. 6. (color online) Front-gate transfer characteristics of (a) unhardened and (b) hardened SOI I/O NMOS ($W/L = 10$ μm/0.35 μm) after different irradiation doses.

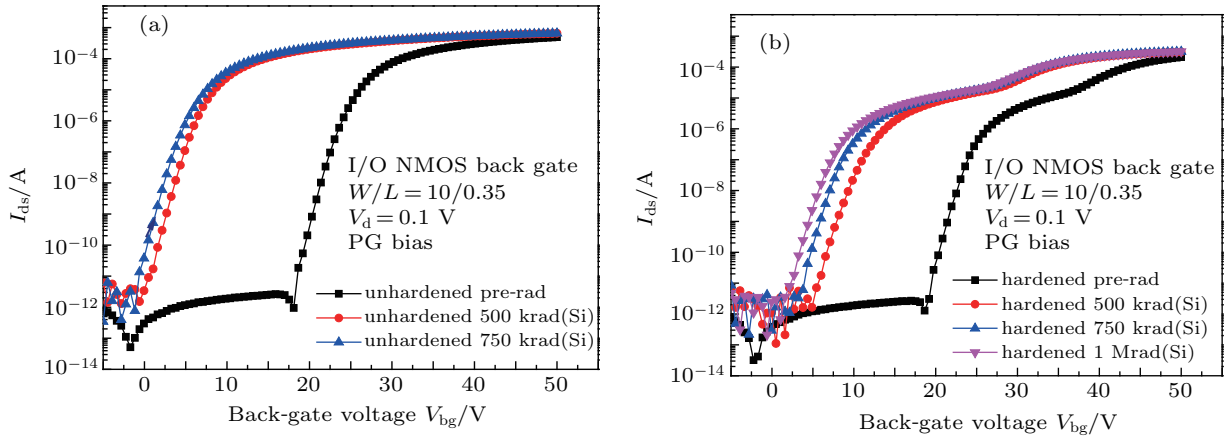


Fig. 7. (color online) Back-gate transfer characteristics of (a) unhardened and (b) hardened SOI I/O NMOS ($W/L = 10$ μm/0.35 μm) after different irradiation doses.

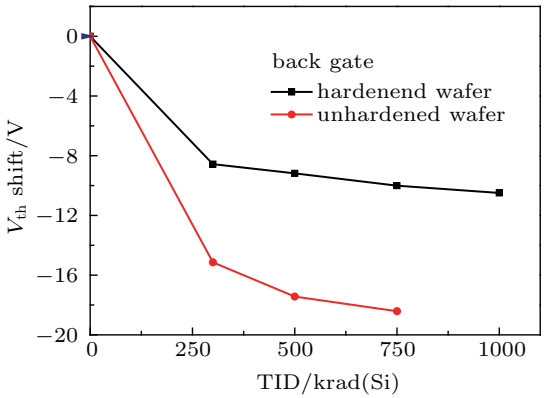


Fig. 8. (color online) Back-gate threshold voltage shifts of unhardened and hardened SOI devices at different irradiation doses.

As reported in previous papers, there is a hysteresis phenomenon in the back-gate *I*–*V* curve for the hardened SOI device due to implantation-induced metastable electron traps.[12,20] By applying different bias voltages to the substrate terminal, the electrons can tunnel into and out of the metastable electron traps, thus changing the back-gate threshold voltage before irradiation. As shown in Fig. 9, the *I*–*V* hysteresis phenomenon also occurs in our Si-implanted SOI device. In order to investigate the electrical characteristics of the metastable electron traps, electrical stress is exerted on the back-gate transistor. The back-gate transistors of unhardened and hardened SOI devices are at 3.63-V drain voltage (V_d) and 30-V back-gate voltage (V_{bg}) for different stress times to generate continuous hot-electron-injection into the BOX. After 20-min long time positive stress 3.63-V drain voltage (V_d) and −30-V back-gate voltage (V_{bg}) are applied to the sample for different stress times to generate continuous hot-hole-injection. According to Fig. 10, for both kinds of SOI devices, the threshold voltage of the back-gate transistor increases with positive stress time increasing due to hot-electron-injection, resulting in STI-induced hump phenomenon of the *I*–*V* curve in the unhardened sample as well, and then the shift approaches to saturation quickly. However, the hardened SOI device shows larger positive shift than the unhardened one after the same stress time. It is interesting to note that, after negative stress, when the unhardened device has a small negative shift of back-gate threshold voltage, the hardened one has a significant negative shift and the threshold voltage turns even much smaller than the initial value after 10-min long time stress.

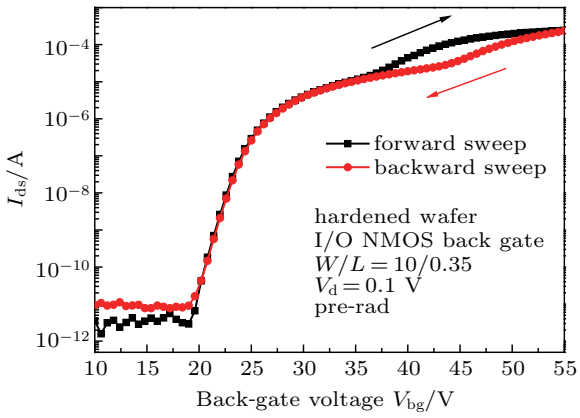


Fig. 9. (color online) Forward and backward sweep transfer *I*–*V* curves of the back-gate transistor of the hardened SOI device.

After implanting Si ions into BOX, deep electron traps with large capture cross section are mostly formed and located at the implantation peak after high temperature annealing. Due to the tail of the implantation profile, there are a small number of Si ions near the top-Si/BOX interface. These near-interfacial implanted Si ions can create electron traps after annealing, which are in the metastable state that can capture or release electrons easily. It is speculated that the metastable electron traps are (or similar to) vacancy related defects and present at elevated densities in the implanted buried oxide.[12] Table 2 shows the threshold voltage value of the back-gate transistor after different positive and negative stress times. Due to the existence of metastable electron traps introduced by Si implantation, the hardened SOI wafer can capture

more electrons than the normal SOI wafer during hot-electron-injection. After 20-min long time positive stress, threshold voltage shifts for unhardened and hardened devices are 6.2 V and 7.8 V respectively. On the other hand, because these traps are in a very instable state, trapped electrons tunnel out of the metastable electron traps quickly after hot-hole-injection, thus making the oxide more positively charged. Moreover, these produced metastable electron traps are located near the top-Si/BOX interface. Hence, once the injection of electrons or holes happens, most of the traps can capture electrons or holes easily, which results in the back-gate threshold voltage shifting to the saturation point quickly. In addition, before irradiation the hardened device has a larger back-gate threshold voltage than the unhardened one when they both use the same technology processing. Furthermore, after 20-min long time negative stress, the back-gate threshold voltage shift of the hardened device is −23.7 V, whose absolute value is larger than the shift value 7.8 V under the same duration of positive stress. Thus, it is certainly believable that part of metastable electron traps have already been occupied by a certain number of electrons generated during processing. After negative stress, these trapped electrons also tunnel out of the implanted BOX, thus leading to large negative shift. According to the final negative shift value (−23.7 V) of the back-gate threshold voltage, from the following Eq. (1), the sheet density of metastable electron trap ($N_{\rm met}$) is estimated at $3.53\times10^{12}/{\rm cm}^2$:

$$\Delta V_{\rm TB} = -q\Delta N_{\rm met}/C_{\rm ox}, \tag{1}$$

where $C_{\rm ox}$ is the buried oxide capacitance per unit area, and $\Delta V_{\rm TB}$ is the threshold voltage shift of the back-gate transistor.

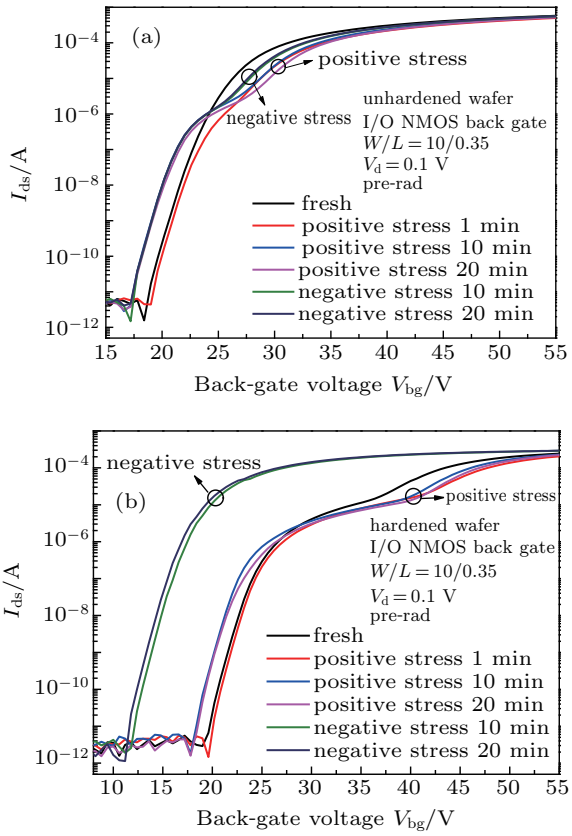


Fig. 10. (color online) Back-gate transfer characteristics after different positive and negative stress times for (a) unhardened and (b) hardened SOI devices.

Table 2. Threshold voltages of the back-gate transistor before and after different positive and negative stress times.

Sample	Fresh	Positive stress			Negative stress	
		1 min	10 min	20 min	10 min	20 min
Unhardened SOI	27.1 V	29.7 V	32.5 V	33.3 V	31.6 V	31.4 V
Hardened SOI	37.8 V	41.9 V	44.7 V	45.6 V	22.4 V	21.9 V

4. Conclusions and perspectives

Before the normal CMOS process, we add an extra single-step Si implantation into BOX layer with post-implantation rapid thermal annealing to harden the SOI wafer. The radiation results show that the hardened SOI device has a good radiation capability and does not have obvious leakage current after 1-Mrad (Si) radiation. It is also proven that this Si implantation technology with appropriate parameters does not affect the quality of the top-Si, and the hardened SOI wafer meets the requirement for device manufacturing. When Si implantation creates deep electron traps in BOX, the metastable electron traps located near the top-Si/BOX interface are also produced. The electrons can tunnel into and out of the metastable electron traps quickly after applying different bias voltages to the substrate terminal, resulting in hysteresis phenomenon in the back-gate I–V curve. Further research needs conducting to avoid generating these metastable traps, especially for fully-depleted SOI wafer.

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