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Influence of fin architectures on linearity characteristics of AlGaN/GaNFinFETs*

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We investigate the influence of fin architecture on linearity characteristics of AlGaN/GaNFinFET. It is found that the FinFET with scaled fin dimensions exhibits much flatter G_m characteristics than the one with long fins as well as planar HEMT. According to the comparative study, we provide direct proof that source resistance rather than tri-gate structure itself dominates the G_m behavior. Furthermore, power measurements show that the optimized FinFET is capable of delivering a much higher output power density along with significant improvement in linearity characteristics than conventional planar HEMT. This study also highlights the importance of fin design in GaN-based FinFET for microwave power application, especially high-linearity applications.

Keywords: AlGaN/GaNFinFETs, output power density, linearity characteristics

PACS: 73.61.Ey, 52.77.Bn, 73.40.Qv **DOI:** 10.1088/1674-1056/27/4/047307

1. Introduction

Recently, GaNFinFETs or tri-gate HEMTs have drawn considerable attention because of their potential advantages over conventional planar HEMTs. Better suppression of short channel effects (SCEs) from enhanced gate control of additional sidewall gates,[1,2] and possible higher electron velocity[3] would enable further scaling of the gate length for high-speed device application. Besides, positive threshold voltage (V_{TH}) shift and better electrostatics also make them a very promising candidate for the power electronics applications.[4,5] To date, there have been multiple demonstrations of GaNFinFETs with varied structures.[1–9] One of the key differences between them lies in the relative position between fins and gate electrode. As suggested by previous work, these fin variants are likely to bring a difference to G_m behavior and thus the linearity characteristics of devices. Azize *et al*. reported a broader G_m curve in a FinFET featuring nanofins along the entire area between source and drain than in planar HEMTs.[7] Similarly, improvement in G_m flatness for Al(In)N/GaN fin-type HEMTs was also observed in Ref. [8] where the formed fins still extended beyond the gate region. On the other hand, extremely high linearity characteristics of G_m and f_T were achieved by forming InAlN/GaN fins only under the gate electrode in a self-aligned way.[9] Recently, our group demonstrated a high-linearity AlGaN/GaNFinFET by developing new fin formation sequences.[10] With regard to microwave applications, a direct comparison between these FinFETs is imperative in order not only to get more insight into various properties of GaNFinFETs but also to determine the optimal fin configuration with the best linearity behavior. However, these efforts are not available at the moment.

In this work, we investigate comparatively two varied AlGaN/GaN fin architectures fabricated in different processes. One FinFET features long fins extending beyond the gate footprint, whereas the other one has fins fully covered by the gate electrode. The latter FinFET is found to exhibit an enhanced direct current (DC), power and linearity performance. The possible origin of G_m nonlinearity behavior is also analyzed.

2. Experimental details

The epitaxial structure consists of an $Al_{0.3}Ga_{0.7}N$ (11 nm)/AlN (1 nm) barrier layer, a 20-nm GaN channel, and a 1.0-μm $Al_{0.4}Ga_{0.96}N$ buffer layer. A sheet carrier density of 1.82×10^{13} cm^{-2} and an electron mobility of 1627 cm^2/V·s were obtained by Hall measurements. After alloyed Ti/Al/Ni/Au ohmic contacts and Ar^+ implantation isolation, the samples were passivated with 60-nm Si_3N_4 deposited by plasma-enhanced chemical vapor deposition. For both kinds of FinFETs, firstly, 600-nm-long nanowire patterns of resist mask were defined in the middle of drain/source electrodes by electron beam lithography (EBL). The SF_6-based plasma etching was then employed to transfer the mask to the Si_3N_4 passivation layer.

For the first structure, denoted as FinFET1, a low-damage BCl_3/Cl_2 plasma dry etching was subsequently performed, resulting in a 600-nm-long Si_3N_4/AlGaN/GaN fin. The Al-

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GaN/GaN heterostructure was etched to a targeted 30-nm depth. Then, a T-type gate was determined by EBL using a bilayer resist. Finally, after removing Si_3N_4 dielectric under the gate footprint by SF6-based plasma etching, an Ni/Au gate metal was evaporated and lifted off.

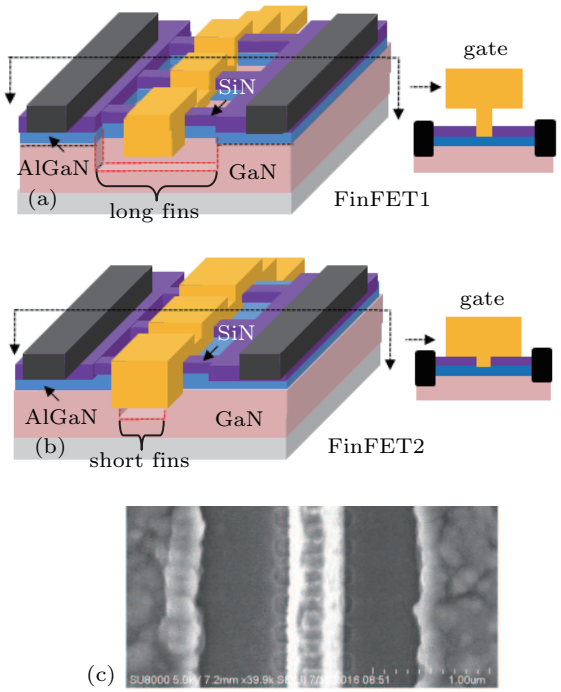


Fig. 1. (color online) Schematics of (a) FinFET1 and (b) FinFET2, (c) SEM image of FinFET2 after gate formation. The difference in gate geometry is also indicated.

On the other hand, for FinFET2, after the above-mentioned Si_3N_4 mask transfer, the gate footprint was first determined by a second EBL. Then, the etching of AlGaN/GaN was carried out with the same depth as that for the FinFET1. Finally, following SiN mask removal from the top of the fin by SF_6-based plasma, a 450-nm-long gate electrode fully covering the fin region was determined by a third EBL. It is noteworthy that this implementation of gate footprint definition prior to AlGaN/GaN etching allows FinFET2 to have scaled nano-fins as long as the gate length. In contrast, the fabricated fins in FinFET1 extended to the source/drain access region for a total of $\sim$ 500 nm, which leads to a relatively large parasitic source resistance.

The structures are schematically shown in Fig. 1. The fin-width ($W_{\rm Fin}$) and pitches ($W_{\rm pitch}$) were measured to be $\sim$ 80 nm and 250 nm by SEM, respectively. All investigated devices each had a gate length ($L_{\rm G}$) of 100 nm, a source–drain distance of 2 μm, and a gate electrode width ($W_{\rm g}$) of 2×50 μm. For the FinFET sample, the effective gate width ($W_{\rm eff}$) was commonly calculated to be $W_{\rm eff} = n \times W_{\rm Fin} = 400 \times 80$ nm $= 32$ μm,[10] where n is the number of fins. In general, for dc and RF power performance, FinFETs were normalized to $W_{\rm eff}$, whereas planar HEMTs were normalized to $W_{\rm g}$.[7–10] Note that a compact device layout with a scaled gate pitch of 8 μm was designed here for power evaluation. Conventional planar HEMTs with field-plate T-gate having identical device dimensions to FinFET2 were also fabricated for comparison.

3. Results and discussion

The direct current (DC) output characteristics of planar HEMT and FinFETs are plotted in Fig. 2. When output current is normalized with respect to $W_{\rm eff}$, FinFET1 delivers a maximum drain current density ($I_{\rm D,max}$) of 870 mA/mm at $V_{\rm G} = 1$ V and $V_{\rm D} = 10$ V along with a maximum transconductance ($G_{\rm m,max}$) of 504 mS/mm, which is closely comparable to 950 mA/mm and 485 mS/mm of planar HEMT. The results indicate that the produced Si_3N_4/AlGaN/GaN fins in the source/drain access regions in FinFET1 maintain the two-dimensional electron gas (2DEG) sheet resistance of the planar structure, most likely caused by the inclusion of the SiN cap, thereby preventing the AlGaN/GaNhetero structure from releasing strain. Besides, planar HEMT suffers pronounced SCEs at low gate voltage as well as self-heating effect when subjected to high drain current. However, both effects become unobvious in the case of FinFETs. Moreover, the much smaller knee voltage indicates FinFETs may be applicable for low voltage applications.

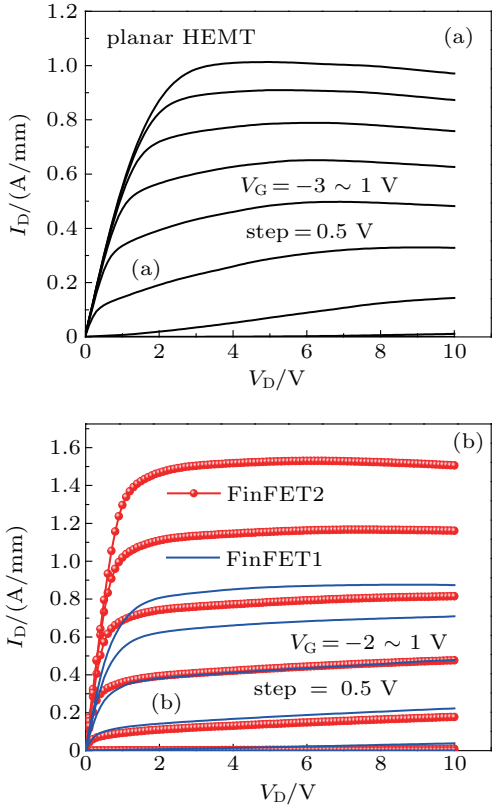


Fig. 2. (color online) Typical normalized $I_{\rm D}$–$V_{\rm D}$ curves of (a) planar HEMT and (b) FinFETs each with a gate length of 100 nm.

Figure 3 displays typical transfer characteristics of these devices. Both FinFETs show a positive $V_{\rm TH}$ shift of $\sim$ 0.9 V

compared with planar HEMT due to the sidewall-gate depletion effect. The slightly larger V_{TH} of FinFET1 than that of FinFET2 possibly results from the partial strain release due to much longer AlGaN/GaN fins in FinFET1. Furthermore, FinFET2 reveals not only a dramatically increased $I_{D,max}$ to 1530 mA/mm and $G_{m,max}$ to 740 mS/mm, but also a broader extrinsic G_m response than planar HEMT and FinFET1.

The values of differential source resistance (R_S) of these devices as a function of drain current are measured to investigate the possible origin of this difference. The gate contact is forward biased with respect to the channel by introducing a 5-mA/mm current through the gate of the transistor into the channel as shown in the inset of Fig. 4. In this experiment, it is assumed that the voltage drop across the gate Schottky barrier is constant. Therefore, the derivative of the gate voltage with respect to the source current gives the differential source access resistance R_S. An obvious nonlinear R_S is observed in both planar devices and FinFET1 as indicated in Fig. 4, whereas this unwanted behavior is dramatically suppressed in FinFET2. As Trew *et al.* previously suggested, the nonlinear R_S behavior is probably induced by space-charge limited current.[11] Under high current condition, the electric field in the gate-source access region is reduced in magnitude as a function of increasing charge injection, leading to an increase in source access resistance with drain current increasing. As is well known, the extrinsic G_m linearity of GaN HEMT is determined by intrinsic transport behavior and parasitic source resistance. Ture *et al.* have claimed that high linearity is inherent to FinFET with tri-gate topology.[12] By excluding the intrinsic behavior of tri-gate topology in this study, comparison of two FinFET variants further demonstrates that the reduced source access resistance is a main contributor to the high extrinsic linearity. Due to the large source access width relative to nano-channels under the gate in FinFET2, enough electrons can be supplied by the source, thus G_m roll-off or drain current drop under the high current condition is mitigated. The result also provides a direct proof of a previous proposal by Lee *et al.*[9] and our group[10] where planar HEMT and FinFET were compared with each other.

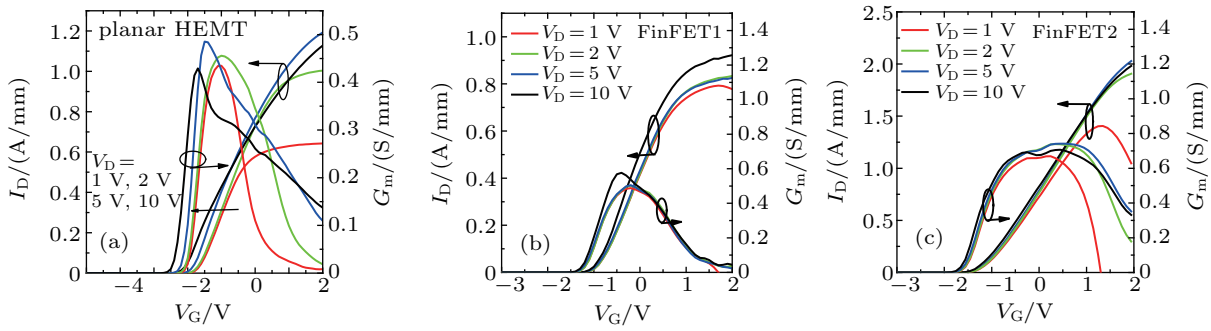


Fig. 3. (color online) Transfer characteristics of (a) planar HEMT, (b) FinFET1, and (c) FinFET2 as a function of drain voltage at V_D = 1 V, 2 V, 5 V, 10 V.

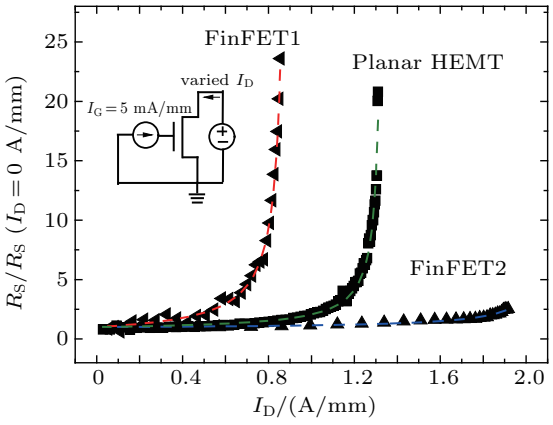


Fig. 4. (color online) Comparison among normalized source resistances as a function of drain current density for all investigated devices.

Sub-threshold characteristics as a function of drain voltage are displayed in Fig. 5. FinFETs are seen to exhibit an almost unchanged sub-threshold slope of around 90 mV/Dec and significant enhancement in DIBL from 137 mV/V to 44 mV/V, indicating SCEs are effectively suppressed by nano-fin configurations stemming from the enhanced gate controllability of the sidewall gate. The difference in off-state current can be explained by the different gate leakage behaviors as shown in the inset of Fig. 5. As expected, planar HEMT shows a sizable increase in reverse leakage because of the electric field concentrating on the gate edge. On the contrary, even with an initial higher value at low V_G for FinFETs, the leakage is rapidly saturated with increasing applied gate bias, which is very desirable for high power applications. Besides, due to larger access resistance, at low V_G FinFET1 has a smaller gate reverse current, but the leakage currents in both FinFETs tend to be comparable to each other because the inherent FinFET configuration begins to dominate the leakage behavior at higher V_G. Nevertheless, the off-state leakage might be further improved by optimizing the etching process such as TMAH treatment.[14,14]

The S parameters are measured on-wafer from 10 MHz to 40 GHz, and the resulting f_T values are shown in Fig. 6. The pronounced drain bias-dependent f_T behaviors in planar

HEMT are greatly improved for both FinFET structures due to remarkably suppressed SCEs as discussed above. However, an extremely flatter curve of extrinsic f_T versus gate bias only occurs in FinFET2, which shows that it is in good agreement with the G_m characteristic. This means that FinFET2 is capable of maintaining a highly linear frequency response throughout a large range of gate and drain biases due to the combination of the intrinsic linearity of tri-gate structure and reduced source resistance in the fin configuration. The relatively low f_T values are attributed to increased parasitic capacitance associated with field-plate T-gate structure and sidewall contact. This adverse effect will degrade the maximum operating frequency and reduce power gain as will be shown below.

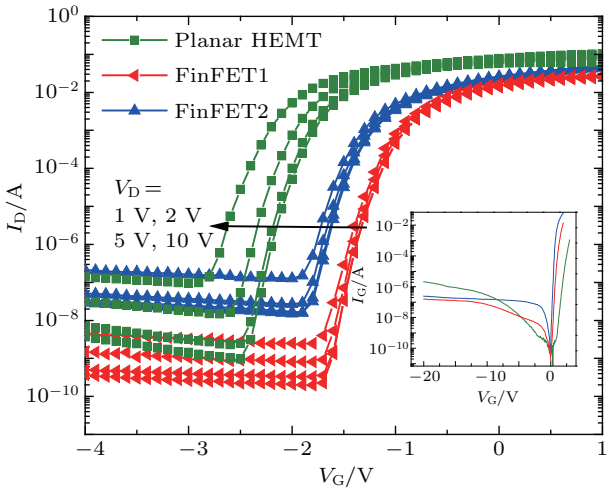


Fig. 5. (color online) Sub-threshold characteristics of three types of devices investigated. Raw current values are given for clear comparison. Inset: gate diode leakage characteristics.

Since FinFET1 exhibits a similar G_m behavior but inferior DC performance in comparison with planar HEMTs, we conduct a comparison of the power performance between planar and FinFET2. Both single and two-tone RF power measurements are performed by a Maury Load–Pull system at 4 GHz. Both devices are biased at a drain voltage of 15 V in class AB using a quiescent drain current of 10% $I_{D,max}$. When matched for maximum output power condition, the FinFET exhibits a 2.1× higher maximum output power density (P_{out}) of 3.3 W/mm from 1.55 W/mm of planar HEMTs (see Figs. 7(a) and 7(b)). This significant improvement probably results from a larger output current and better thermal management capacity in a tri-gate configuration.[10,13] Linearity is characterized through third-order distortion measurements (IM3) with 10-MHz spacing. Devices are tuned for maximum PAE. As presented in Fig. 7(c), FinFET2 shows a slightly higher PAE, while IM3 characteristics are seen to be greatly improved. Specifically, for the same PAE of 55%, an IM3 suppressed by about 6 dBc is obtained for FinFET2.

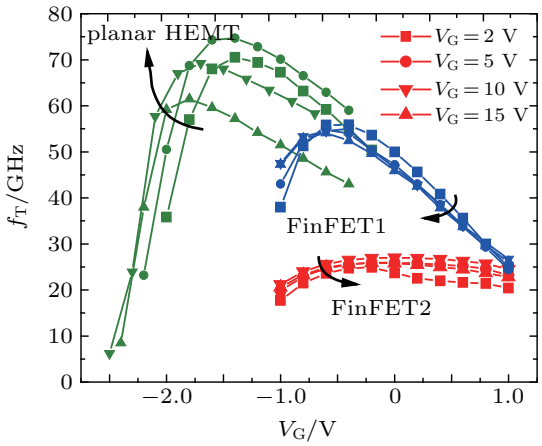


Fig. 6. (color online) Changes of f_T with gate and drain voltage.

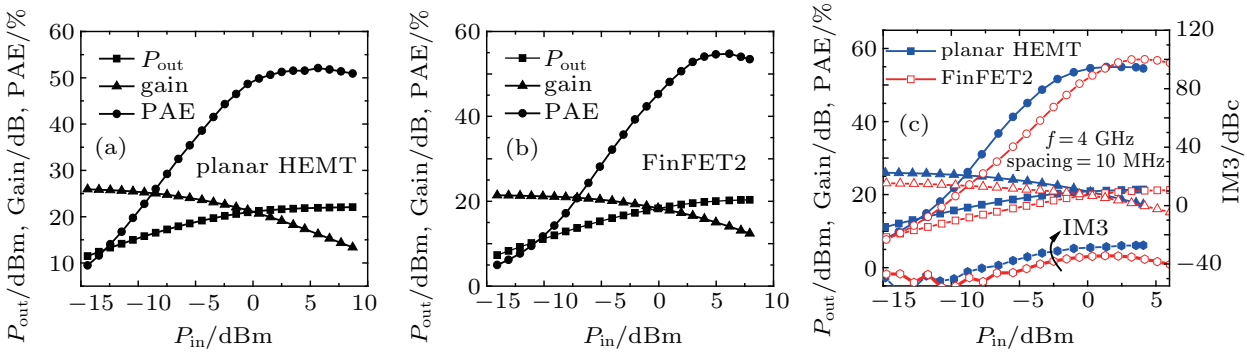


Fig. 7. (color online) (a) Large-signal output power characteristics of (a) planar HEMT, (b) FinFET2, and (c) two-tone linearity measurements conducted at 4 GHz with 10-MHz tone spacing.

4. Conclusions and perspectives

A comparison of two types of fin architectures has been performed in this work. The SCEs and gate leakage properties are improved for both FinFETs in comparison with planar HEMT. However, the FinFET featuring nano-fins fully covered by a T-gate electrode allows higher values of G_m and $I_{D,max}$, and especially, extremely linear G_m behavior. The delivered 2.1× improvement in output power density along with the advantage of noticeably enhanced linearity characteristics indicates that the optimized FinFET is highly promising for high-power applications where both linearity and efficiency are critical. For higher frequency application, nevertheless,

further reduction in parasitics by updating the device design is required.

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