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Analysis of multiple cell upset sensitivity in bulk CMOS SRAM after neutron irradiation

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In our previous studies, we have proved that neutron irradiation can decrease the single event latch-up (SEL) sensitivity of CMOS SRAM. And one of the key contributions to the multiple cell upset (MCU) is the parasitic bipolar amplification, it bring us to study the impact of neutron irradiation on the SRAM's MCU sensitivity. After the neutron experiment, we test the devices' function and electrical parameters. Then, we use the heavy ion fluence to examine the changes on the devices' MCU sensitivity pre- and post-neutron-irradiation. Unfortunately, neutron irradiation makes the MCU phenomenon worse. Finally, we use the electric static discharge (ESD) testing technology to deduce the experimental results and find that the changes on the WPM region take the lead rather than the changes on the parasitic bipolar amplification for the 90 nm process.

Keywords: displacement damage, neutron irradiation, multiple cell upset (MCU), parasitic bipolar amplification

PACS: 85.30.De, 61.80.–x, 73.40.Qv **DOI:** 10.1088/1674-1056/27/3/038501

1. Introduction

With the downscaling of semiconductor feature size, the critical charge is getting smaller. Single event upset (SEU) is one of the predominant soft errors to memory devices all the time. A decrease in the critical charge can lead to an increase in SEU rate.[1] What is worse, an increase of packing densities results in the multiple node charge collection becoming more obvious.[2] This means that one incidence particle can impact more adjacent nodes which pose a significant problem for traditional SEU mitigation techniques like error correction coding (ECC).[3] As we can see, multiple cell upset (MCU) can be expected to dominate the error cross section in the future.

There are three important semiconductor parameters of bulk Si which are known as carrier lifetime, carrier concentration, and carrier mobility.[4] Neutron irradiation can change these three parameters at the same time, but the relative sensitivity is not the same as shown in Fig. 1.[4] The most sensitive parameter is the carrier lifetime which could impact the current gains of parasitic bipolar transistors in the CMOS inverter. The previous work has shown that using neutron irradiation can decrease the single event latch-up (SEL) sensitivity of CMOS static random access memory (SRAM).[5]

It is common knowledge that one of the key contributions to MCU is the parasitic bipolar amplification.[6] Therefore, we expected that using neutron irradiation could improve the MCU sensitivity of CMOS SRAM devices. Focusing on this goal, we conducted heavy ion experiments to test how the MCU sensitivity changes after neutron irradiation. Finally, we analyzed the experimental results and obtained the conclusions.

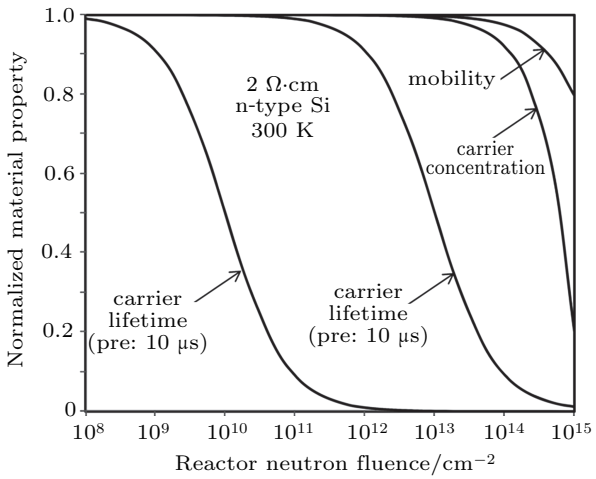


Fig. 1. Changes on three semiconductor parameters induced by neutron irradiation.[4]

2. Neutron irradiation

The CY62126EV30LL is a 1-Mbit (64K×16) static RAM which is fabricated on a 90 nm bulk CMOS process and is claimed to be immune to SEL. This brought us to test its MCU characteristics after neutron irradiation. There is no well contact in each bit cell, the N-well and P-well contacts are placed at intervals of 32 rows. The practical size of each bit cell is 0.84 μm×1.2 μm.

Neutron irradiation experiments were conducted at the Xi'an Pulsed Reactor (XAPR), which is located at the Northwest Institute of Nuclear Technology (NINT) in China. XAPR provides both thermal and fast neutron beams over a range of

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energies. We used the 1# shielding equipment which held a high n/γ value around 6.1×10^{9} cm^{-2}·rad(Si)$^{-1}$as the experimental environment.[7] The cumulative neutron fluence was 2×10^{14} 1-MeV(Si)-n/cm^2.

Before further testing, the chips were stored until the radioactivity was reduced to the safe range.[5] To verify the functions of the post-neutron-irradiation chips after neutron irradiation, we used the VLSI test system J750E$_X$ to test the primary electrical parameters of the chips from the datasheet in two months. The test results are shown in Table 1. No parameter's variation between the pre- and post-neutron-irradiation chips exceeds 10%.

Table 1. Electrical parameters of CY62126EV30 taken on the pre-neutron-irradiation chips (1# and 2#) and the post-neutron-irradiation chips (3#, 4#, and 5#).

Chip	Read-write test	I_{CC}/mA	I_{SB}/μA	T_{AA}/ns	T_{ACE}/ns	T_{AW}/ns	T_{PWE}/ns
1#	pass	1.2329	0.6882	78.0000	88.0000	72.0000	109.0000
2#	pass	1.3416	0.9722	74.0000	84.0000	70.0000	105.0000
3#	pass	1.2528	1.0266	73.0000	84.0000	69.0000	105.0000
4#	pass	1.3345	1.0637	74.0000	84.0000	70.0000	105.0000
5#	pass	1.2865	1.0522	73.0000	83.0000	69.0000	105.0000

3. Heavy ion experiment

3.1. Experimental test setup

The heavy ion experiments were carried out at the heavy-ion SEE irradiation facility located at China's Institute of Atomic Energy (CIAE). The ^{48}Ti and ^{79}Br ions were chosen to expose our SRAM chips. Table 2 shows the heavy ion species including their associated energies, linear energy transfer (LET), and ranges in Si.

Table 2. Heavy ions used for characterization of 90 nm SRAM.

Ion	Energy/MeV	LET/MeV·cm^2·mg^{-1}	Range in Si/μm
^{48}Ti	169	21.8	34.7
^{79}Br	218	42.0	30.2

3.2. Experimental results

Before the heavy-ion experiment, the DUTs already decapsulated were previously written with the initial data pattern "0x5555". Next, the SRAMs were tested statically by reading back memory cells' data and monitoring the current for latchups.

After the heavy-ion experiment, the test results were recorded and saved. Table 3 lists an example of MCU at one moment under ^{48}Ti ion irradiation. The total upset number was 18 including 7 bits' flip from 0 to 1 and the other 11 bits' flip from 1 to 0.

What is more, to obtain the corresponding relationship between the CY62126EV30's logical address and physical address, chip's reverse analysis was performed. Based on the above work, we developed the mapping application shown in Fig. 2.[8]

When the test results in Table 3 were imported to the mapping application, we could obtain every bit flip's address and physical location like Fig. 2. As we can see, the flips during this read cycle included 3 to 5 bits' upset. According to all the heavy-ion experimental results at CIAE, we charted the histograms of pre- and post-neutron-irradiation chips' percentages of different flips' event shown in Figs. 3 and 4.

Figure 3 shows the histograms of the MCUs obtained with ^{48}Ti exposure. The black bars show the distribution of different flips' event for the devices without neutron irradiation and the red bars for the 2×10^{14} 1-MeV(Si)-n/cm^2 neutron irradiated devices. Firstly, the upset number of the pre-neutron-irradiation chips focused on 2 to 4 bits (accounted for more than 70%) and there were little upsets above 8 bits. Secondly, for the post-neutron-irradiation chips, the upset number focused on 4 to 6 bits (accounted for more than 50%) and the possibility of upsets above 8 bits became bigger.

As is shown in Fig. 4, the upset number of chips without neutron irradiation focused on 4 to 6 bits (accounted for more than 50%) under ^{79}Br ion environment. After 2×10^{14} 1-MeV(Si)-n/cm^2 neutron irradiation, the upset number above 8 bits accounted for more than 70%.

Table 3. An example of MCU at one moment under ^{48}Ti ion irradiation.

Address (in Hex)	Read data	Expected data	Address (in Hex)	Read data	Expected data	Address (in Hex)	Read data	Expected data
0802	55D5	5555	0810	55D5	5555	7AE1	5554	5555
7AE9	5554	5555	7AF9	5554	5555	82E0	5155	5555
82E8	5155	5555	9AAD	1555	5555	9AAF	1555	5555
9AB9	4555	5555	9ABD	1555	5555	9ABF	1555	5555
A2E0	5155	5555	A619	55D5	5555	BCA1	555D	5555
BCA3	555D	5555	BCB1	555D	5555	EBF7	55D5	5555

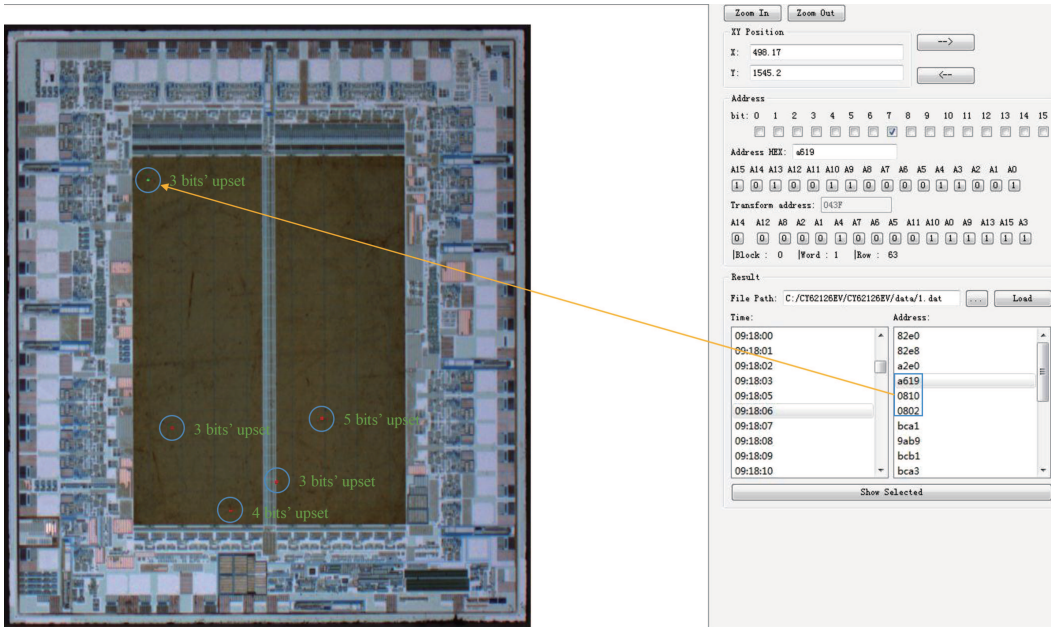


Fig. 2. (color online) Map of bit flips under ^{48}Ti irradiation. Only those bits flipped during one read cycle are plotted.

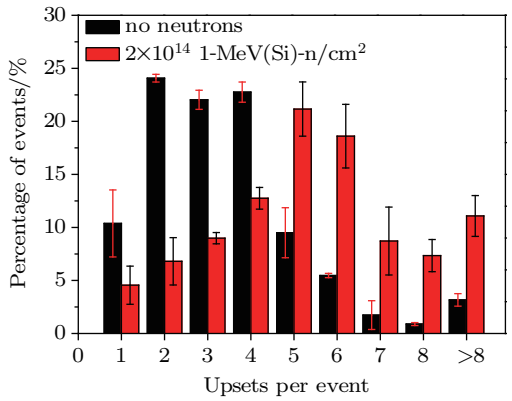


Fig. 3. (color online) Histograms of the MCUs obtained with ^{48}Ti exposure (LET : 21.8 MeV·cm^2·mg^{-1}).

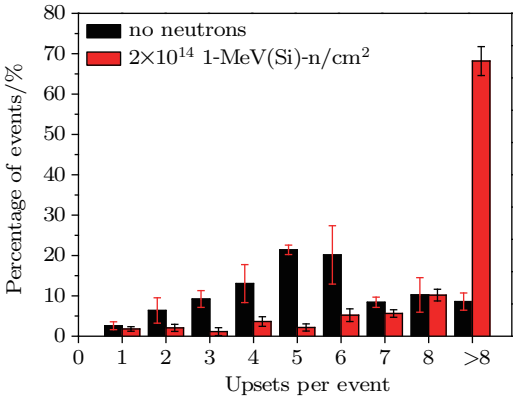


Fig. 4. (color online) Histograms of the MCUs obtained with ^{79}Br exposure (LET : 42.0 MeV·cm^2·mg^{-1}).

3.3. Results analysis

Beyond our expectation, the heavy-ion experimental results show that the upset number of CY62126EV30 get increased in one MCU event after neutron irradiation. So, we conclude that the SRAM's MCU phenomenon becomes worse after neutron irradiation which is not the same as the SEL sensitivity experimental results.[5] As we all know, the parasitic bipolar amplification and the well potential modulation (WPM, shown in Fig. 5) mechanism are two mutually limiting factors to the MCU phenomenon. The heavy-ion experimental results illustrate that the impact of the neutron induced displacement damage on the WPM mechanism is the predominant impact factor.

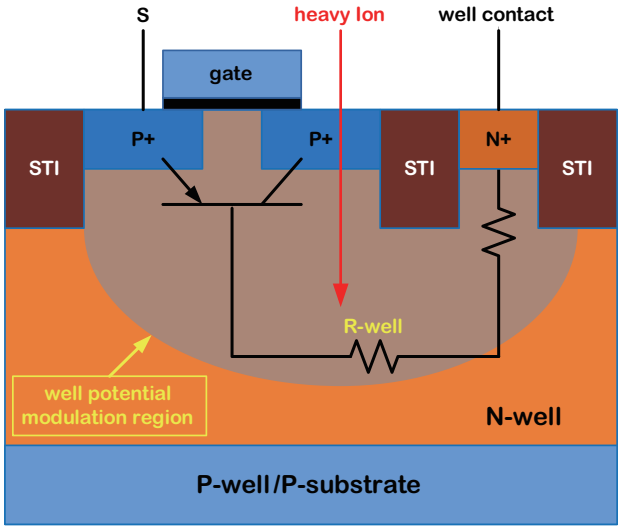


Fig. 5. (color online) Schematic diagram of WPM region in MOSFET induced by heavy ion strike.

From Fig. 1, it is found that neutron induced displacement damage can reduce the carrier concentration, which could lead to an increase of the well region's resistivity and further result in an expanded WPM region. Gaspard *et al.*[9] have studied the relationship between the n-well doping concentration and the WPM under a heavy ion strike as shown in Fig. 6. When the peak doping decreased from 10^{18} cm^{-3} to 10^{17} cm^{-3}, the

WPM extended 4 times on the spatial scale and 6 times on the temporal scale. This means that the WPM region will expand after neutron irradiation. When a heavy ion strikes the well region, it will impact more adjacent nodes, leading to an increase of MCU sensitivity.

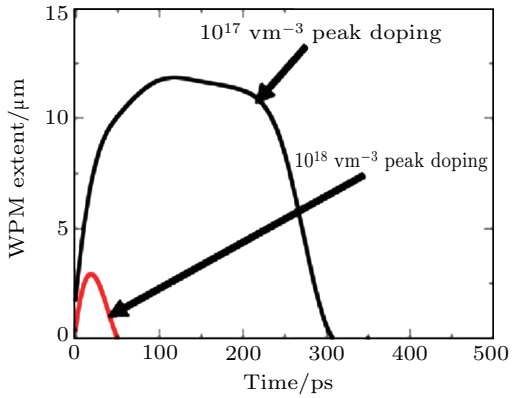


Fig. 6. (color online) Simulation results from Gaspard *et al.*,[9] which show the WPM extent versus time in an N-well with 10 μm-spaced well contacts for two peak well doping concentrations.[9]

To verify our analysis, we utilized the electric static discharge (ESD) diode technique.[10] As we all know, SRAM's modern technique always uses the ESD diodes on the chip's I/O pins to protect it from electrostatic discharge. Generally, one ESD diode is made up of one N-well diode and one P-well diode and its breakdown voltage is proportional to the doping concentration of the well region ($V_{BD} \sim N^{-2/3}$). Therefore, we could measure these ESD diodes' breakdown voltage to estimate the changes on the well regions' carrier concentration.

For the N-well ESD diode, we applied a bias voltage (from 0 to 2.5 V) to VDD and one I/O pin; the other chip's pins kept floating as shown in Fig. 7(a). The current was constantly monitored as the voltage increased, and then we obtained the *I*–*V* sweep in Fig. 7(b). As shown in the test results, the breakdown voltage of the N-well ESD diode has obviously increased after neutron irradiation. Therefore, we concluded that the N-well doping concentration decreased after neutron irradiation.

For the P-well ESD diode, the bias voltage was applied to one I/O pin and GND; the other chip's pins kept floating as shown in Fig. 8(a). Analogously, the *I*–*V* sweep for the P-well ESD diode was obtained in Fig. 8(b). We found that the P-well doping concentration showed no change after 2×10^{14} 1-MeV(Si)-n/cm^2 neutron irradiation.

Above all, we found that the major factor which leads to the increase of CY62126EV30's MCU sensitivity is the expanded WPM region. Neutron exposure will decrease the SRAM chip's N-well doping concentration and the resistivity decreases at the same time. Therefore, the WPM extends on both temporal and spatial scales.

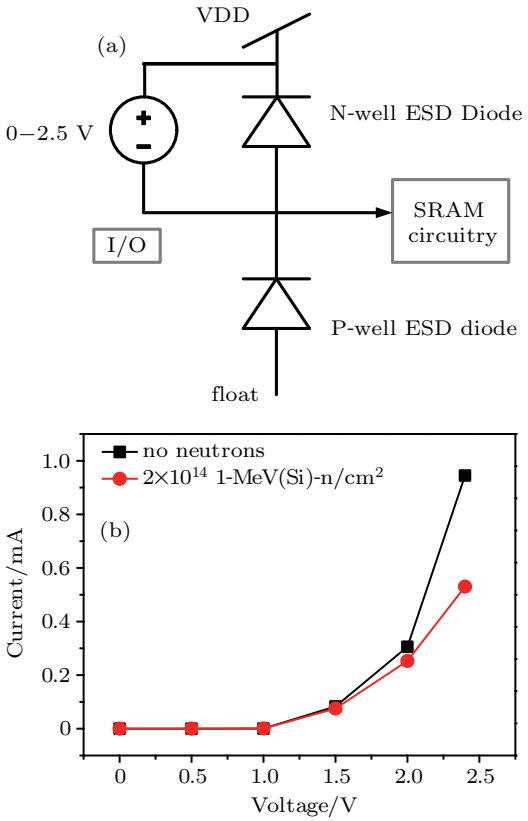


Fig. 7. (color online) (a) Schematic diagram for testing N-well ESD diode's breakdown voltage and (b) the experimental results.

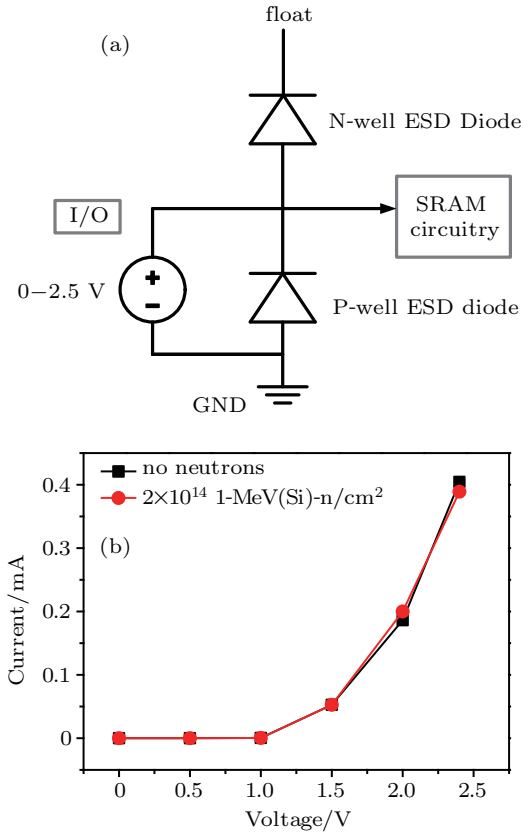


Fig. 8. (color online) (a) Schematic diagram for testing P-well ESD diode's breakdown voltage and (b) the experimental results.

4. Conclusion

In this paper, we study the changes of CMOS SRAM's MCU sensitivity after neutron irradiation. Firstly, the test results of J750E$_X$ show that neutron irradiation has negligible impact on the performance of CY62126EV30. After 2×10^{14} 1-MeV(Si)-n/cm^2 neutron irradiation, the heavy ion experiment is conducted, and the upset number in one MCU event increases. This phenomenon illustrates that the dominant impact of neutron exposure on MCU sensitivity is the expanded WPM's range induced by carrier removal, which is not the same as the experimental result of SEL sensitivity. Then, we use the ESD circuitry in the SRAM chip to verify our deduction. The test results show that the chip's N-well doping concentration decreases after neutron irradiation and the neutron fluence has no obvious impact on the P-well doping regions' concentration. What is more, the WPM mechanism is not obvious for the large feature size SRAM devices. It is very necessary to do more experiments with different layout design SRAM devices on different feature sizes and different neutron fluences.

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