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Citation: Chin. Phys. B . 2018, 27(2): 027201. **doi:** 10.1088/1674-1056/27/2/027201

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Observation of nonconservation characteristics of radio frequency noise mechanism of 40-nm n-MOSFET*

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(Received 9 November 2017; revised manuscript received 12 November 2017; published online 5 January 2018)

Bias non-conservation characteristics of radio-frequency noise mechanism of 40-nm n-MOSFET are observed by modeling and measuring its drain current noise. A compact model for the drain current noise of 40-nm MOSFET is proposed through the noise analysis. This model fully describes three kinds of main physical sources that determine the noise mechanism of 40-nm MOSFET, i.e., intrinsic drain current noise, thermal noise induced by the gate parasitic resistance, and coupling thermal noise induced by substrate parasitic effect. The accuracy of the proposed model is verified by noise measurements, and the intrinsic drain current noise is proved to be the suppressed shot noise, and with the decrease of the gate voltage, the suppressed degree gradually decreases until it vanishes. The most important findings of the bias non-conservative nature of noise mechanism of 40-nm n-MOSFET are as follows. (i) In the strong inversion region, the suppressed shot noise is weakly affected by the thermal noise of gate parasitic resistance. Therefore, one can empirically model the channel excess noise as being like the suppressed shot noise. (ii) In the middle inversion region, it is almost full of shot noise. (iii) In the weak inversion region, the thermal noise is strongly frequency-dependent, which is almost controlled by the capacitive coupling of substrate parasitic resistance. Measurement results over a wide temperature range demonstrate that the thermal noise of 40-nm n-MOSFET exists in a region from the weak to strong inversion, contrary to the predictions of suppressed shot noise model only suitable for the strong inversion and middle inversion region. These new findings of the noise mechanism of 40-nm n-MOSFET are very beneficial for its applications in ultra low-voltage and low-power RF, such as novel device electronic structure optimization, integrated circuit design and process technology evaluation.

Keywords: nanoscale MOSFET, non-conservation characteristics, noise mechanism, radio frequency

PACS: 72.70.+m, 72.30.+q, 73.43.Fj **DOI:** 10.1088/1674-1056/27/2/027201

1. Introduction

With the advent and application of metal–oxide–semiconductor field-effect transistor (MOSFET), the research and characterization of its noise mechanism has become the focus of research.Its low frequency noise is used to identify the deep level defects of the device, in order to ascertain the reliability of the device. With the development of down-scaling of technology, it is very important to understand the high frequency noise characteristics of nanoscale MOSFET. Its radio frequency (RF) noise is modeled to meet the needs of the optimal designs of various information transmission and processing systems.[1–5]

The needs of low-voltage and low-power design of modern and future wireless communication/network systems have greatly stimulated the applications of digital complementary metal–oxide–semiconductor (CMOS) technology in RF analog integrated circuits. One of the most important problems is how to establish a precise RF equivalent noise circuit model of MOFET. In the two-port equivalent noise model of the common source configuration of MOSFET shown in Fig. 1, the drain current noise (S_{id}) has always been a concern because it characterizes the noise mechanism of MOSFET.[1,3,6–11] The power spectral density (PSD) of induced-gate current noise (S_{ig}), which is correlated with $S_{id}(S_{igid*})$, is 2–3 orders of magnitude lower in dimension than S_{id}.[1–7,12,13] Therefore, S_{id} is the dominant noise source of MOSFET, but the most important problem is that the noise mechanism for different channel lengths may be channel thermal noise or shot noise.



Fig. 1. Equivalent noise current source representation of MOSFET.

The long channel thermal noise model has been extensively studied for submicron channel MOSFET, and many different models have been proposed. A physical model based on the electronic structure of devices for a long channel MOSFET is[12]

$$S_{id} = \delta 4kT \left(\frac{W}{L_{eff}} \mu_{eff} C'_{ox} \right) V_{GT}, \tag{1}$$

*Project supported by the National Natural Science Foundation of China (Grant No. 69901003) and the Scientific Research Fund of Sichuan Provincial Education Department.

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where δ is the noise parameter, k is the Boltzmann's constant, T is the absolute temperature parameter and characterizes its thermal noise mechanism, $V_{GT} = V_{GS} - V_T$ is the gate overdrive voltage, $V_T = V_{T0} - V_{DS}$ is the threshold voltage taking into account the drain-induced barrier lowering effect. The parameters in the bracket are the microelectronic process structure parameters of the device.

The most famous compact model for submicron and deep-submicron channel MOSFET is[1,13]

$$S_{id} = 4kT\gamma g_{ds0}, \tag{2}$$

where γ is the bias-dependent noise parameter and g_{ds0} is the output conductance at zero drain voltage (V_{DS}). The accuracy of the model from the strong inversion (SI) region to the weak inversion (WI) region has been confirmed.

Recently, no thermal noise has been observed for an ultrashort (ballistic) channel MOSFET because the scattering centers inside the channel are scarce.[1] Therefore, the shot noise characteristics of around-10-nm MOSFET are observed in the SI and middle inversion (MI) region.[6] The shot noise in ballistic MOSFET has been modeled by modifying the full shot noise model[1,7]

$$S_{id} = 2qI_{DS}F, \tag{3}$$

where the drain current I_{DS} characterizes its shot noise mechanism, the Fano factor F is used to characterize the suppressed shot noise in the SI region. The reason for this suppression has been explained by the Fermi exclusion principle at the barrier and the Coulomb interactions between the carriers already in the channel.[1] Also, F will tend to 1 at a given small drain current.[1,6–8] Recently, a theoretical model of the Fano factor in the strong inversion region has been given.[9]

A more complicated physical model of shot noise based on the device electronic structure for short channel MOSFET is[10]

$$S_{id} = 2q\frac{W}{L_{eff}}\mu_{eff}C'_{ox}(n-1)v_{th}^2 \exp\left(\frac{V_{GT}-V_{off}}{nv_{th}}\right) \times \left(1+e^{-V_{DS}}/v_{th}\right), \tag{4}$$

where $v_{th} = kT/q$ is the thermal voltage, n is the sub-threshold slope factor, and $V_{off} = V_{T,sub} - V_T$ is the offset voltage, which can be extracted from the current–voltage characterization in the sub-threshold region.

At present, the noise investigations of short channel MOSFET focus on the SI and MI region, and the noise mechanism is verified to be the suppressed shot noise for channel length 40 nm or less,[7,9,13] but the thermal noise for channel length longer than 40 nm.[2,7] The WI region is becoming more important for low-voltage and low-power RF applications,[4,5,11,14,15] but recent studies for the devices of 40 nm,[5] 65 nm,[14] and 80 nm[15] have focused on the characterizations of the macroscopic four noise parameters independent of the noise mechanism. In addition, since the millimeter wave effects of S_{ig} and S_{igid*} in sub-threshold region are very obvious; recent studies[4,5,11] have focused on their accurate and continuous modeling from SI to WI region. Unfortunately, S_{ig} and S_{igid*} cannot be used to characterize the device noise mechanism. The following noise observations of 40 nm n-MOSFET are carried out for S_{id} because the noise mechanism of MOSFET is characterized by S_{id}.[1,3,6–11]

In this paper, a physic-based compact model for S_{id} is proposed and validated. New observations of 40-nm n-MOSFET noise controlled by gate voltage (V_{GS}) and drain voltage (V_{DS}) simultaneously from SI to WI region are presented. The special bias non-conservation phenomenon is also characterized by noise analysis and measurement.

2. Device and experiments

In this paper, two n-MOS transistors respectively with channel lengths of 40 nm and 120 nm, fabricated by a 40-nm COMS process, are used for the unified comparison and identification of noise mechanism. The 120-nm device is used to calibrate the noise measurement and analysis method used here because its thermal noise mechanism is well known and can accurately be predicted by the well-proved long channel thermal noise model.[1,3,4,13] Two n-MOS transistors both have $M = 6$ (the number of devices in parallel), $N_f = 10$ (the number of fingers per device) and $W = 2$ μm (width). The measurement frequency ranges from 1 GHz to 60 GHz where the low-frequency noise is negligible.

The RF equivalent circuit model shown in Fig. 2[2,11,16] is used to characterize the device noise behaviors. Figure 3 shows the scattering (S) parameters of 40-nm n-MOSFET in a frequency range of 1 GHz–60 GHz measured by a commercial Agilent 8510C network analyzer. Thus, the parameters of small-signal equivalent circuit of 40-nm n-MOSFET shown in Table 1 can be carefully extracted by using the dummy open and short de-embedding technique.[4,5,17,18]

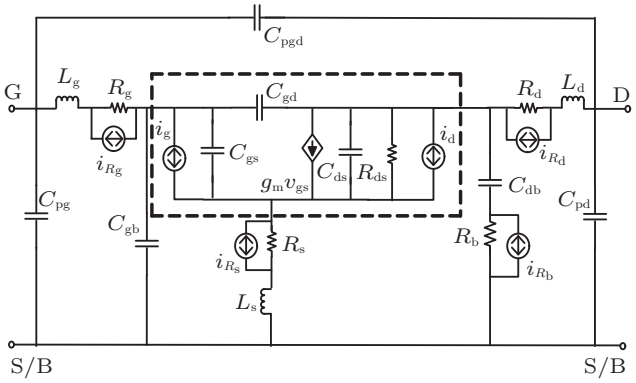


Fig. 2. RF noise equivalent circuit model for tested n-MOSFET.

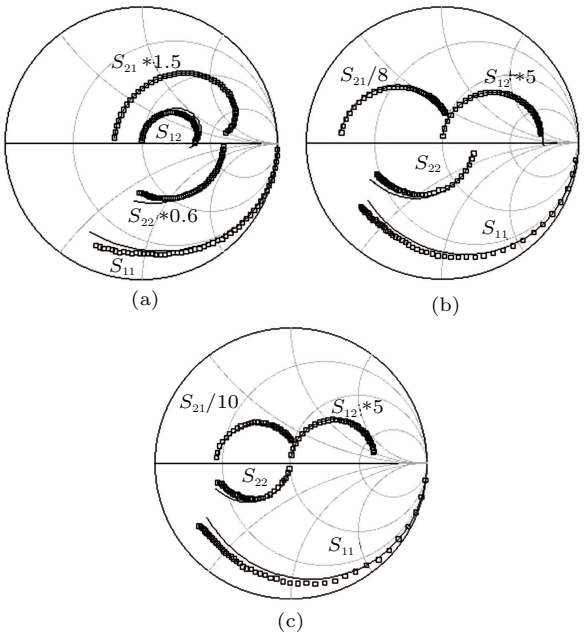


Fig. 3. Measured S parameters of 40-nm n-MOSFET in a frequency range of 1 GHz–60 GHz and with $V_{DS} = 1.1$ V and $V_{GS} =$ (a) 0.18 V, (b) 0.35 V, and (c) 0.7V.

The four noise parameters for 40-nm n-MOSFET, shown in Fig. 4, can also be measured by using a commercial spread-spectrum Agilent N8976B noise figure analyzer.[17–20] After de-embedding the parasitic and noise, the measured S_{id} characterizing the devices noise mechanism can be obtained from[3–5,13]

$$S_{id} = 4kTR_n |Y_{21}|^2, \tag{5}$$

where

$$Y_{21} = \frac{g_m - \omega^2 C_{gd}\left(C_{gd}+C_{gs}\right)R_g - j\omega\left[\left(C_{gd}+C_{gs}\right)R_g g_m + C_{gs}\right]}{1+\omega^2\left(C_{gd}+C_{gs}\right)^2 R_g^2}.$$

Figure 5 shows the observation of noise mechanism for 120-nm n-MOSFET from SI to WI region. The good agreement between the extracted channel thermal noise and its theoretical value based on model (2) validates the reliabilities of noise measurement and analysis method used here.

Table 1. Extracted small-signal parameters of 40-nm n-MOSFET in Fig. 2 which can benefit the noise analysis at $V_{DS} = 1.1$ V.

	V_{GS}/V	0.18	0.35	0.7
	C_{pg}/fF	8	8	8
	C_{pd}/fF	20	20	20
	C_{pgd}/fF	2.1	2.1	2.1
PAD	L_g/pH	52.5	52.5	52.5
parasitic	L_d/ pH	20	20	20
parameters	L_s/ pH	12	12	12
	R_g/Ω	3.98	3.98	3.98
	R_s/Ω	0.378	0.378	0.378
	R_d/Ω	0.306	0.306	0.306
Substrate	R_b/Ω	40.56	17.6	2.00
parasitic	C_{db}/fF	18.10	19.61	20.83
parameters	C_{gb}/fF	0.51	2.39	3.19
	C_{gs}/fF	36.12	47.18	59.78
	C_{gd}/fF	29.76	29.81	30.13
Intrinsic	C_{ds}/fF	4.62	4.96	5.09
parameters	g_m/ms	0.57	5.65	112.82
	τ/ps	0.02	0.08	0.21
	g_{ds}/ms	1.23	7.28	17.68

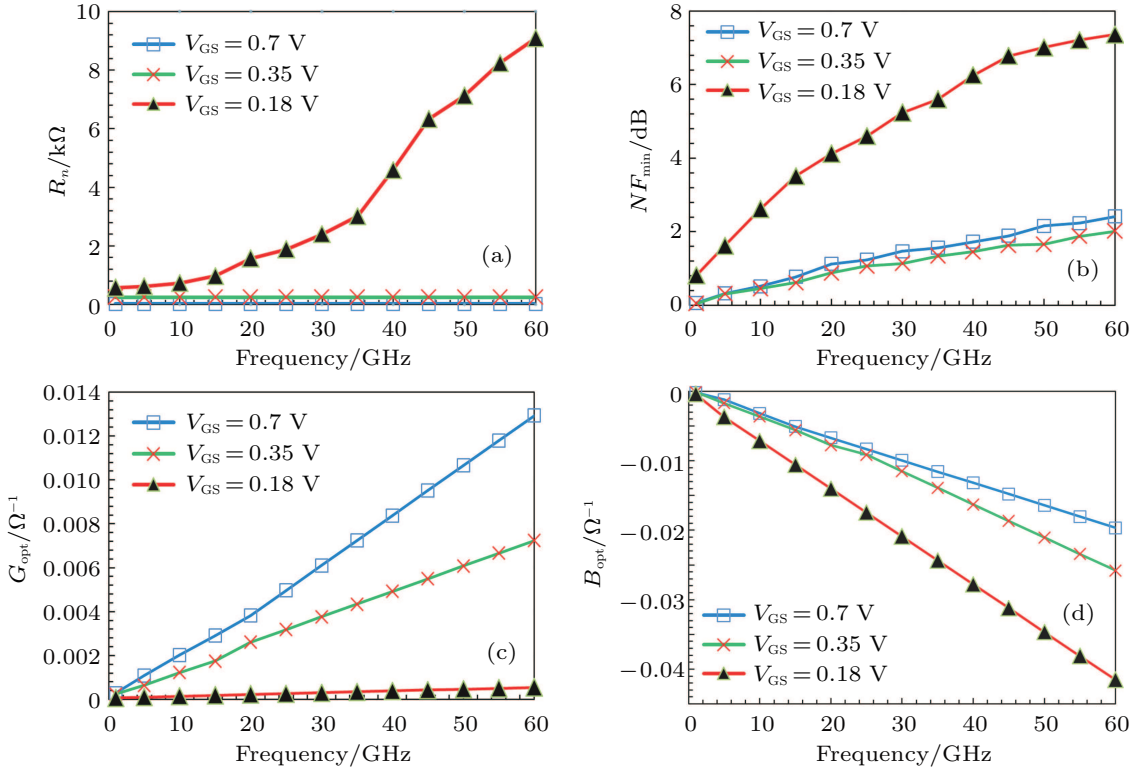


Fig. 4. (color online) Measured four noise parameters of 40-nm n-MOSFET in a frequency range of 1 GHz–60 GHz, showing plots of (a) equivalent noise resistance R_n against frequency, (b) minimum noise figure NF_{min} against frequency, (c) real part of optimum source admittance G_{opt} against frequency, (d) imaginary part of optimum source admittance B_{opt} against frequency.

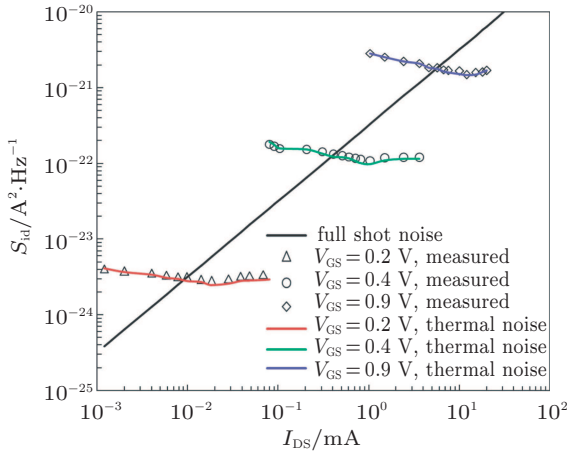


Fig. 5. (color online) Plots of measured S_{id} against I_{DS} for 120-nm n-MOSFET at 10 GHz and $V_{DS} = 1.1$ V.

3. Experimental results and discussion

3.1. Noise source characterization and modeling of 40-nm n-MOSFET

Figure 6 shows that the noise predicted by full shot noise model increases monotonically with V_{GS}.[6,13] The measurement results indicate that in the SI region, the noise mechanism of 40-nm n-MOSFET acts as the suppressed shot noise similar to the recent theoretical prediction,[7,9,13] but a weak temperature dependence is observed. In the MI region, the noise mechanism is near to full shot noise in which the measurement results are all the same as the expectations from model (3). Some own features of 40-nm n-MOSFET are observed that the drain current noise separates itself gradually from full shot noise in the WI region, and ultimately turns into the thermal noise with obvious temperature dependence. Figure 6 also shows that in the WI region, a severe underestimation of noise intensity is obtained if only the shot noise model is used consistently.

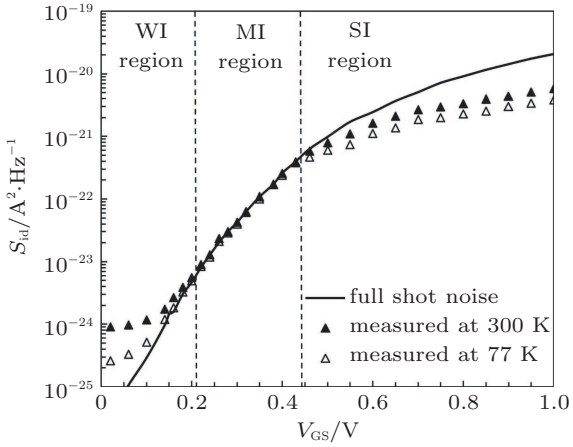


Fig. 6. Plots of measured S_{id} against V_{GS} for 40-nm n-MOSFET at 10 GHz, $V_{DS} = 1.1$ V, and two different temperatures.

For explaining the bias non-conservation characteristics of noise mechanism of 40-nm n-MOSFET shown in Fig. 6, some equivalent circuit parameters of device shown in Table 1 are analyzed.

Firstly, with the improvements of process technology on gate materials, the number of gate fingers and gate layout, the gate parasitic resistance R_g has been greatly reduced. However, the value of R_g in Table 1 is still much larger than those of R_d and R_s. As a common source configuration, device itself provides the transconductance gain g_m from the source to the drain. Therefore, the noise contribution of R_g to S_{id} has always been considered seriously; its strong influence on the long channel[3,4] and 65-nm[2] n-MOSFET in SI region has been confirmed. The thermal noise contribution of R_g to S_{id} can be modeled by[2–4,8]

$$\overline{i^2_{nR_g=}} = 4kTg_m^2R_g. \tag{6}$$

Secondly, Table 1 also shows that drain to substrate parasitic capacitor C_{db} and substrate parasitic resistance R_b may have a greater influence on intrinsic noise current. This is because at low frequencies, idealized substrates do not have coupling effects. However, as the operating frequency rises up to GHz, the reduction of junction capacitance leads to severe coupling between drain and substrate.[21] Such a nonideal coupling effect will obviously affect the characteristic of the output admittance by $Y_{sub} = \omega^2C_{db}^2R_b + j\omega C_{db}$. Therefore, the noise contribution of substrate parasitic to S_{id} can be modeled by

$$\overline{i^2_{nb}} = 4kT\mathrm{Re}(Y_{sub}) = 4kT(\omega C_{db})^2R_b. \tag{7}$$

If the intrinsic drain current noise is assumed to be the suppressed shot noise, its PSD $\overline{i^2_d}$ can be modeled by Eq. (3). Thus, a compact RF noise model for drain current noise of 40-nm n-MOSFET can be described as

$$\begin{aligned} S_{id} &= \overline{i^2_{nd}} + \overline{i^2_{nR_g}} + \overline{i^2_{nb}} \\ &= 2qI_{DS}F + 4kTg_m^2R_g + 4kT(\omega C_{db})^2R_b. \end{aligned} \tag{8}$$

In order to evaluate the noise contributions of R_g and R_b in different operating regions and to verify model (8), the typical PSD values listed in Table 2 are calculated by using the extracted parameters shown in Table 1. Further observations for device noise mechanism are discussed as follows.

Table 2. Typical noise contributions of R_g and R_b for S_{id} at room temperature (300 K) and 10 GHz. The $\overline{i^2_{nd_{max}}}$ and $\overline{i^2_{nd_{min}}}$ represent the shot noise PSDs for intrinsic drain current noise at different V_{DS}.

V_{GS}/V	0.18	0.35	0.7
$\overline{i^2_{nR_g}}/A^2\cdot Hz^{-1}$	2.14×10^{-26}	2.10×10^{-24}	839×10^{-22} (max)
			1.82×10^{-22} (min)
$\overline{i^2_{nb}}/A^2\cdot Hz^{-1}$	8.68×10^{-25}	4.42×10^{-25}	5.63×10^{-26}
$\overline{i^2_{nd_{max}}}/A^2\cdot Hz^{-1}$	3.02×10^{-24}	1.08×10^{-22}	1.55×10^{-21}
$\overline{i^2_{nd_{min}}}/A^2\cdot Hz^{-1}$	4.80×10^{-25}	3.33×10^{-24}	1.44×10^{-23}

3.2. Further observation of noise mechanism change and model verification

As shown in Fig. 7, the characteristics of suppressed ($F \approx 0.301$) shot noise of 40-nm n-MOSFET in saturation region (big I_{DS}) is confirmed by noise measurements at $V_{GS} = 0.7$ V. The $F \approx 0.301$ is consistent with the theoretically predicted value of 0.3 in Ref. [9], which can verify the validity of model (8) about the hypothesis of the intrinsic drain current noise mechanism. Figure 7 also shows that the noise mechanism in the saturation region looks like suppressed shot noise, but it is weakly affected by the thermal noise of R_g. In the linear region, as the V_{DS} decreases, the suppression of the shot noise is reduced (i.e., $F \to 1$), but when I_{DS} is extremely small, the whole noise is almost controlled by R_g. These particular bias non-conservation properties of 40-nm n-MOSFET are also verified by comparing the noise data between 300 K and cryogenic temperature (77 K). Note that as the predictions in the column of $V_{GS} = 0.7$ V in Table 2, the thermal noise in the SI region has a slight influence on the intrinsic shot noise property of the device even though the short channel process has significantly reduced R_g. This is because the transconductance amplification of common source configuration is very strong under the condition of high V_{DS} in the SI region, i.e., very high g_m, which leads to the strong thermal noise contribution of R_g modeled by Eq. (6). But R_b is very small in SI region because the conduction characteristic of channel is very good. Therefore, the model (7) shows that R_b contributes little to the substrate coupling thermal noise as predicted in the column of $V_{GS} = 0.7$ V in Table 2.

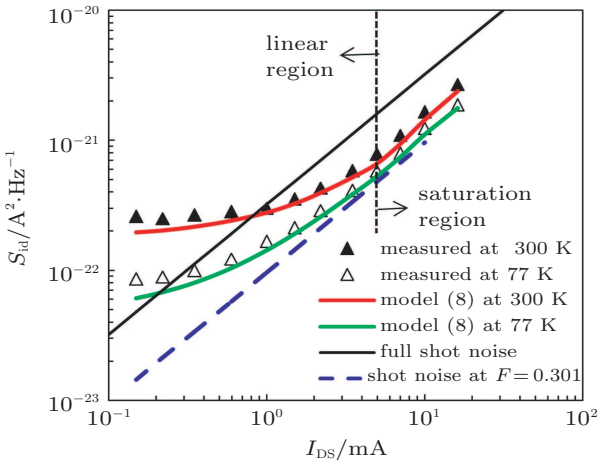


Fig. 7. (color online) Plots of measured and calculated S_{id} against I_{DS} for 40-nm n-MOSFET at $V_{GS} = 0.7$ V (SI) and different temperatures.

As shown in Fig. 8, the measured data at $V_{GS} = 0.35$ V are further analyzed to explain the noise mechanism of 40-nm n-MOSFFET in MI region. Obviously, the device noise mechanism in the saturation region is almost entirely determined by intrinsic drain current noise and is near to the full shot noise as expected in Refs. [9] and [13]. As the predictions in the column of $V_{GS} = 0.35$ V in Table 2, the thermal noise contribution of R_g is greatly reduced in the MI region due to the reduction of g_m, and plays a weak role only in the deep triode region. Moreover, because the conduction characteristic of channel is still good, the thermal noise contribution of R_b is very small.

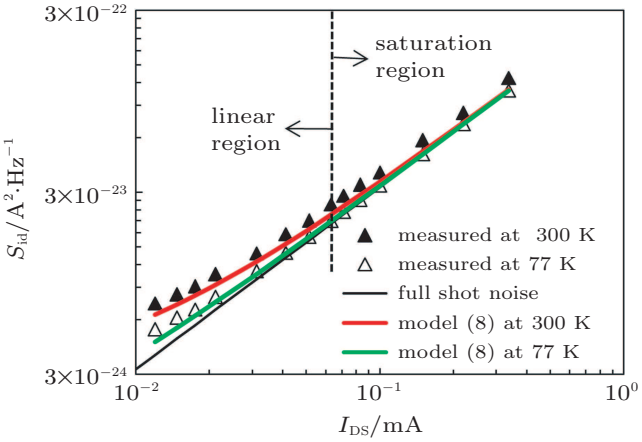


Fig. 8. (color online) Plots of measured and calculated S_{id} against I_{DS} for 40-nm n-MOSFET at $V_{GS} = 0.35$ V (MI) and different temperatures.

Also as shown in Fig. 9, the thermal noise characteristics in the WI region are verified by noise measurements at $V_{GS} = 0.18$ V. The noise behaviors can be determined by further comparing the noise data between 300 K and 77 K at 10 GHz. It is worth emphasizing that the thermal noise behavior of 40-nm n-MOSFET under low voltage weak interaction is very obvious. As the predictions in the column of $V_{GS} = 0.18$ V in Table 2, the thermal noise caused by the substrate coupling (C_{db}, R_b) is higher than intrinsic shot noise and thermal noise of R_g, and becomes the main RF noise source in the WI region. The reason is that g_m is very small under the condition of low bias voltage in WI region, but R_b is relatively high. In addition, the experimental results in Fig. 9 at 30 GHz and 60 GHz show that the substrate coupling noise is strongly frequency-dependent in the WI region, which makes substrate coupling noise become the focus of low-voltage applications in CMOS technology, especially in millimeter wave band.

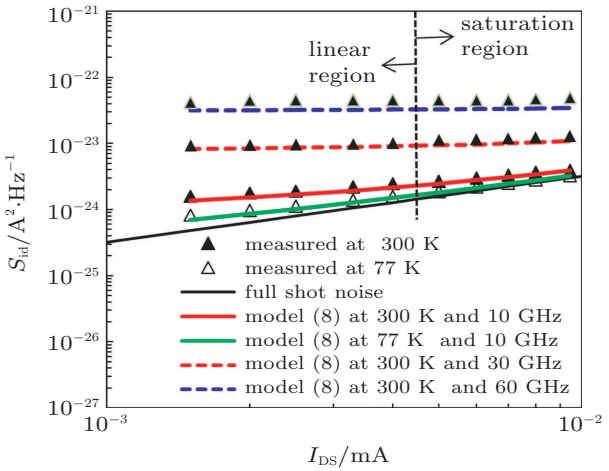


Fig. 9. (color online) Plots of measured and calculated S_{id} against I_{DS} for 40-nm n-MOSFET at $V_{GS} = 0.18$ V (WI) and different temperatures.

4. Conclusions

The RF physical behaviors of drain current noise of 40-nm n-MOSFET are distinguished by noise measurement and analysis over the extended ranges of bias voltage and temperature. The proposed model here is very attractive and promising for the simulation design of novel RF integrated circuit due to its model accuracy especially in the WI region. The noise modeling and measurement results strongly indicate that the RF noise mechanism of 40-nm n-MOSFET changes from intrinsic suppressed shot noise to thermal noise under the condition of low-voltage weak interaction.

Acknowledgment

The authors are grateful to Dr. Cheng Y and his team of Massachusetts Institute of Technology for their helpful discussion on the difficult measurement at low level of inversion.

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