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A simulation study of field plate termination in Ga_2O_3 Schottky barrier diodes*

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In this work, the field plate termination is studied for Ga_2O_3 Schottky barrier diodes (SBDs) by simulation. The influence of field plate overlap, dielectric material and thickness on the termination electric field distribution are demonstrated. It is found that the optimal thickness increases with reverse bias increasing for all the three dielectrics of SiO_2, Al_2O_3, and HfO_2. As the thickness increases, the maximum electric field intensity decreases in SiO_2 and Al_2O_3, but increases in HfO_2. Furthermore, it is found that SiO_2 and HfO_2 are suitable for the 600 V rate Ga_2O_3 SBD, and Al_2O_3 is suitable for both 600 V and 1200 V rate Ga_2O_3 SBD. In addition, the comparison of Ga_2O_3 SBDs between the SiC and GaN counterpart reveals that for Ga_2O_3, the breakdown voltage bottleneck is the dielectric. While, for SiC and GaN, the bottleneck is mainly the semiconductor itself.

Keywords: Ga_2O_3, Schottky barrier diode, field plate, termination technique

PACS: 73.40.Mr, 84.30.Jc, 85.30.De, 85.30.Kk **DOI:** 10.1088/1674-1056/27/12/127302

1. Introduction

In the past decades, wide band gap semiconductor devices, such as SiC and GaN, have been studied extensively for their superior properties. Nowadays, Ga_2O_3, with a wider band gap (4.8 eV), receives more and more attention.[1,2] The Baliga merit of Ga_2O_3 is about 10 times that of 4H–SiC and four times that of GaN,[3] suggesting that it is more suitable for high-power and high-voltage applications.

As a new semiconductor device, the Ga_2O_3 device is just beginning to be studied, and mainly in the Schottky barrier diodes (SBDs)[4,5] and MOSFETs.[6–8] For Ga_2O_3 SBD, edge termination is necessary because the electric field will concentrate on the edge of Schottky junction. In past studies, several ways of terminating edge have been applied to SiC SBDs, including field plates, guarding rings, mesa structures, high-resistivity layers or the combination of such techniques.[9–11] Among these methods, the field plate is very simple and widely adopted when the voltage requirement is not that high, such as the case of 1 kV.[12] For Si or SiC, SiO_2 is often used as the field plate dielectric, while for Ga_2O_3 whose dielectric is proper still needs to be investigated.

Recently, Cha *et al.*[13] studied the field plate structure of Ga_2O_3 SBD with a p-type drift layer by simulation. They found that the dielectric should possess both high permittivity and a high breakdown field. This work focuses on a Ga_2O_3 SBD with an n-type drift layer. The field plate is studied to provide improved reverse electric field (E-field) distribution of Ga_2O_3 SBDs, which is conducive to breakdown performance. The work is based on simulations and three kinds of dielectrics. A series of field plate overlaps and dielectric thicknesses are studied systematically.

2. Simulation details

The simulations are carried out by using Silvaco TCAD software. The parameters of Ga_2O_3 are cited mainly from Ref. [14]. The Ga_2O_3 band gap and affinity are 4.8 eV and 4 eV, respectively. The work function of the Schottky electrode is 5 eV. The thickness and electron concentration of the Ga_2O_3 drift layer are 7 μm and 1×10^{16} cm^{-3}, respectively. The drift layer thickness is the same as that in Refs. [12] and [15]. Figure 1(a) indicates that the breakdown voltage for such a Ga_2O_3 drift layer is larger than 4000 V theoretically. The electron concentration of Ga_2O_3 substrate is 1×10^{19} cm^{-3}. SiO_2, Al_2O_3, and HfO_2 are employed as the field plate dielectric, respectively. The dielectric are the same as that in Ref. [13], their permittivity values are 3.9, 9.3, and 22, respectively. The maximum electric field intensity in Ga_2O_3 drift layer, at the edge of the Schottky junction (E_j) and the edge of the plate (E_p), as a function of the overlap are studied at

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different values of dielectric thickness and reverse voltage. In addition, the maximum electric field intensity in the dielectric (E_d), located at the edge of plate, as a function of dielectric thickness is also studied. The reverse bias voltages are 600 V and 1200 V, respectively. The range of field plate overlap is 1 μm–20 μm. The thickness ranges of SiO_2, Al_2O_3, and HfO_2 are 200 nm–500 nm, 300 nm–700 nm, and 300 nm–700 nm, respectively. The device structure is shown in Fig. 1(b).

In addition, 4H–SiC and GaN counterparts with similar device structures are also presented for comparison. The thickness and electron concentration of the drift layer are the same as those of Ga_2O_3. The field plate overlap is 20 μm. The thickness range of SiO_2, Al_2O_3, and HfO_2 are 200 nm–300 nm, 300 nm–600 nm and 300 nm–900 nm, respectively. The SiC band gap and affinity are 3.2 eV and 3.5 eV, and the GaN band gap and affinity are 3.4 eV and 4 eV, respectively. The work function of the Schottky electrode is 4.5 eV for SiC and 5 eV for GaN, thus keeping the same Schottky barrier height as that in the case of Ga_2O_3.

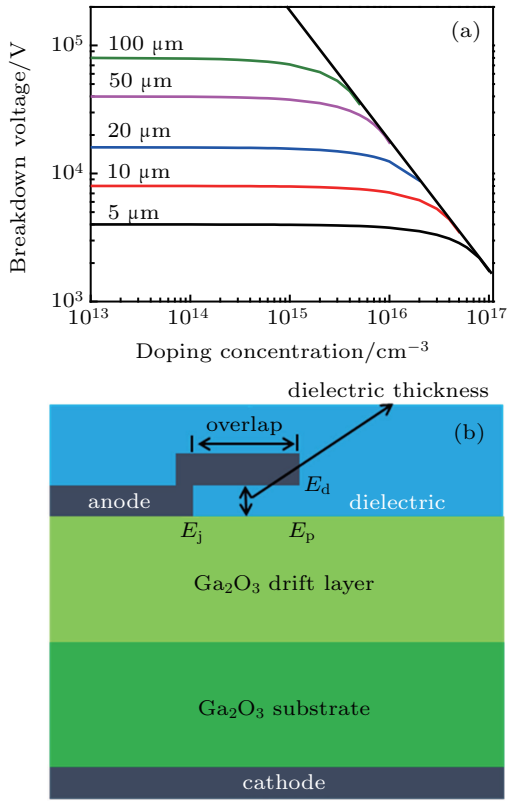


Fig. 1. (color online) (a) Breakdown voltages *versus* doping concentration for different Ga_2O_3 thicknesses; (b) schematic diagram of the field plate termination of Ga_2O_3 SBD.

3. Results and discussion

Figure 2(a) shows the variations of E_j and E_p with overlap and SiO_2 thickness at 600 V. It is seen that, as the overlap increases from 1 nm to 5 μm, the E_j decreases quickly and the E_p increases slightly; as it exceeds 5 μm, their variations both become very slow. To save the termination area, 10 μm length overlap is sufficient. When the SiO_2 thickness is 200 nm, the E_j and E_p eventually tend to 2.66 MV/cm and 2.9 MV/cm, respectively. In this case, E_j is smaller than E_p. As SiO_2 thickness is 250 nm, both of the values tend to 2.81 MV/cm and 2.66 MV/cm, respectively. In this case E_j becomes greater than E_p. As SiO_2 thickness further increases, their gap becomes larger. Since the function of the field plate is to share the high termination electric field, it is ideal when E_j and E_p are both small and equal. Therefore, Fig. 1(a) reveals that the optimal SiO_2 thickness is between 200 nm and 250 nm at 600 V.

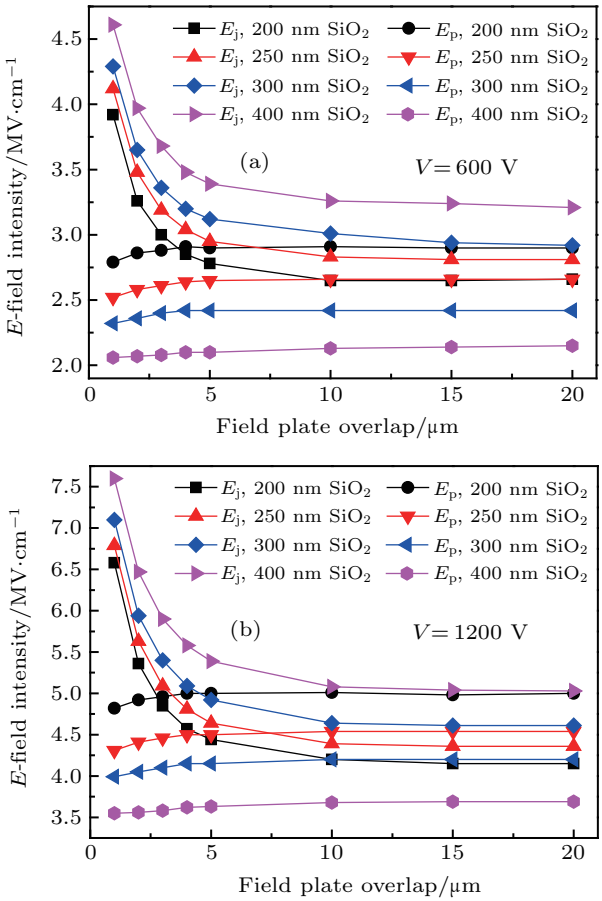


Fig. 2. (color online) Plots of E_j and E_p *versus* field plate overlap for different SiO_2 thicknesses and reverse bias voltage of (a) 600 V and (b) 1200 V.

Figure 2(b) shows the variations of E_j and E_p with the overlap and SiO_2 thickness at 1200 V. It is seen that the variation tendency is similar to that in Fig. 2(a), but differences still exist obviously. In Fig. 2(b), when SiO_2 thickness is 200 nm, E_j is still smaller than E_p, while their gap becomes larger than that in Fig. 2(a). When SiO_2 thickness is 250 nm, E_p begins to be greater than E_j, which is diametrically opposite to that in Fig. 2(a). When SiO_2 thickness further increases, E_j is still greater than E_p, while their gap becomes smaller. Figure 2(b) reveals that the variations of E_j and E_p at 1200 V are different from those in the case of 600 V, and the optimal SiO_2 thickness will be a little greater than 250 nm at 1200 V.

Figure 3(a) shows the variations of E_j and E_p with the overlap and Al_2O_3 thickness at 600 V. It shows that when

Al_2O_3 thickness is 300 nm, E_j is much smaller than E_p; as it increases to 400 nm, both of the values become almost equal; as it further increases to 500 nm, E_j begins to be larger than E_p. Figure 3(a) reveals that the optimal Al_2O_3 thickness is about 400 nm at 600 V.

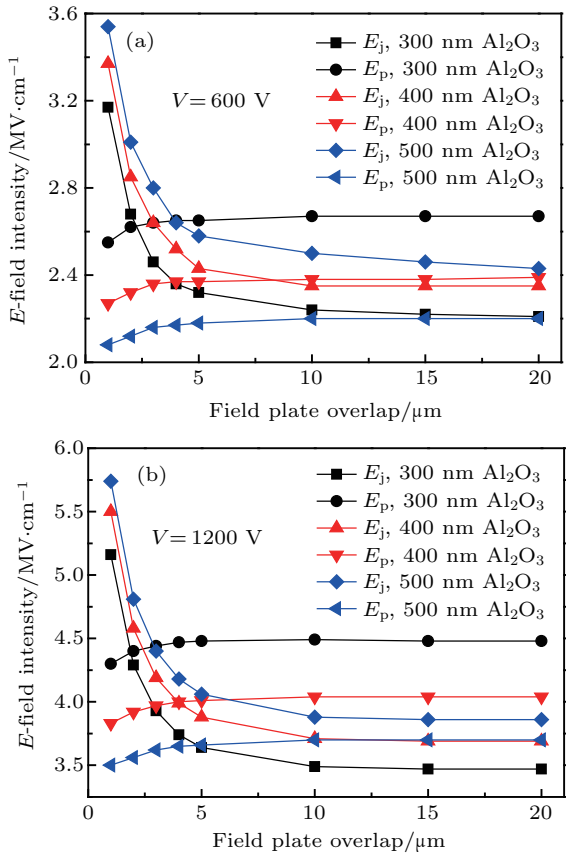


Fig. 3. (color online) Plots of E_j and E_p *versus* field plate overlap for different Al_2O_3 thickness. The reverse bias is (a) 600 V and (b) 1200 V.

Figure 3(b) shows the variations of E_j and E_p with the overlap and Al_2O_3 thickness at 1200 V. Comparing with Fig. 3(a), it is seen that in the condition of 400 nm Al_2O_3 thickness, the gap between E_j and E_p turns larger, signifying that it is no longer the optimal thickness in this case. Moreover, the gap between E_j and E_p becomes very close when Al_2O_3 thickness is 500 nm. So it can be deduced that the optimal Al_2O_3 thickness is a little less than 500 nm at 1200 V.

Figure 4(a) shows the variations of E_j and E_p with the overlap and HfO_2 thickness at 600 V. It is seen that E_j is much smaller than E_p when HfO_2 thickness is 500 nm; as it increases to 600 nm, their gap becomes smaller; as it increases to 650 nm, E_j is just a little smaller than E_p; as it further increases to 700 nm, E_j starts to be greater than E_p. Figure 4(a) reveals that the optimal HfO_2 thickness is between 650 nm and 700 nm at 600 V.

Figure 4(b) shows the variations of E_j and E_p with the overlap and HfO_2 thickness at 1200 V. Comparing with Fig. 4(a), it is seen that E_j is still smaller than E_p, their gap even becomes larger when HfO_2 thickness is 500 nm. The scenario for HfO_2 with 600 nm in thickness is similar to that with 650 nm in thickness. When HfO_2 thickness is 700 nm, E_j is just a little smaller than E_p. It means that at 1200 V, the optimal HfO_2 thickness is greater than 700 nm.

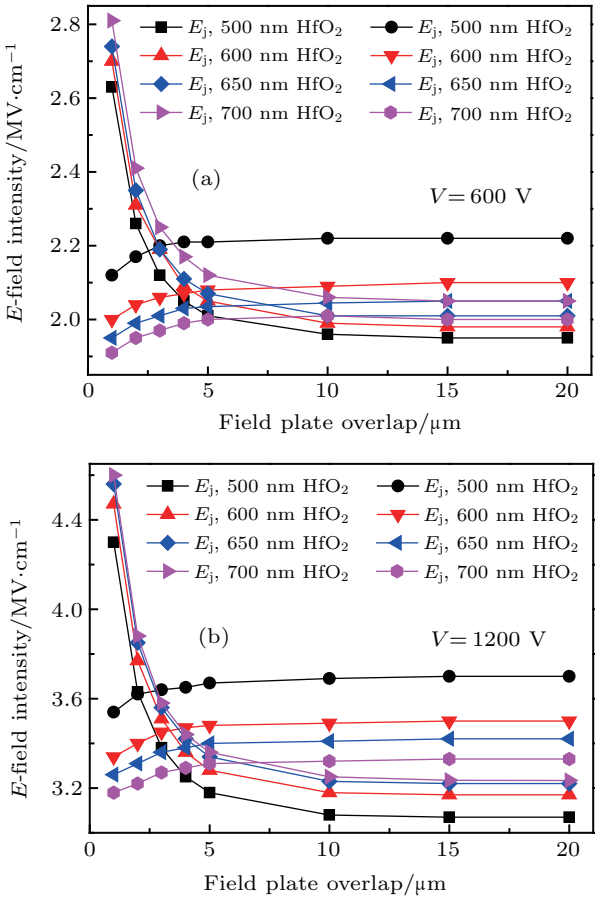


Fig. 4. (color online) Plots of E_j and E_p *versus* field plate overlap for different HfO_2 thickness. The reverse bias voltage is (a) 600 V and (b) 1200 V.

Figures 2–4 reveal that there is an optimal dielectric thickness for a certain circumstance. This is because, on the one hand, the dielectric thickness should be sufficiently thick so that the peak electric field inside the dielectric will not exceed its breakdown intensity; on the other hand, it should also be sufficiently thin so that the field plate can influence the electric field distribution inside the semiconductor and provide sufficient field relief at the edge.[9] It is also observed that, as the reverse bias increases, the optimal thickness increases accordingly in the condition of same dielectric, which is very significant for designing the different voltage rate SBDs. Moreover, as the relative permittivity increases from 3.9 (SiO_2) to 22 (HfO_2), the optimal dielectric thickness also increases accordingly. In addition, the E_j and E_p both become smaller at optimal dielectric thickness as the permittivity increases. For example, at 600 V, the lowest values of E_j and E_p are both about 2.8 MV/cm for SiO_2, and decrease to about 2.4 MV/cm for Al_2O_3 and about 2.1 MV/cm for HfO_2, indicating that the higher the permittivity, the lower the breakdown risk of Ga_2O_3 will be.

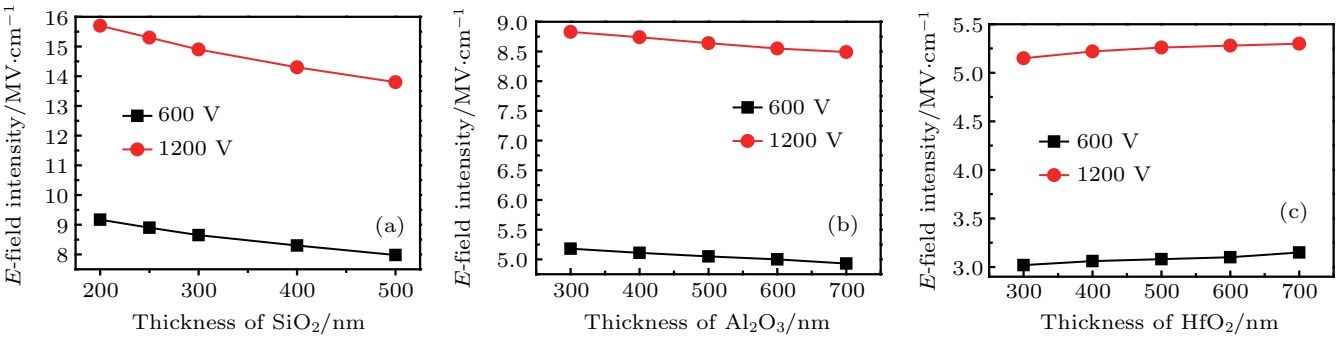


Fig. 5. (color online) Variations of E_d with dielectric thickness, the dielectric is (a) SiO_2, (b) Al_2O_3, and (c) HfO_2.

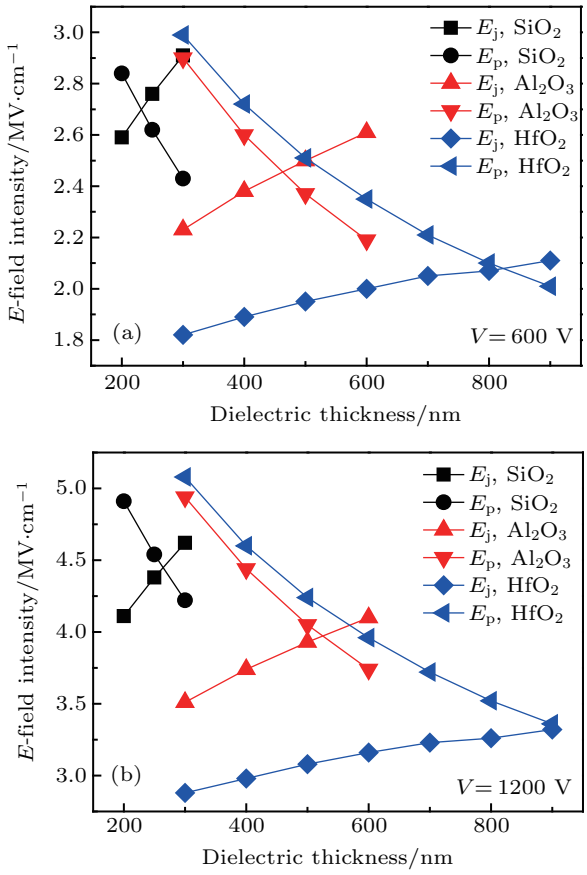


Fig. 6. (color online) Plots of E_j and E_p *versus* dielectric thickness for SiC SBDs. The reverse bias voltage is: (a) 600 V and (b) 1200 V.

Figure 5 shows the relationships between E_d and dielectric thickness for different dielectrics. In Fig. 5(a), it is seen that E_d decreases with SiO_2 thickness increasing. While it is worth noting that it is more than 8 MV/cm and 14 MV/cm at 600 V and 1200 V, respectively. Figure 2 shows that the maximum electric field in Ga_2O_3 is about 2.8 MV/cm and 4.5 MV/cm at 600 V and 1200 V, respectively. Since the critical breakdown electric field (E_c) of Ga_2O_3 and SiO_2 are 8 MV/cm[3] and 15 MV/cm, respectively,[16] suggesting that that SiO_2 is suitable to be the dielectric for the 600-V Ga_2O_3 SBDs but not quit suitable for the 1200 V ones.

Figure 5(b) shows that E_d also decreases with Al_2O_3 thickness increasing, while its decreasing rate is less than the decreasing rate of E_d that decreases as SiO_2 thickness increases. The value of E_d is about 5 MV/cm and 8.5 MV/cm at 600 V and 1200 V, respectively. The corresponding maximum electric field in Ga_2O_3 is about 2.4 MV/cm (Fig. 3(a)) and 3.8 MV/cm (Fig. 3(b)) at 600 V and 1200 V, respectively. Since the E_c of Al_2O_3 is 11.2 MV/cm–13.8 MV/cm,[16] implying that Al_2O_3 is suitable for both the 600 V and 1200 V Ga_2O_3 SBDs.

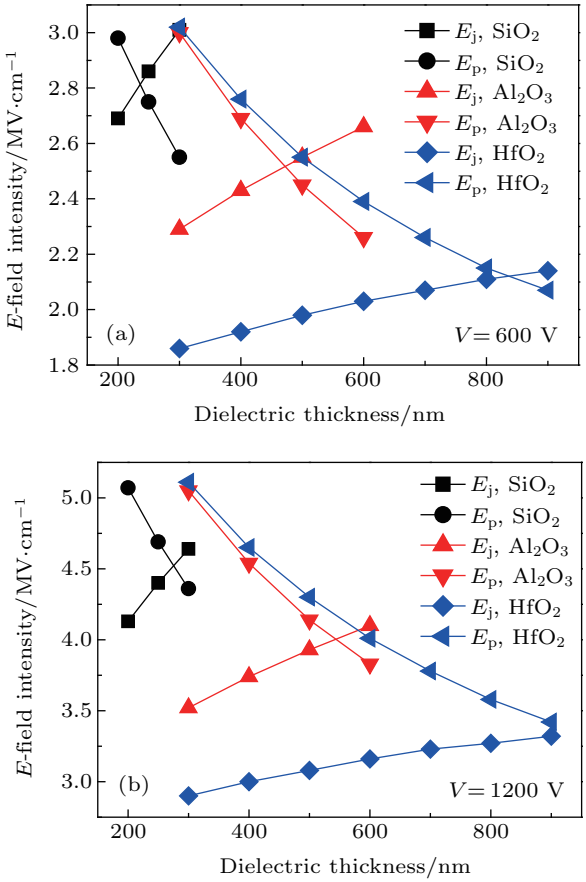


Fig. 7. (color online) Plots of E_j and E_p with dielectric thickness for GaN SBDs. The reverse bias voltage is (a) 600 V and (b) 1200 V.

Figure 5(c) shows that E_d increases slightly as HfO_2 thickness increases, which is different from the scenarios of SiO_2 and Al_2O_3. The E_d is about 3 MV/cm and 5.2 MV/cm at 600 V and 1200 V, respectively. The corresponding maximum electric field in Ga_2O_3 is about 2.1 MV/cm (Fig. 4(a))

and 3.3 MV/cm (Fig. 4(b)) at 600 V and 1200 V, respectively. Since the E_c of HfO_2 is 3.9 MV/cm–6.7 MV/cm,[16] suggesting that it is only suitable for the 600-V Ga_2O_3 SBDs. All the results indicate that the dielectric permittivity of HfO_2 should approach that of Ga_2O_3. Reference [13] indicates that for Ga_2O_3 SBD with p-type Ga_2O_3 drift layer the best choice is HfO_2, thus our results also show that the scenario of the n-type drift layer is different that of the p-type one.

Figure 6 shows the variations of E_j and E_p with dielectric thickness for SiC SBDs at 600 V and 1200 V. Figure 6(a) shows that at 600 V, the optimal SiO_2 thickness is between 200 nm and 250 nm, the optimal Al_2O_3 thickness is between 400 nm and 500 nm, and the optimal HfO_2 thickness is about 800 nm. Figure 6(b) shows that at 1200 V, the optimal SiO_2 thickness is a little larger than 250 nm, the optimal Al_2O_3 thickness is a little larger than 500 nm and the optimal HfO_2 thickness is about 900 nm. Comparing with the results of Ga_2O_3, it is known that at the same reverse bias, the optimal dielectric thickness is larger for the SiC counterpart. Moreover, since the E_c of SiC is 2.5 MV/cm, suggesting that such a SiC drift layer is not able to withstand 1200 V (Fig. 6(b)). In Fig. 6(a), it can also be observed that such a drift layer is not suitable for the 600 V SiC SBD when the dielectric is SiO_2 or Al_2O_3.

Figure 7 shows the variations of E_j and E_p with dielectric thickness for the GaN SBDs at 600 V and 1200 V. Figure 7(a) is for the case with a reverse bias of 600 V, an optimal SiO_2 thickness of nearly 250 nm, an optimal Al_2O_3 thickness is nearly 500 nm, and an optimal HfO_2 thickness larger than 800 nm. Figure 7(b) is for the case with a reverse bias of 1200 V, the optimal SiO_2 thickness is larger than 250 nm, the optimal Al_2O_3 thickness is larger than 500 nm, and the optimal HfO_2 thickness is a little larger than 900 nm. Comparing with the results of Ga_2O_3 and SiC, it is known that at the same reverse bias, the optimal dielectric thickness for the GaN SBDs is even larger than the SiC ones. Furthermore, since the E_c of GaN is 3.4 MV/cm,[17] suggesting that such a GaN drift layer is also not able to withstand 1200 V (Fig. 7(b)).

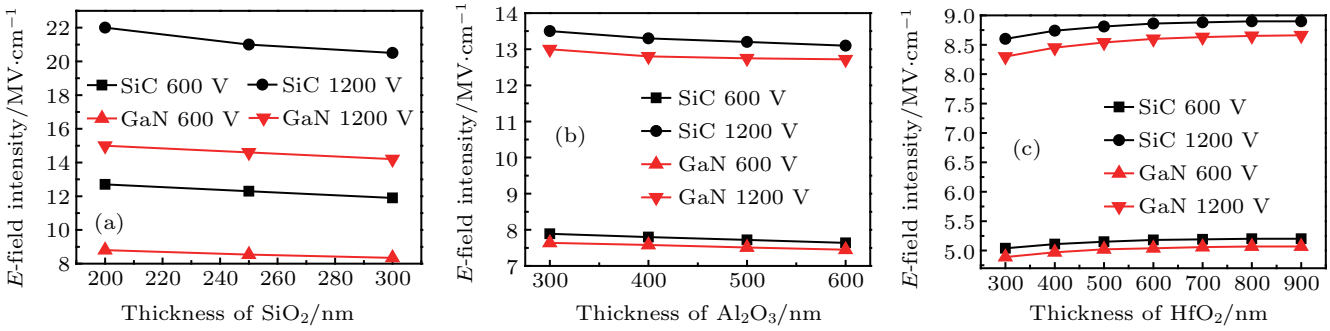


Fig. 8. (color online) Plots of E_d as *versus* dielectric thickness for SiC and GaN SBDs, the dielectric is (a) SiO_2, (b) Al_2O_3, (c) HfO_2.

Figure 8 shows the relationship between E_d and dielectric thickness for the SiC and GaN SBDs. It is seen that at the same dielectric thickness and reverse bias, the E_d of GaN SBDs is less than that of the SiC ones. Combing Figs. 7(a), 8(a), and 8(b), it is clear that such a GaN drift layer is able to withstand 600 V when the dielectric is SiO_2 or Al_2O_3. It is because in such cases the maximum electric field does not exceed the E_c of GaN nor SiO_2 nor Al_2O_3 at 600 V. Figure 8(c) shows that the electric field intensity is about 5 MV/cm in HfO_2 at 600 V. Since the E_c of HfO_2 is 3.9 MV/cm–6.7 MV/cm, suggesting that it is not suitable for the 600-V rate SiC nor GaN power devices. Moreover, figure 6(a) already indicates that the drift layer is not appropriate for the 600 V SiC SBDs either, when the dielectric is SiO_2 or Al_2O_3, implying that the drift layer is not suitable for the 600-V rate SiC devices either, no matter which dielectric is chosen.

Comparing Ga_2O_3 SBDs with the SiC and GaN counterparts, it is known that for Ga_2O_3 devices, the breakdown voltage bottleneck is the dielectric. While for SiC and GaN devices, the bottleneck is mainly the semiconductor itself.

4. Conclusions

In this work, the field plate termination in a Ga_2O_3 Schottky barrier diode (SBD) is studied systematically. Three kinds of oxides, *i.e.*, SiO_2, Al_2O_3, and HfO_2, are used as the field plate dielectric, respectively. The influence of field plate overlap and dielectric thickness on the maximum electric field in Ga_2O_3 as well as the dielectric are studied. The results reveal that the optimal dielectric thickness increases with reverse bias increasing. The maximum electric field intensity decreases in SiO_2 and Al_2O_3, while it increases in HfO_2 with the increase of the dielectric thickness. Moreover, the results also indicates that SiO_2 and HfO_2 are suitable for the 600-V rate Ga_2O_3 SBD, the Al_2O_3 is suitable for both 600-V and 1200-V level Ga_2O_3 SBD. Furthermore, the comparison among Ga_2O_3, SiC and GaN devices reveals that, for the Ga_2O_3 device, the breakdown voltage bottleneck is the dielectric. While, for SiC and GaN devices, the bottleneck is mainly the semiconductor itself.

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