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Impact of variations of threshold voltage and hold voltage of threshold switching selectors in 1S1R crossbar array*

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The impact of the variations of threshold voltage (V_{th}) and hold voltage (V_{hold}) of threshold switching (TS) selector in 1S1R crossbar array is investigated. Based on ON/OFF state *I*–*V* curves measurements from a large number of Ag-filament TS selectors, V_{th} and V_{hold} are extracted and their variations distribution expressions are obtained, which are then employed to evaluate the impact on read process and write process in 32×32 1S1R crossbar array under different bias schemes. The results indicate that V_{th} and V_{hold} variations of TS selector can lead to degradation of 1S1R array performance parameters, such as minimum read/write voltage, bit error rate (BER), and power consumption. For the read process, a small V_{hold} variation not only results in the minimum read voltage increasing but it also leads to serious degradation of BER. As the standard deviation of V_{hold} and V_{th} increases, the BER and the power consumption of 1S1R crossbar array under 1/2 bias, 1/3 bias, and floating scheme degrade, and the case under 1/2 bias tends to be more serious compared with other two schemes. For the write process, the minimum write voltage also increases with the variation of V_{hold} from small to large value. A slight increase of V_{th} standard deviation not only decreases write power efficiency markedly but also increases write power consumption. These results have reference significance to understand the voltage variation impacts and design of selector properly.

Keywords: RRAM, threshold switching selector, crossbar array, variation

PACS: 85.30.–z, 85.40.–e, 72.20.–i **DOI:** 10.1088/1674-1056/27/11/118502

1. Introduction

Resistive switching random access memory (RRAM) has become a popular candidate for next generation non-volatile memories.[1–4] To achieve high density and large capacity for resistive memories, crossbar array architecture is introduced for memory circuit design.[5,6] However, the parasitic leakage paths through unselected cells limit the array size and increase power consumption in operating a crossbar array. To suppress a sneak path current, the selector devices are usually added in series with a resistive memory device, constituting an 1S1R structure.[7,8] Threshold switching (TS) selectors based on metal filament have attracted much attention due to its large ON/OFF ratio, low leakage current, and compatibility with CMOS process.[9] As an important part of 1S1R structure, selector parameters have great effects on 1S1R array performance. Many studies[10–12] have investigated the impact of the selector characteristics on the performance of 1S1R arrays. But most of them assume that the selector is ideal. In fact, because of the non-uniformity existing in filament set-up process, the selector's characteristics may have a large variation. For example, threshold voltage (V_{th}) and hold voltage (V_{hold}) always have a non-negligible variation in the range of hundreds of mV. The variation in TS selectors potentially introduces serious problems to the array's operation, such as the increase in power consumption and high bit error rate (BER).

To investigate the impact of voltage variations of threshold switching selectors in 1S1R crossbar array, in this work—based on ON/OFF state *I*–*V* curves measurements from a large number of Ag-filament TS selectors—the variations of V_{th} and V_{hold} are expressed to evaluate the impact on the performance parameters from a 32×32 1S1R crossbar array.

2. Statistic and expressions for variations of V_{th} and V_{hold} of TS selectors

The statistics and expressions of variations of V_{th} and V_{hold} of TS selectors are obtained based on measurement results of the Ag-filament TS selectors fabricated by our group.[13] Figure 1(a) shows the measured *I*–*V* curves for numerous TS selectors under switching cycles. These devices have enhanced the performance of high selectivity by more than 10^8 and high ON-state current by greater than 100 μA. The variation of V_{th} and V_{hold} of selectors can be observed.

The variation of V_{th} and V_{hold} can be modeled by the nor-

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mal distribution functions

$$f(V_{\rm th}) = \frac{1}{0.033\sqrt{2\pi}} \exp\left(-\frac{(V_{\rm th}-0.18)^2}{2\times 0.033^2}\right), \quad (1)$$

$$f(V_{\rm hold}) = \frac{1}{0.017\sqrt{2\pi}} \exp\left(-\frac{(V_{\rm th}-0.038)^2}{2\times 0.017^2}\right). \quad (2)$$

Figure 1(b) shows the numerical results of the two normal distribution functions based on statistical distribution. We can see that the normal distributions of $V_{\rm th}$ and $V_{\rm hold}$ reflect real variation of $V_{\rm th}$ and $V_{\rm hold}$ of TS selector samples. In the next section, two models in conjunction with ohmic behaviors of the OFF-state and ON-state current are utilized to evaluate the impact on read and write process in 32×32 1S1R crossbar array under different schemes with MATLAB. During the MATLAB processing, the TS selectors are set to the OFF-state or ON-state, which is triggered by the comparison between applying voltage and $V_{\rm th}$ or $V_{\rm hold}$. A selector and an RRAM in series are connected to wordline and bitline of the crossbar array, respectively. All of the paths current and nodes voltage in the crossbar array can be calculated based on Kirchhoff's law. Furthermore, the 1S1R array's performance parameters, such as power consumption and BER, can be evaluated based on the path's current and the node's voltage.

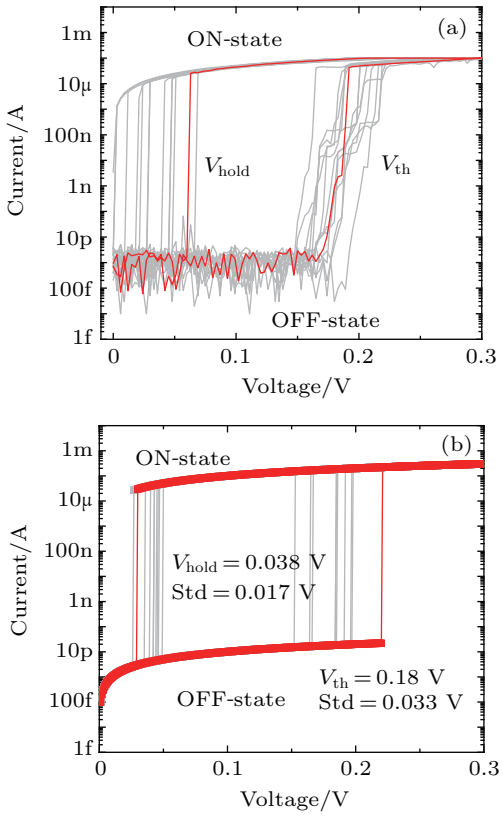


Fig. 1. (color online) *I–V* curves of the TS selector: (a) test results and (b) numerical results of the expressions.

3. Read process

Figure 2 shows the effect of variation of $V_{\rm hold}$ on minimum read voltage ($V_{\rm read_min}$) under different schemes during the read process. A 0.02 V variation of $V_{\rm hold}$ from 0.03 V to 0.05 V can give rise to over 0.1 V increase of $V_{\rm read_min}$. The reason is that with the increase of $V_{\rm hold}$, a larger applied voltage of selector is needed to keep the selector in the ON-state. Consequently, the read voltage is increased due to the increase of $V_{\rm hold}$. There is an insignificant difference in $V_{\rm read_min}$ for the array under difference bias scheme because most of the voltage drop is taken on by the RRAM device when the selector is set to ON-state.

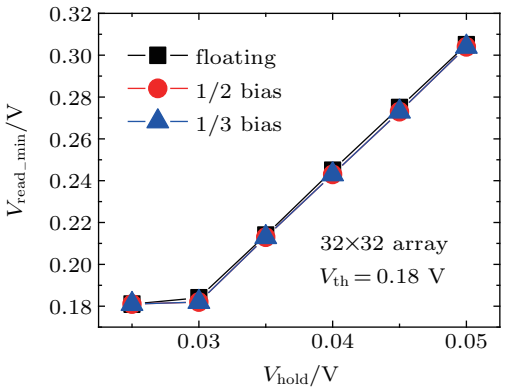


Fig. 2. (color online) $V_{\rm read_min}$ with the variation of $V_{\rm hold}$ for 1S1R crossbar array under different bias schemes.

The BER of a 32×32 array with the variation of $V_{\rm hold}$ and $V_{\rm th}$ is shown in Fig. 3 at $V_{\rm read}=0.3$ V and the array under floating scheme. As shown in Fig. 3(a), when the mean value of $V_{\rm hold}$ increases by only 0.03 V from 0.01 V to 0.04 V with the standard deviation of 0.017 V, the BER increases by two orders of magnitude. Meanwhile, as $V_{\rm hold}$ standard deviation increases from 0.002 V to 0.01 V with the mean value of $V_{\rm hold}$ of 0.038 V, the BER rises greatly, as shown in Fig. 3(b). Under a certain read voltage and standard deviation of $V_{\rm hold}$, the increase of the mean value of $V_{\rm hold}$ will lead to more selectors under the OFF-state and the BER will increase. In another case, when the standard deviation of $V_{\rm hold}$ increases under a certain read voltage and $V_{\rm hold}$ mean value, $V_{\rm hold}$ distribution has a wider range. Therefore, more selectors are triggered to the OFF-state and this will result in serious degradation of the BER. Compared to the mean value of $V_{\rm hold}$, the standard deviation of $V_{\rm hold}$ has more serious degradation on BER. The variation of $V_{\rm th}$ also degrades the BER, as shown in Figs. 3(c) and 3(d). However, the impact of $V_{\rm th}$ on BER is less than that of $V_{\rm hold}$. This happens because the BER mainly depends on the variation of $V_{\rm hold}$ when $V_{\rm read}$ is large enough to make the selected cell stay in ON-state.

Figure 4 show the effect of standard deviation of $V_{\rm th}$ on power consumption and power efficiency under different bias schemes and $V_{\rm th}=0.18$ V during read process. Power is the total power consumption of the crossbar array, which can be calculated by multiplying $V_{\rm read}$ and the sum of output current, and power efficiency can be obtained by the ratio of the power of

selected cell to total power. As the standard deviation of V_{th} increases, the power consumption increases and the power efficiency decreases. The comparison among under different bias schemes reveals that as the standard deviation increases, 1/2 bias tends to result in drastic degradation of power consumption and power efficiency than that in cases of 1/3 bias and floating scheme. For the effect of standard deviation of V_{hold} on power consumption and power efficiency, when the variation of V_{hold} makes BER remain at low level, the cells have less opportunity to be mis-operated. Consequently, V_{hold} has a small impact on power consumption and power efficiency of the crossbar array, and the power consumption and power efficiency are mainly influenced by the variation of V_{th}.

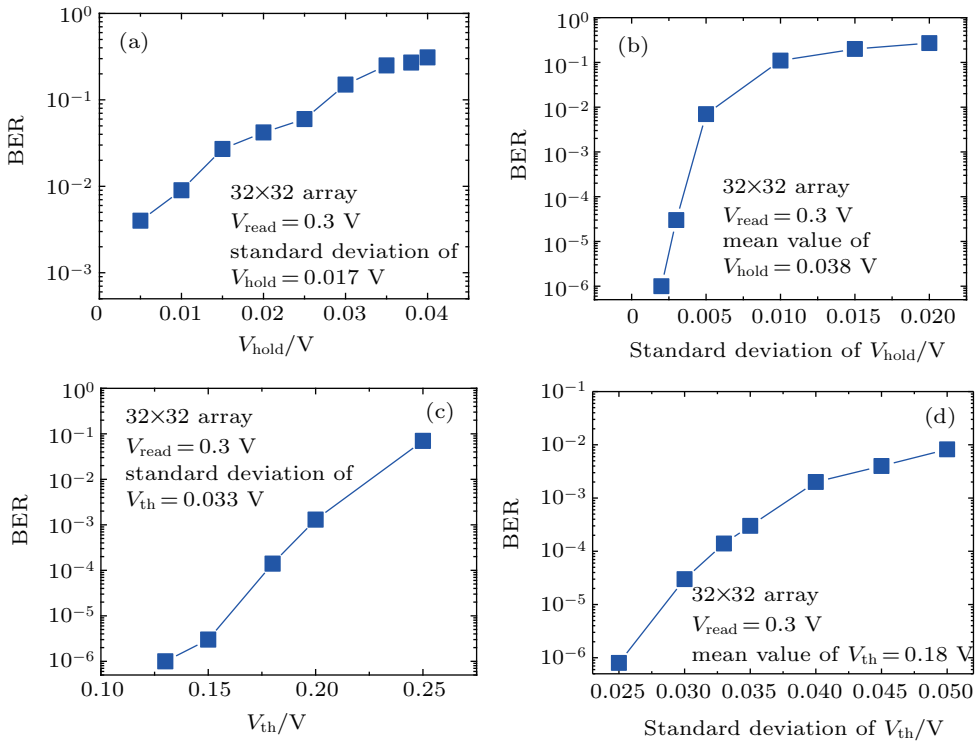


Fig. 3. (color online) BER versus (a) V_{hold}, (b) standard deviation of V_{hold}, (c) V_{th}, and (d) standard deviation of V_{th}.

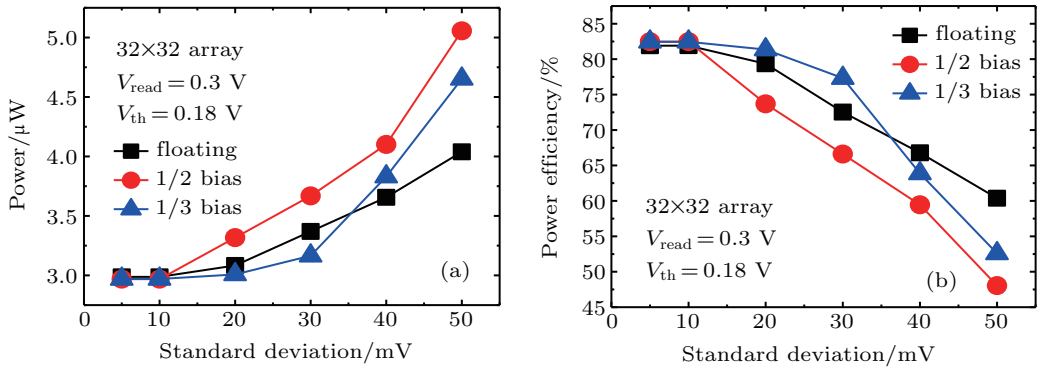


Fig. 4. (color online) The effect of standard deviation of V_{th} on (a) power consumption and (b) power efficiency under different bias schemes.

4. Write process

Figure 5 shows V_{write_min} with a variation of V_{hold} for 1S1R array under different bias scheme during write process. V_{write_min} also increases with a variation of V_{hold} from a small to a large value. This happens because a larger voltage drop of the selector is needed to keep the selector in the ON-state with the an increase of V_{hold}. Therefore, the write voltage is increased due to the increase of V_{hold}. It is observed that V_{write_min} in the 1/2 bias scheme is larger than the write voltage in 1/3 bias scheme. The reason for this is that under 1/2 bias scheme, write voltage is larger in unselected cells, which will cause more leakage current. Thus, a larger voltage is needed to compensate the required voltage for switching a RRAM device, which results in high V_{write_min}. Therefore, the performance is degraded due to the variation of V_{hold}.

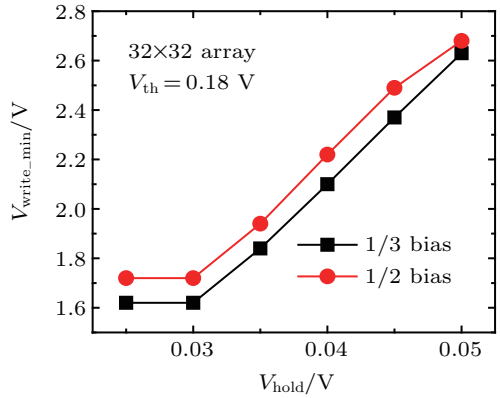


Fig. 5. (color online) V_{write_min} with the variation of V_{hold} for 1S1R array under different bias scheme.

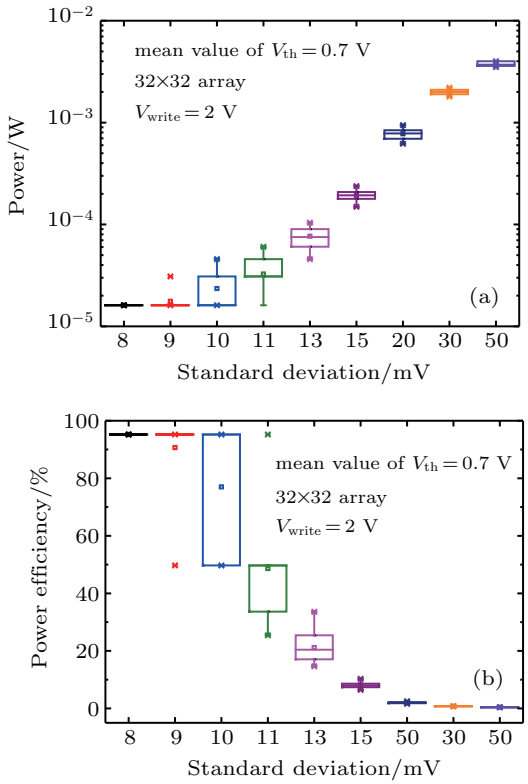


Fig. 6. (color online) The effect of the standard deviation of V_{th} on (a) power consumption and (b) power efficiency.

Figure 6 depicts the impact of the variation of V_{th} standard deviation on power consumption and power efficiency, where the mean value of V_{th} is 0.7 V to ensure that the unselected cells keep in OFF-state. Power is the total power consumption of crossbar array which can be calculated by multiplying V_{write} and the sum of output current, and power efficiency can be obtained by the ratio of the power of selected cell to total power. As the standard deviation of V_{th} increases, the power consumption increases and the power efficiency decreases. When the standard deviation of V_{th} increases from 8 mV to 50 mV, the power consumption increases by more than two orders of magnitude, as shown in Fig. 6(a), and the power efficiency decreases by 93%, as shown in Fig. 6(b). This happens because the increases of standard deviation mean that more unselected cells are unexpectedly turned on. Consequently, the power consumption increases and the power efficiency decreases markedly. Therefore, the performance is degraded due to the large standard deviation of V_{th}.

5. Conclusion

The impact of variability of threshold voltage (V_{th}) and hold voltage (V_{hold}) of selectors in a 1S1R crossbar array is investigated. For the read process, as V_{hold} varies from small to large value, the minimum read voltage increases. As the mean value of V_{hold} and standard deviation of V_{hold} increase, the performance of BER degrades drastically, and a small increase of V_{th} standard deviation leads to a rapid decline of power efficiency. Furthermore, the case under 1/2 bias tends to become most serious. During the write process, a small increase of V_{hold} can cause a large degradation of the minimum write voltage. With a slight increase of V_{th} standard deviation, there is a marked decrease in write power efficiency and an increase in write power consumption. These results indicate that V_{th} and V_{hold} variations of TS selector can degrade the performances of 1S1R array seriously, such as minimum read/write voltage, BER, and power consumption. This paper has significance because it helps us to properly understand the impacts of voltage variation and the design of the selector.

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