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Analysis of tail bits generation of multilevel storage in resistive switching memory*

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The tail bits of intermediate resistance states (IRSs) achieved in the SET process (IRS^S) and the RESET process (IRS^R) of conductive-bridge random-access memory were investigated. Two types of tail bits were observed, depending on the filament morphology after the SET/RESET operation. (i) Tail bits resulting from lateral diffusion of Cu ions introduced an abrupt increase of device resistance from IRS to ultrahigh-resistance state, which mainly happened in IRS^S. (ii) Tail bits induced by the vertical diffusion of Cu ions showed a gradual shift of resistance toward lower value. Statistical results show that more than 95% of tail bits are generated in IRS^S. To achieve a reliable IRS for multilevel cell (MLC) operation, it is desirable to program the IRS in RESET operation. The mechanism of tail bit generation that is disclosed here provides a clear guideline for the data retention optimization of MLC resistive random-access memory cells.

Keywords: resistive random-access memory (RRAM), multilevel cell, tail bits

PACS: 85.30.De, 83.85.Ns, 85.40.Qx **DOI:** 10.1088/1674-1056/27/11/118501

1. Introduction

As the scalability of traditional flash memory cells approaches the physical limits, resistive random-access memory (RRAM) is emerging as one of the most promising candidates because of its outstanding performance, complementary metal oxide semiconductor (CMOS) technology compatibility, and three-dimensional (3D) integration.[1–4] To further increase memory density and reduce fabrication cost, a multilevel cell (MLC) is an effective approach by splitting the RRAM cell into different intermediate resistance states (IRSs). From the mechanism point of view, IRSs can be understood as different geometries/sizes of the conducting filament or the modulation of the tunneling gap in the electrolyte layer.[5–7] Lee *et al.* implemented MLC in a 1T1R device by controlling different compliance currents,[8] whereas Yu *et al.* proposed that MLC could be achieved by varying the RESET pulse width or amplitude,[9] which means that IRSs can be realized either in SET or in RESET operations. However, until now, which one is preferred to achieve reliable IRSs is still an open question.[10–13]

In this work, the tail bits generation of various types of IRSs is investigated in a 1-kb 1T1R array consisting of HfO_2-based conductive-bridge random-access memory (CBRAM) under high-temperature baking. The results show that there are two types of tail bits in IRSs: abrupt increase to an ultrahigh resistance state or shift to a lower resistance state, named tail bits (1) and tail bits (2), respectively. By tracing the program history of these tail bits, more than 95% of tail bits (1) are from the SET process (IRS^S) and tail bits (2) are always observed in the RESET process (IRS^R). A physical model is proposed to account for IRS degradation.

2. Experiments

A 1-kb 1T1R memory array with a Cu/HfO_2/Pt RRAM structure was fabricated in standard 0.13-μm CMOS technology. The 6-nm HfO_2 switching layer and 70-nm Pt top electrodes were deposited by ion beam sputtering and electron beam evaporation, respectively. The size of the RRAM device was 300 nm×400 nm, defined by the Cu plug after chemical mechanical polish (CMP). The gate electrode in every row was connected to function as the word line (WL). The source and drain electrodes in every column were connected in series to form the source line (SL) and bit line (BL). Finally, the memory array was covered by an SiO_2 passivation layer, leaving the test pads exposed. Figure 1(a) shows the schematic of a 1-kb RRAM array.

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3. Testing results and discussion

The electrical characteristics of the memory cells were preliminarily measured by a semiautomatic array testing (SAAT) system. The SET or RESET operation was carried out by applying a positive voltage on BL or SL, respectively. The compliance current (I_{CC}) could be modulated with different voltage bias on WL (V_{WL}). The resistance was measured by a read voltage of 0.1 V. By applying 1.35-V, 1.1-V, and 0.9-V voltages on WL during SET operation, a low resistance state (LRS) valued 10 kΩ and IRSs valued 100 kΩ and 1 MΩ were obtained. Fixing V_{WL} at 2 V, similar IRSs and high resistance states (HRS) could be achieved by setting the RESET voltage as 0.8 V, 1 V, and 1.25 V. The IRSs valued at 100 kΩ and 1 MΩ were named IRS-1 and IRS-2, respectively. Figure 1(b) shows the resistance distribution of MLC in a 2-kb array by either SET operation or RESET operation.

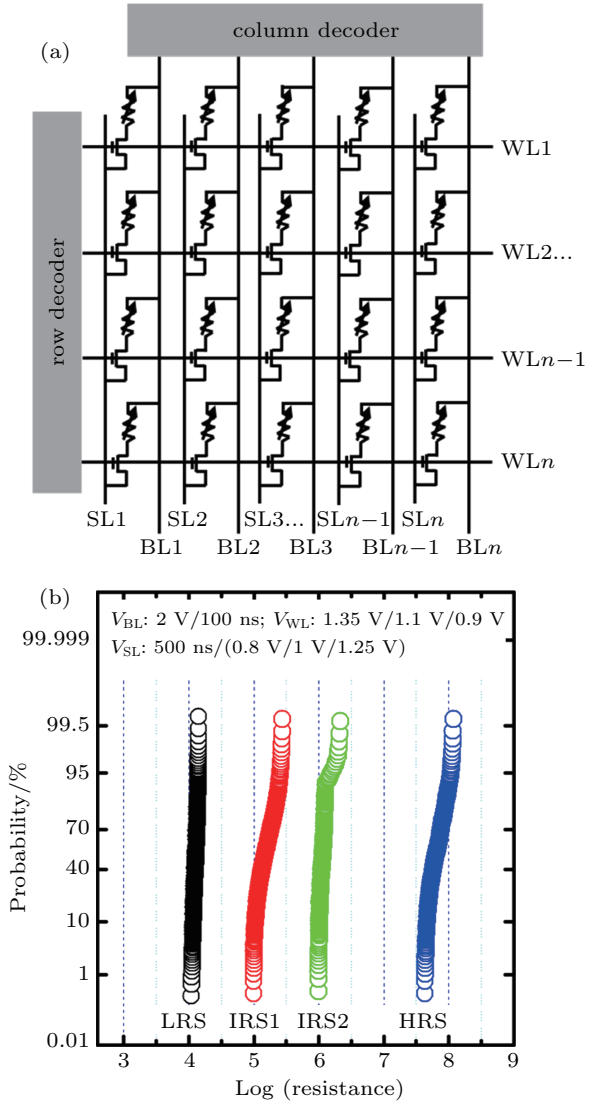


Fig. 1. (color online) (a) Schematic of 1-kb RRAM array. The SET operation is executed by applying voltage bias on BL. For RESET operation, voltage is applied on SL. (b) Multilevel storage is achieved in the 1-kb array by either SET operation or RESET operation.

To investigate the influence of different operation schemes on the retention characteristics of IRS devices, all of the cells in each array were divided into two parts, which were programmed in SET and RESET operations, respectively. The operation history of the cells could be tracked accurately based on the address information. After screening out the unsuccessful IRS cells, approximately 1650 devices were left. Because of the one-pulse scheme and the initial defects introduced by raw materials and manufacturing processes, there are metastable devices that would undermine the results of retention investigation. To ensure the reliability of the retention investigation of IRSs, a prebaking process, a short-time (approximately 50 s) baking at 85 °C, was executed to screen the metastable devices. After prescreening, approximately 1500 cells were left for further statistical analysis. All of the effective devices were baked in a vacuum oven at 110 °C. The resistance of the cells was read out sequentially at predefined intervals.

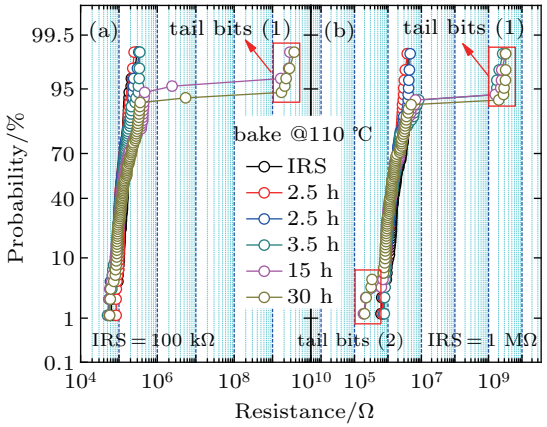


Fig. 2. (color online) Tail bits of IRS data retention: (a) tail bits (1) in IRS-1 after 15-h baking at 110 °C and (b) IRS-2 with two types of tail bits. Historical records of the operations of these bits indicate that most of them stem from IRS^{S}.

Figure 2 illustrates the distribution of IRSs after different baking time. After 15 h, there is a steep rise of device resistance in IRS-1, resulting in two distinct levels. The ultrahigh resistance confuses the IRSs and HRSs, and they are defined as tail bits (1). For IRS-2, tail bits (1) begin to emerge after 2.5 h. In addition, a drift of device resistance toward a lower resistance state is detected after 15 h. Because the preset margin of IRS-1 and IRS-2 is 10 times, the shift in IRS may cause the overlapping of two memory states, leading to a read error that is tail bits (2). Careful examination of the physical states of the failed device indicates that most of the failed cells can be classified as tail bits (1). Figure 3 shows the tendency chart of IRS-2^{S} and IRS-2^{R} under high temperature, which explains the effect of program mode on IRS data retention. The IRS-2^{S} state only contains tail bits (1), whereas the IRS-2^{R} state mainly suffers from tail bits (2), accompanied by a small amount of tail bits (1). Historical records of program

operations reveal that more than 95% of IRS tail bits are programmed in the SET process. The type of tail bit is correlated with the program algorithm adopted. Tail bits (1) are the predominant issue for IRS retention, and the RESET operation is more suitable for MLC applications.

Based on a previous study,[14] filament growth in CBRAM is related to the transportation of Cu ion in the lattice of the electrolyte. The increment in filament length is matched with the hopping conduction of Cu ions between the interstitial sites of the electrolyte lattice. A complete filament formation includes the following four steps: 1) ionization of Cu atoms on the anode, 2) transportation of Cu ions between adjacent interstitial sites of the electrolyte, accompanied by reduction process, resulting in a discrete change of the tunnel conductance, 3) the transition from a tunnel gap region to quantized conductance with the formation of atomic constriction of the filament, and 4) nucleation of Cu ions at the cathode when its concentration reaches a certain value. For HRS and IRS, the resistance is mainly determined by the tunnel gap length.[7]

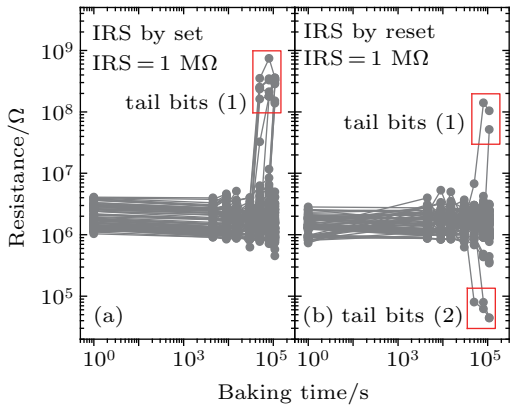


Fig. 3. (color online) Tendency chart of the typical distribution of IRS^S and IRS^R as bake time increases: (a) IRS^S contains tail bits (1) without any tail bits (2) and (b) IRS^R mainly suffers from tail bits (2), accompanied by several tail bits (1).

Based on this result, the IRS^S does not go through the nucleation stage and has lower copper concentration in the filament tip. In contrast, the IRS^R occurs with the rupture of filament associated with the electrical field and joule heating. The resulting residual filament still has the crystal phase and has higher Cu concentration. The different filament morphologies after SET and RESET operations account for the degradation characteristics of IRS^S and IRS^R.

Figure 4 illustrates the physical modeling of IRS retention loss. The difference of copper concentration in the filament tip between IRS^S and IRS^R is clearly shown in Figs. 4(a) and 4(b). The IRS with the same value has a comparable gap length. Under thermal stress, Cu ions diffuse from the residual filament to the surrounding dielectric, including lateral and vertical directions, which leads to the degradation of IRS. The retention time follows the analytical model[13]

$$t_c = \frac{1}{\pi D_0}\left(\frac{N_{Cu}}{N^*}\right)^2 \exp\left(\frac{E_a}{\kappa T}\right), \quad (1)$$

where N_{Cu} is the total number of Cu ions in the conductive filament (CF), and D_0 is the diffusion coefficient. $N*$ is the critical Cu^+ density out of the filament. $N_{Cu}/N*$ is the concentration gradient that determines the diffusion behavior of the copper species in the relaxation processes. E_a is the activation energy for Cu^+ migration.

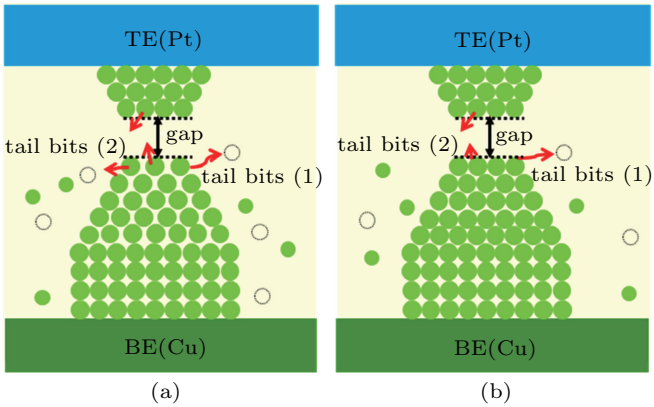


Fig. 4. (color online) Physical modeling for the retention loss of (a) IRS^S and (b) IRS^R. Tail bits (1) result from the depletion progress on the filament tip due to lateral diffusion of Cu ions. Tail bits (2) stem from the vertical diffusion from the residual filament and Cu reservoir on the inert electrode.

When the residual copper species on the filament tip is depleted through lateral diffusion, IRSs abruptly increase, resulting in tail bits (1). The worst tail bits (1) of IRS^S are due to the faster depletion progress as a result of fewer copper species on the filament tip formed during SET program operation. From the hour-glass model, the Cu ion accumulation in the inert electrode serves as an extra reservoir. As the baking time increases, the Cu species diffuse from this reservoir or the residual filament to the tunneling gap through vertical diffusion. When the diffused Cu ions occupy the interstitial sites of the electrolyte in the tunneling gap, the effective length of the gap decreases, this results in the smoothly decreasing resistance of tail bits (2). Because of the larger concentration gradient of IRS^R, shown in Fig. 4(b), the Cu ions diffuse faster along the vertical direction, leading to more tail bits (2) after RESET operation.

The two types of tail bits are confirmed by the IRS retention characteristics at 200 °C (Fig. 5). The IRS is obtained through the same program condition as mentioned previously. Both of the two tail bits are detected in IRS-1 and IRS-2. For IRS-2, tail bits (1) appear after baking 2.5 h, and no more device failure is then detected. After baking 10 h, tail bits (2) appear in IRS-2 as well. Because of the faster diffusion of Cu ions along horizontal and vertical directions under higher temperature, both tail bits (1) and tail bits (2) deteriorate. Taking

the temperature of the memory device (< 85 °C) into consideration, the RESET program is the first choice for MLC applications. After extracting the lifetime, which is defined as the time when 20% of the cells in the array fail under elevated temperatures of 150 °C, 180 °C, and 200 °C, the E_a could be calculated as 0.95 eV through the Arrhenius equation

$$t_c = \exp\left(-\frac{E_a}{\kappa T}\right). \quad (2)$$

The E_a value is consistent with the published results,[14,15] confirming the credibility of this result.

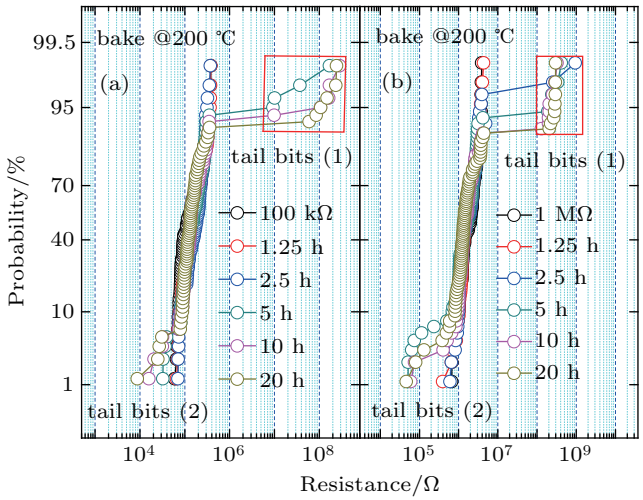


Fig. 5. (color online) Retention characteristics of IRS at 200 °C. For (a) IRS-1 and (b) IRS-2, both tail bits (1) and tail bits (2) are detected. The tail bits deteriorate at higher baking temperatures.

Tail bits have become the main reliability issue for memory chips.[16] Researchers have developed several optimized approaches to minimize tail bits, such as adopting a multilayer structure, improving program algorithms, and improving circuit structure.[17–21] Because of the two types of tail bits in IRSs, the optimization for MLCs would be more complicated and worthy of in-depth study. The underlying mechanism and physical evidence for MLC stability under different program modes need further exploration.

4. Conclusion and perspectives

In this work, the data retention of IRSs programmed in SET or RESET process was investigated. There are two types of tail bits for IRS retention loss. Tail bits (1) appear as the sudden increase to an ultrahigh-resistance state, whereas tail bits (2) behave as a gradual shift toward lower resistance. Under 110 °C, tail bits (1) are the predominant failure type. By tracing the program history, most of the tail bits (1) are produced by SET operation, and tail bits (2) are, for the most part, induced by IRS^R. A physical model is proposed to account for the observed phenomenon. The worse tail bits (1) of IRS^S result from the lower copper concentration on the filament tip. The tail bits (2) of IRS^R result from the high concentration gradient between the residual filament tip and the tunneling gap formed after the RESET operation. These results present a practical guideline for the stability enhancement of IRSs for MLC applications.

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