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Citation: Chin. Phys. B . 2018, 27(10): 108101. **doi:** 10.1088/1674-1056/27/10/108101

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Efficient thermal analysis method for large scale compound semiconductor integrated circuits based on heterojunction bipolar transistor*

Shi-Zheng Yang(杨施政), Hong-Liang Lv(吕红亮)†, Yu-Ming Zhang(张玉明), Yi-Men Zhang(张义门), Bin Lu(芦宾), and Si-Lu Yan(严思璐)

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(Received 23 April 2018; revised manuscript received 2 July 2018; published online 10 September 2018)

In this paper, an efficient thermal analysis method is presented for large scale compound semiconductor integrated circuits based on a heterojunction bipolar transistor with considering the change of thermal conductivity with temperature. The influence caused by the thermal conductivity can be equivalent to the increment of the local temperature surrounding the individual device. The junction temperature for each device can be efficiently calculated by the combination of the semi-analytic temperature distribution function and the iteration of local temperature with high accuracy, providing a temperature distribution for a full chip. Applying this method to the InP frequency divider chip and the GaAs analog to digital converter chip, the computational results well agree with the results from the simulator COMSOL and the infrared thermal imager respectively. The proposed method can also be applied to thermal analysis in various kinds of semiconductor integrated circuits.

Keywords: thermal analysis, temperature distribution, iterative algorithm, compound semiconductor integrated circuit

PACS: 81.70.Pg, 68.60.Dv, 85.40.Qx, 44.05.+e **DOI:** 10.1088/1674-1056/27/10/108101

1. Introduction

InGaP/GaAs or InGaAs/InP heterojunction bipolar transistors (HBTs) are widely used in mixed-signal, high-speed, or high-power circuits[1–4] with the advantages of high cut-off frequency[5–8] while maintaining high breakdown voltage.[9–11] Today, with the development of integrated circuits (ICs) and the growth in military and commercial applications, the size of HBT has been scaled down rapidly for higher operating frequency, leading to a huge number of devices integrated in a small chip and a higher current density. Because of the self-heating and thermal coupling effect, the thermal problem becomes more and more serious in HBTs.[12–14] With the temperature increasing in a device, the electrical device characteristics could degrade due to the thermal instability,[15–17] which reduces the reliability of the circuit seriously.[18–20] Therefore, it is of great importance to evaluate the distribution of temperature accurately during the design of integrated circuits.

With the technology of ICs entering into the nanometer domain, the thermal analysis for large ICs faces great challenges. Many improved numerical methods for fast thermal analysis were developed,[21–24] in which compact heat transfer equations are solved to characterize the temperature distribution in all parts of the IC chip including the thick substrate based on partitioning an IC chip into many discrete three-dimensional (3D) elements.[25,26] The accuracy of the temperature distribution increases with the number of discrete 3D thermal elements increasing. In this case, the calculation would be significantly time-consuming, which makes it hardly possible to achieve a large scale circuit.

However, the heat source generated by the active layer of each device in an IC is usually located in a thin layer close to the top surface of the IC chip, so only the temperature distribution within the related layer is of interest. For an HBT, the current flows from the emitter junction into the collector junction and the collector junction is at high reverse bias, so the power dissipation is mainly from the collector junction.[27] As a result, the collector junction will be the high-temperature region and the highest temperature will be located in the middle area between the base and collector, which is the so-called junction temperature. It will be easy to obtain the important temperature information of the IC chip with minor calculations if the highest temperature in this area is calculated for each heat source, avoiding a huge quantity of calculations of the numerical methods mentioned above.

In this paper, a semi-analytic temperature superposition method (SATSM) is proposed, based on the principle of superposition of temperature with considering the self-heating effect of the device and the thermal coupling effect between devices. The temperature distribution for the full chip can be

*Project supported by the Advance Research Foundation of China (Grant No. 9140Axxx501), the National Defense Advance Research Project, China (Grant No. 3151xxxx301), the Frontier Innovation Program, China (Grant No. 48xx4), and the 111 Project, China (Grant No. B12026).

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easily depicted by calculating the highest temperatures for all devices in a chip with high efficiency and reasonable accuracy. Meanwhile, the temperature dependence of thermal conductivity on the thermal coupling from devices between each other should be considered in implementing the temperature superposition, otherwise, the measured temperature is higher than the calculated temperature and the difference increases with temperature increasing, especially in the high-temperature region.

A more accurate thermal analysis method based on an iterative algorithm, called SATSM-I, is proposed with considering the temperature dependent thermal conductivity. The SATSM-I shows higher accuracy while SATSM exhibits high efficiency and simplicity in calculation. The detailed steps of SATSM and SATSM-I are described in Section 2. The temperature distributions of the InP HBT frequency divider circuit and GaAs HBT analog to digital converter (ADC) chip designed by our research group[28] and calculated by SATSM-I are compared with the results from SATSM, the simulator COMSOL and the infrared thermal imager respectively in Section 3 for verification. Finally, some conclusions are drawn from the present study in Section 4.

2. Temperature distribution calculation procedure

Based on the principle of superposition of temperature, there are three factors to affect the thermal distribution, which include the self-heating effect of the individual device, denoted as $\Delta T_{\rm self}$, the thermal coupling effect from the devices between each other, named $\Delta T_{\rm other}$, and the ambient temperature $T_{\rm a}$.

Therefore, the SATSM calculation procedure mainly consists of two steps.

Step 1.1 The initial temperature $T_{\rm a}$ is assigned to each device in the circuit.

Step 1.2 The temperature increments of $\Delta T_{\rm self}$ and $\Delta T_{\rm other}$ of each device are calculated, according to the semi-analytic temperature distribution function for each kind of device, and the junction temperature T of each device can be worked out finally by temperature superposition. The computation process will be done and the final junction temperature T will be output.

In this case, it is very convenient to obtain the temperature distribution of the HBT IC as long as the semi-analytic temperature distribution function for each device is determined. Each kind of device is firstly simulated by using COMSOL, and the semi-analytic function of the temperature distribution is obtained by fitting with MATLAB. Then, the highest temperature of each device will be worked out with the algorithm based on Steps 1.1 and 1.2, which is implemented in MATLAB.

Table 1 shows the thermal conductivities of the semiconductor materials, in which the thermal conductivity of the semiconductor material decreases as temperature increases. In this case, the $\Delta T_{\rm self}$ and $\Delta T_{\rm other}$ will be intensified when local temperature $T_{\rm Lo}$ is increased. Thus, the temperature of devices calculated by the superposition of the semi-analytic temperature distribution function will be lower than the actual temperature if the temperature dependence of thermal conductivity is not considered.

Table 1. Thermal conductivity of semiconductor material.

Material	Thermal conductivity/(W/m·K)
GaAs[29]	$46\cdot(T/300)^{-1.4}$
InP[29]	$68\cdot(T/300)^{-1.4}$
GaP[29]	$77\cdot(T/300)^{-1.4}$
InGaP[29]	$5.2\cdot(T/300)^{-1.4}$

The influence caused by the thermal coupling effect from the adjacent device in a circuit can be equivalent to the change of local temperature $T_{\rm Lo}$. Thus, $T_{\rm Lo}$ can be replaced by a slightly higher local temperature $T_{\rm Lo-new}$, resulting in the re-change of the thermal conductivity of materials. The $T_{\rm Lo}$ would approximate well to the actual local temperature by the continuous iteration procedure. Therefore, more accurate junction temperature T of each device can be obtained. Based on the idea above, an efficient thermal analysis method (SATAM-I) is proposed with the following calculation steps.

Step 2.1 The initial $T_{\rm a}$ and $T_{\rm Lo}$ are assigned to each device in the circuit.

Step 2.2 The temperature increments $\Delta T_{\rm self}$ and $\Delta T_{\rm other}$ for each device will be calculated, according to the semi-analytic temperature distribution function for each kind of device, and the junction temperature T of each device can be worked out finally by temperature superposition.

Step 2.3 The new $T_{\rm Lo-new}$ of each device can be obtained according to the relationship between T and $T_{\rm Lo}$.

Step 2.4 The computational process will be done and the final junction temperature T will be output if the relative error between $T_{\rm Lo}$ and $T_{\rm Lo-new}$ is less than or equal to the specified iterative precision for all devices in a circuit, otherwise, $T_{\rm Lo-new}$ will be re-assigned to $T_{\rm Lo}$ for the corresponding device and the process will be repeated from Step 2.2 until the precision is satisfied.

In order to realize the total computational process to obtain the temperature distribution of the HBT IC, the temperature distribution of each kind of device is first simulated by using COMSOL, and the semi-analytic function of temperature distribution is obtained by fitting with MATLAB, the same as the process made in SATAM. In the following, the GaAs HBTs with four sizes are taken for example to describe the total computational process.

2.1. Semi-analytic temperature distribution function for individual device

Before making the function fitting for a single GaAs HBT, the model of each kind of device is first set and its temperature distribution is simulated by COMSOL. Figure 1 shows the schematic diagram of a GaAs HBT simulation model. The simulation region is 350 μm×170 μm×100 μm including the backside metallization and passivation layer. For the thermal boundary conditions, the bottom of the model is set to be at different local temperatures and the rest of the boundaries are in natural convection in air. In order to obtain the accurate simulation results, the temperature dependent thermal conductivity is involved as shown in Table 1.

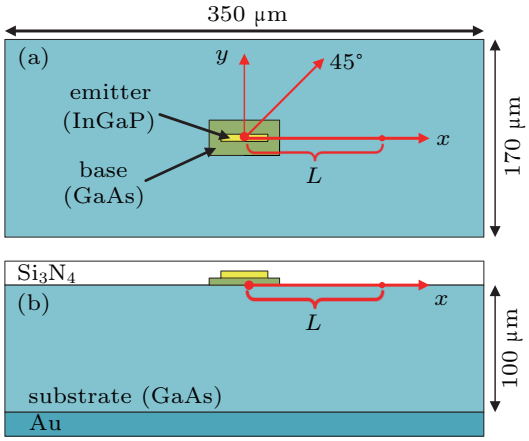


Fig. 1. (color online) Schematic diagram of GaAs HBT simulation model, showing (a) top view and (b) sectional view.

The collector–emitter current flows through the collector-base depletion region with high reverse voltage, resulting in the highest Joule heating. Therefore, heat generation comes from the collector-base depletion region.[30] In order to simplify the model, the power of each device is applied to the interface between the base and collector, which is called the heat source that is assumed to cover the emitter area as shown in Fig. 2. The highest temperature would be located at the center of the heat source, which is called junction temperature.

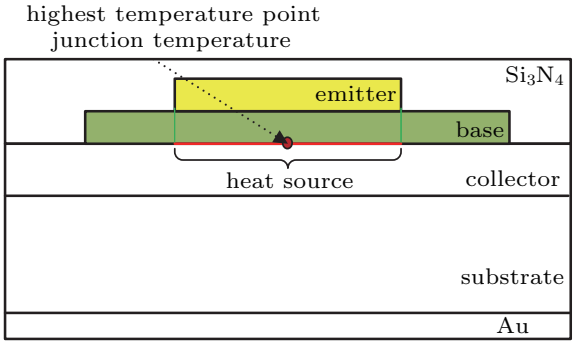


Fig. 2. (color online) Position of the heat source and the highest temperature point in the simulation model.

The $\Delta T_{\rm self}$ is affected by dissipated power p, heat source area s, and local temperature $T_{\rm Lo}$. Thus, $\Delta T_{\rm self}$ is a function of p, s, and $T_{\rm Lo}$ and is expressed as

$$\Delta T = f_1(p, s, T_{\rm Lo}). \tag{1}$$

Figure 3 indicates the center temperatures versus power dissipation from 0 to 20 mW for four devices with different emitter areas. It is apparent that the temperature $\Delta T_{\rm self}$ is a linear function of dissipated power p, and can be expressed by an empirical equation (2):

$$\Delta T_{\rm self} = g_1(T_{\rm Lo}, s) \cdot p, \tag{2}$$

where $g_1(T_{\rm Lo}, s)$ is a function of $T_{\rm Lo}$ and s. The $g_1(T_{\rm Lo}, s)$ increases linearly with $T_{\rm Lo}$ as given in Fig. 4, and $\Delta T_{\rm self}$ can be rewritten as follows:

$$\Delta T_{\rm self} = (g_2(s) \cdot T_{\rm LO} + g_3(s)) \cdot p. \tag{3}$$

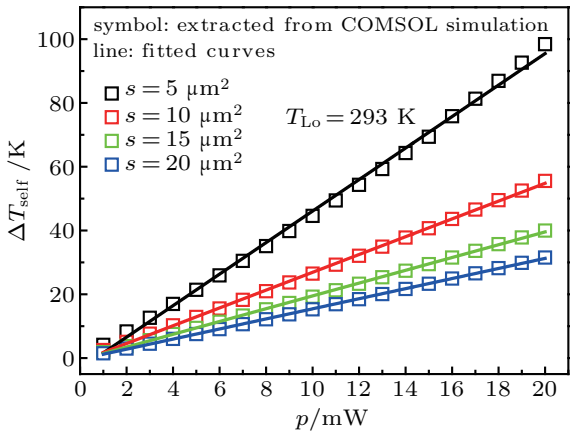


Fig. 3. (color online) Plots of $\Delta T_{\rm self}$ versus p for different sizes of devices at 293 K.

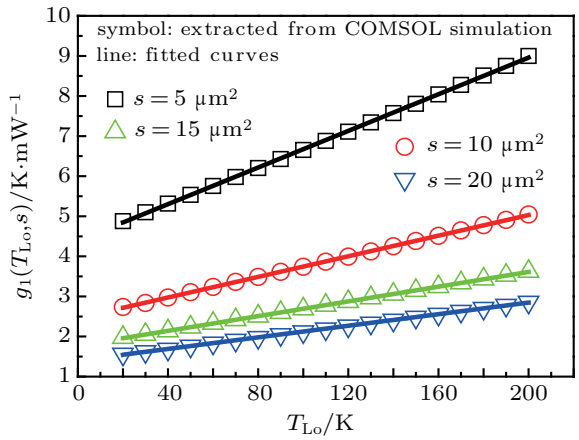


Fig. 4. (color online) Plots of $g_1(T_{\rm Lo}, s)$ versus $T_{\rm Lo}$ for different sizes of devices.

Since $g_2(s)$ and $g_3(s)$ decrease exponentially with s as given in Fig. 5, equation (3) can be rewritten as

$$\Delta T_{\rm self} = (a_1 \cdot s^{a_2} \cdot T_{\rm Lo} + a_3 \cdot s^{a_4}) \cdot p, \tag{4}$$

where a_1–a_4 are four constants extracted from the data fitting in Fig. 5.

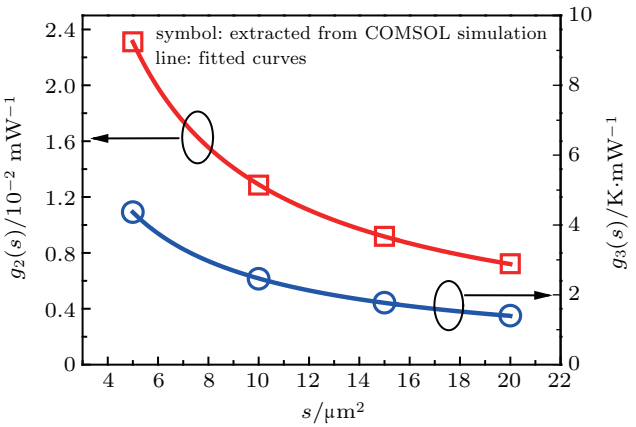


Fig. 5. (color online) Plots of $g_2(s)$ and $g_3(s)$ versus s.

Then the junction temperature $T(i)$ can be given as follows:

$$\begin{aligned} T(i) &= T_{\rm Lo}(i) + \Delta T_{\rm self}(i) \\ &= T_{\rm Lo}(i) + (a_1 \cdot s^{a_2} \cdot T_{\rm Lo} + a_3 \cdot s^{a_4}) \cdot p, \end{aligned} \tag{5}$$

which is the temperature at the center of a single heat source i without the thermal coupling from other heat sources.

Based on the relationship between the junction temperature $T(i)$ and the local temperature $T_{\rm Lo}(i)$ in Eq. (5), $T_{\rm Lo}(i)$ can be derived and expressed as follows:

$$T_{\rm Lo}(i) = \frac{T(i) - a_3 \cdot s^{a_4} \cdot p}{a_1 \cdot s^{a_2} \cdot p + 1}. \tag{6}$$

Figure 6 illustrates the variations of the temperature increment ΔT with distance L from the central point along three directions: x direction, y direction, and 45°-direction in the x–y plane at a power of 10 mW for the device with an emitter area of 5 μm^2 at 300 K, with the three directions shown in Fig. 1. It is obvious that the temperature differences in the three directions are large within a distance of 5 μm, and the maximum temperature difference can reach 25 K between the x direction and y direction because of the rectangle emitter.

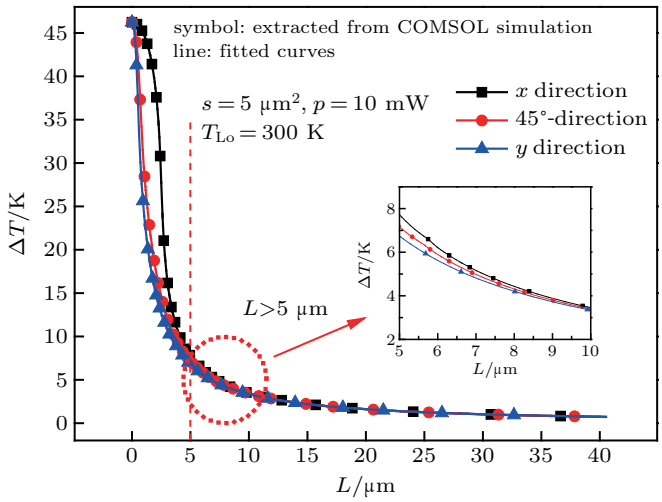


Fig. 6. (color online) Plots of ΔT versus L from the central point along three directions.

Whereas, for the distance larger than 5 μm, the thermal profile is almost the same in the three directions. In this case, it can be found from the layout of the GaAs HBT ICs that the distance from the center point of the device is at least 20 μm. Therefore, there is no big difference of the temperature distributions in three directions for expressing the thermal coupling effect and it is reasonable to choose the x-direction in the following calculation. The 5 μm cut-off distance is adopted for the GaAs HBT technology currently used. For the other types of circuits, the method is also applicable. The difference is that the cut-off distance would decrease to a few nanometers, such as VLSI, where the distance between devices is on the nanoscale.

The temperature increment away from the center point is denoted as $\Delta T_{\rm couple}$. The $\Delta T_{\rm couple}$ is a function of the distance L between two devices, p, s, and $T_{\rm Lo}$. Therefore, $\Delta T_{\rm couple}$ can be expressed as

$$\Delta T_{\rm couple} = f_2(p, s, T_{\rm Lo}, L). \tag{7}$$

Figure 7 shows the temperature $\Delta T_{\rm couple}$ of the device with an emitter area of 5 μm^2 in the x-direction for four different powers at 293 K. It is clear that the temperature distribution at more than 5 μm away from the center point exhibits the power function form as expressed below.

$$\Delta T_{\rm couple} = a_0 \cdot a \cdot L^b + c, \tag{8}$$

where a_0 is defined as $1/\mu m^b$ to express the units of the three above undetermined coefficients a, b, and c conveniently.

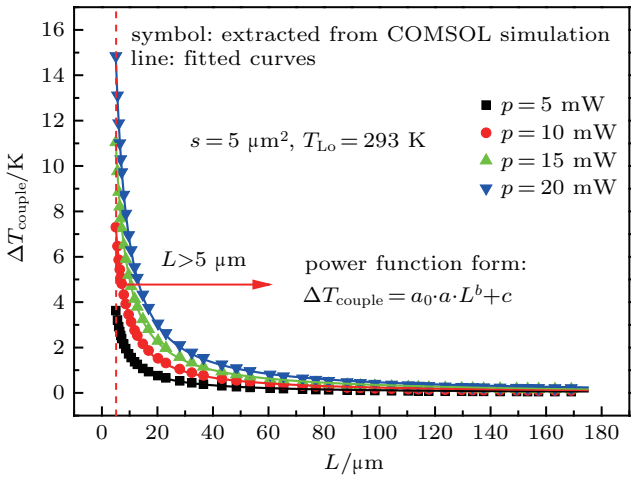


Fig. 7. (color online) Temperature distributions in the x direction for different powers.

This power function of $\Delta T_{\rm couple}$, i.e., Eq. (8), has been verified.[31] Figure 8 shows the temperature increment $\Delta T_{\rm couple}$ versus L with power dissipation caused by a resistor as an on-chip heater from 50 to 110 mW in steps of 20 mW, which is measured by p–n diode sensors at 293 K. The fitted curves in the power function form are consistent with the measured data.

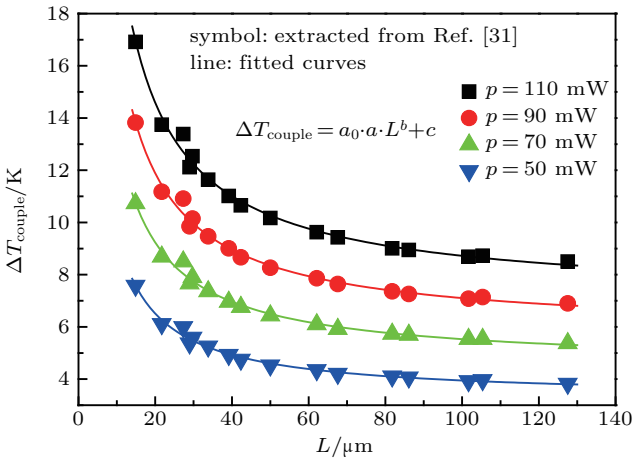


Fig. 8. (color online) ΔT_{couple} versus L for different p at 293 K in Ref. [31].

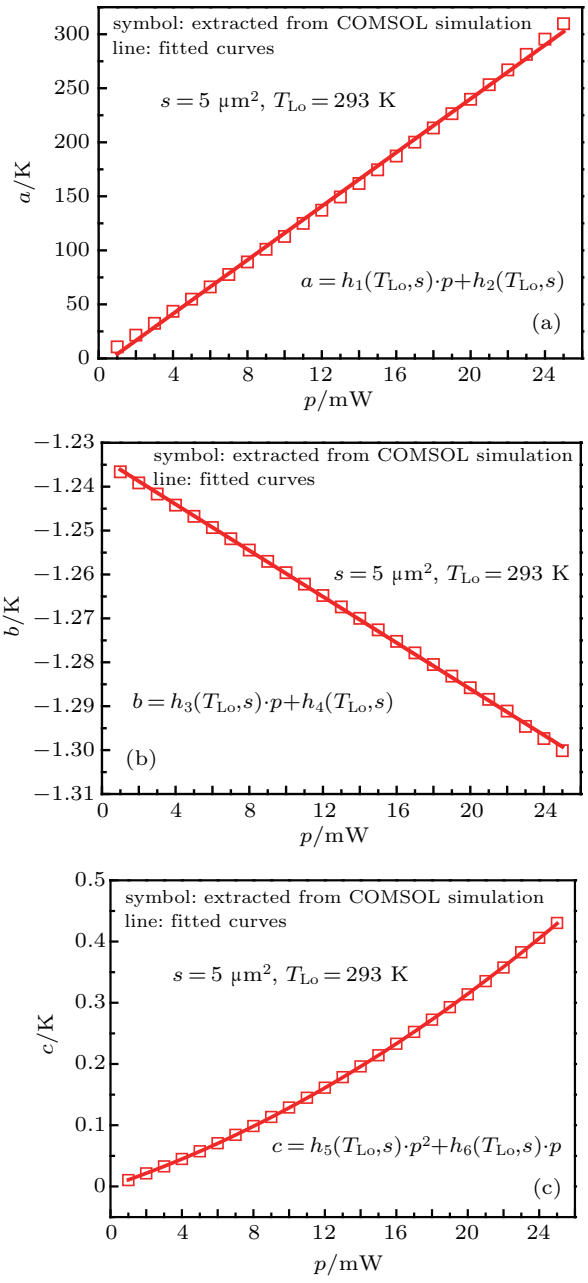


Fig. 9. (color online) Relationships of a, b, and c with p.

Figure 9 shows the relationship of a, b, and c with the dissipated power p for the device with an emitter area of 5 μm² at 293 K. The a, b, and c can be expressed by Eqs. (9), (10), and (11), respectively,

$$a = h_1(T_{Lo},s) \cdot p + h_2(T_{Lo},s), \tag{9}$$

$$b = h_3(T_{Lo},s) \cdot p + h_4(T_{Lo},s), \tag{10}$$

$$c = h_5(T_{Lo},s) \cdot p^2 + h_6(T_{Lo},s) \cdot p. \tag{11}$$

As shown in Fig. 10, $h_1(T_{Lo},s)$–$h_6(T_{Lo},s)$ are linearly related with T_{Lo} separately for the device with the emitter area of 5 μm² at 293 K, which can be expressed as follows:

$$\begin{aligned} h_1(T_{Lo},s) &= h_7(s) \cdot T_{Lo} + h_8(s), \\ h_2(T_{Lo},s) &= h_9(s) \cdot T_{Lo} + h_{10}(s), \\ &\vdots \\ h_6(T_{Lo},s) &= h_{17}(s) \cdot T_{Lo} + h_{18}(s). \end{aligned} \tag{12}$$

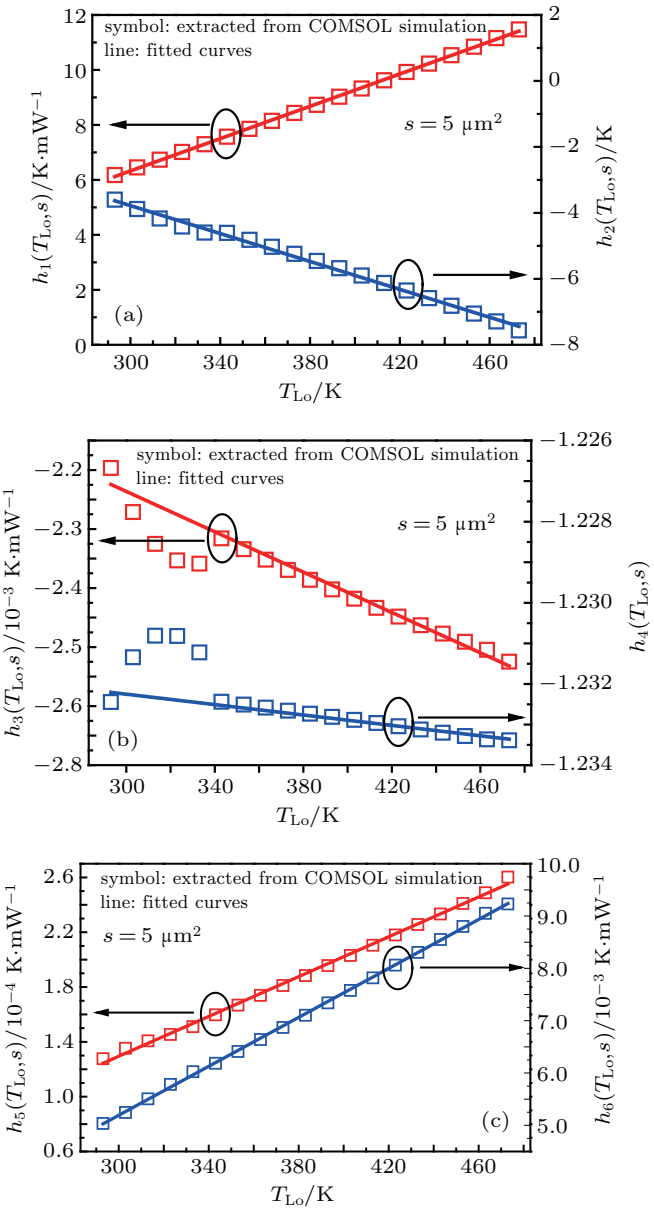


Fig. 10. (color online) Relationships of $h_1(T_{Lo},s)$–$h_6(T_{Lo},s)$ with T_{Lo}.

Then, the functions of $h_7(s) \sim h_{18}(s)$ are fitted with s for four devices. Finally, the temperatures ΔT_{self} and ΔT_{couple} expressed by Eqs. (1) and (7) are determined respectively. Furthermore, the obtained functions can also be re-used for the circuits with the same technology.

2.2. Temperature distribution for full IC chip

For an IC chip with n heat sources, the temperature increment at the center of heat source i is obtained by summing the temperature increment caused by source i itself and coupling heat from the sources of $n-1$ based on the principle of superposition.[32] Then the final junction temperature at the center of heat source i can be written as

$$\begin{aligned} T(i) &= T_{\text{a}}(i) + \Delta T_{\text{self}}(i) + \Delta T_{\text{other}}(i) \\ &= T_{\text{a}}(i) + \Delta T_{\text{self}}(i) + \sum_{k=1, k\neq i}^{n} \Delta T_{\text{couple}}(i), \end{aligned} \tag{13}$$

where T_{a} is the initial ambient temperature, $\Delta T_{\text{self}}(i)$ is its own temperature increment, $\Delta T_{\text{other}}(i)$ is the temperature increment based on the thermal coupling effect from other devices, and $\Delta T_{\text{couple}}(k)$ is the temperature increment from the coupled heat source k. Therefore, the new equivalent local temperature $T_{\text{Lo-new}}$ can be calculated from Eq. (6).

Based on Eq. (6) and the calculation steps, such as Steps 1.1 to 1.2 or Steps 2.1 to 2.4, the junction temperature T of each device can be worked out sequentially by SATSM or SATSM-I to obtain the temperature distribution of the circuit. Also, this method can be generally applied to the thermal analysis for various kinds of semiconductor integrated circuits as long as the geometric models are applied to the corresponding devices in COMSOL.

3. Thermal analysis for compound semiconductor integrated circuits

In this section, the method will be applied to the actual circuits. The SATSM and SATSM-I are codified by MATLAB on a Lenovo QiTianM6500-N000 desktop computer with 8-GB memory and an Intel(R) Core$^{\text{TM}}$ i5-4570 CPU @3.20 GHz. The COMSOL is operated on a DELL R730 server with 128-GB memory and 2 Xeon (R) E–2683 V3 CPUs @2.00 GHz. The first example is an InP HBT frequency divider, which is a small scale IC. The layout of the circuit is shown in Fig. 11, in which 28 transistors are included.

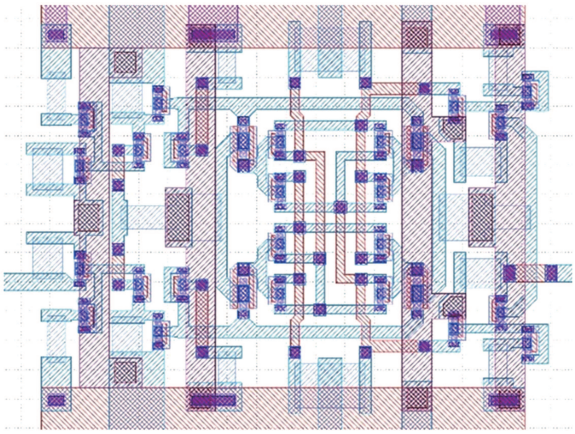


Fig. 11. (color online) Layout of InP HBT frequency divider.

The initial ambient temperature and local temperature surrounding the individual device are set to be 300 K. The calculations of the center temperature for each of all the devices are accomplished within 0.54 second and 0.69 second by SATSM and SATSM-I respectively, and the thermal profiles of the devices in the frequency divider are mapped using MATLAB for 28 devices and shown in Fig. 12(a). It is obvious that the farther the distance from the center of the device, the lower the temperature is. The maximum temperature is 361.03 K located in the center position of the device of No. 13, owing to its higher dissipated power.

In order to validate the temperature distribution, the simulation of the temperature distribution is performed by using COMSOL with a great number of grids, costing CPU time of about 3 hours with the peak memory usage of 100 GB as shown in Fig. 12(b). Therefore, it can be concluded that SATSM and SATSM-I are more efficient than COMSOL. Comparing Fig. 12(a) with Fig.12(b), the maps of the two thermal profiles are consistent with each other. However, there are differences between these two thermal profiles of the full circuit somewhat, because the number of the meshes in COMSOL is far more than that in SATSM-I.

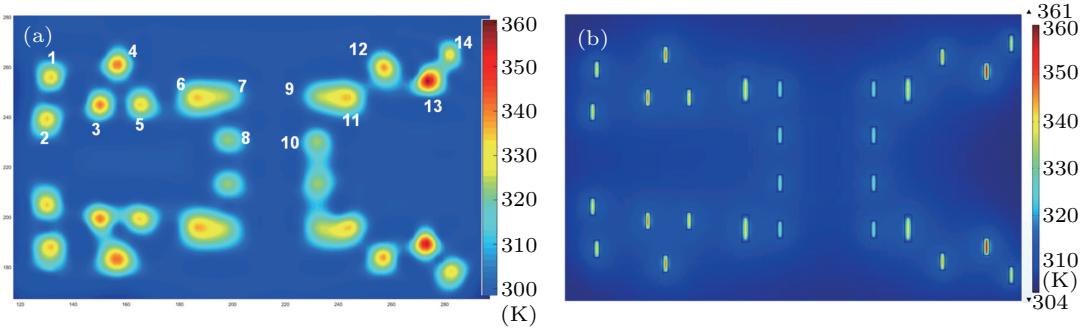


Fig. 12. (color online) Thermal profiles of frequency divider, obtained from (a) SATSM-I and (b) COMSOL.

Table 2 shows the junction temperatures of the devices obtained by using the COMSOL, SATSM, and SATSM-I. Due to the longitudinal symmetry of layout, there are only 14 devices listed in Table 2 and their locations are shown in Fig. 12(a). It can be obviously seen that the results from SATSM-I match the results from COMSOL very well. Furthermore, the mean relative error of the SATSM-I is reduced by 19.35%, which decreases significantly compared with that of SATSM.

Table 2. Comparison among temperatures of frequency divider, obtained from SATSM, SATSM-I, and COMSOL.

No.	COMSOL/K	SATSM/K	SATSM-I/K	Error of SATSM/K	Error of SATSM-I/K	Decrease of relative error/%
1	343.10	342.23	342.77	0.87	0.33	37.93
2	343.05	342.16	342.72	0.89	0.33	37.08
3	350.19	349.23	350.12	0.96	0.07	7.29
4	350.23	349.3	350.11	0.93	0.12	12.90
5	343.42	342.67	343.37	0.75	0.05	6.67
6	343.2	342.47	343.16	0.73	0.04	5.48
7	332.5	332.07	332.63	0.43	0.13	30.23
8	332.56	332.01	332.57	0.55	0.01	1.82
9	332.34	331.96	332.51	0.38	0.17	44.74
10	332.27	331.77	332.31	0.50	0.04	8.00
11	342.85	342.29	342.95	0.56	0.10	17.86
12	345.35	344.64	345.26	0.71	0.09	12.68
13	360.86	360.08	361.03	0.78	0.17	21.79
14	339.8	339.18	339.65	0.62	0.15	24.19

In order to verify the proposed method for large scale IC, a 6-bit 3-Gsps ADC chip is used as a testing example, including 3449 GaAs HBTs processed with 1 μm GaAs HBT technology. Figure 13 shows the full layout of the ADC chip, which consists of THA, folding-interpolating block, digital encoder, etc.

For more than 3 thousand devices, a huge quantity of calculations would take unbearable computation time and memory if the simulation is implemented by using the simulator COMSOL, leading to it being far beyond the capability of the computer. However, this problem can be easily solved by the proposed method with only 58.61 seconds and 242.70 seconds by SATSM and SATSM-I respectively.

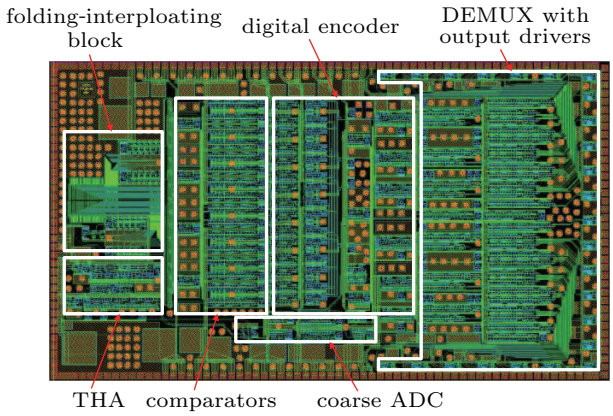


Fig. 13. (color online) Full layout of GaAs HBT ADC chip.

Figure 14 shows the temperature distribution and the isothermal distribution obtained from SATSM-I. In order to figure out the validity of the results from SATSM-I, the temperature distribution of the ADC chip is measured by an infrared thermal imager, and the thermal image of the ADC chip is shown in Fig. 15. As can be seen from Fig. 14(a), the temperatures of regions 1 and 2 are much higher than those of other parts of circuits because of their larger power dissipation. The highest temperature has reached 506 K located in region 1.

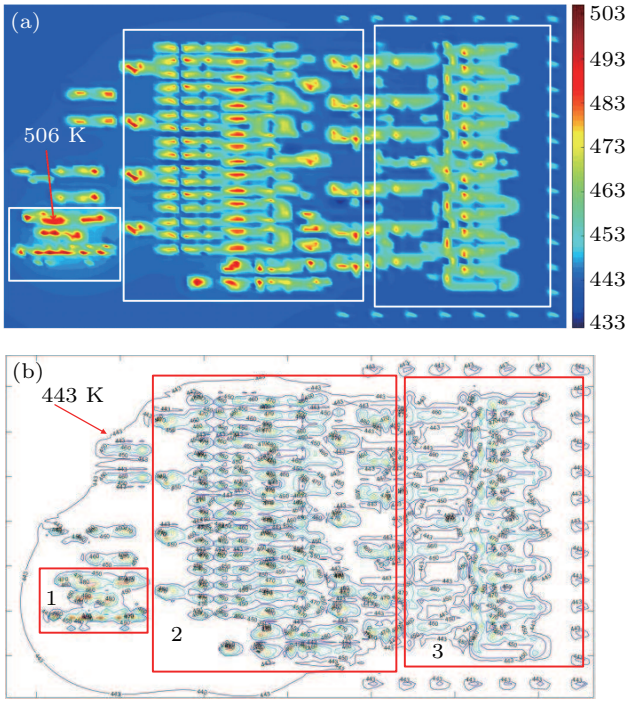


Fig. 14. (color online) (a) Temperature distribution and (b) isothermal distribution of ADC from SATSM-I.

From Fig. 14(b), it is clear to see that the temperature around the chip is about 443 K. Owing to the lower resolution, the thermal imager can only provide an average temperature

in the related range, resulting in a little difference in temperature distribution between Fig. 14(a) and Fig. 15. It is found from Fig. 15 that the ambient temperature of the chip is about 405 K from the green area outside the chip, and the yellow part around the chip is 443 K approximately. The purple and white parts in region 1 are the high-temperature area, with a maximum temperature of about 521 K.

Table 3 shows the results of the chip temperatures, calculated by SATSM-I and SATSM, and also the temperature measured by the infrared thermal imager. Comparing with the measured values, the difference in the highest temperature is 15 K with a relative error of 2.88% obtained by SATSM-I. The SATSM-I reduces the error by 55.56%, compared with the results calculated by the SATSM. For the lower dissipated power than the THA circuit in region 1, the highest temperatures in regions 2 and 3 and the temperature around the chip calculated by SATSM-I are about 493 K and 473 K, which are the same as the measured values, because the variation of thermal conductivity is taken into consideration in implementing the temperature superposition by iterative algorithm.

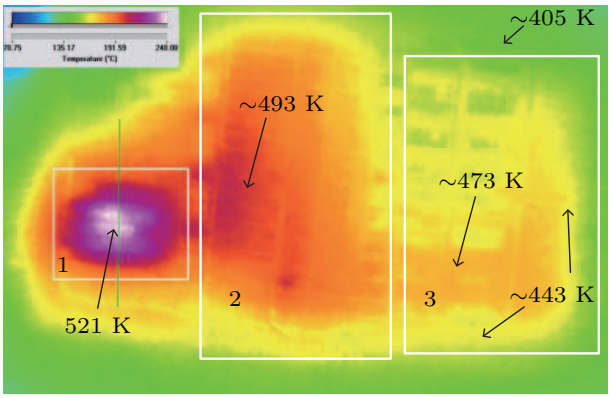


Fig. 15. (color online) Thermal image of ADC chip.

Table 3. Comparisons between chip temperatures calculated by SATSM-I and SATSM with measured values

Method	Ambient temperature/K	The highest temperature in region 1/K	The highest temperature in region 2/K	The highest temperature in region 3/K	Temperature around the chip/K
SATSM	405	494	~ 483	~ 463	~ 438
SATSM-I	405	506	~ 493	~ 473	~ 443
Measured values	405	521	~ 493 (488~498)*	~ 473 (468~478)*	~ 443 (438~ 448)*

*These temperatures are estimated from the thermal image.

As shown from Table 3, the accuracy of SATSM-I is improved more than that of SATSM. However, the temperatures calculated by SATSM-I are almost the same as the measured values except in the highest temperature region, for which the most important reason is that the power dissipation of each device used in the calculation is obtained in circuit simulation software with constant local temperature. Actually, the power dissipation for each device increases with the increase of local temperature in operation because of the temperature positive feedback. Therefore, the difference between the actual temperature and the calculated temperature by SATSM-I or SATSM must be more obvious in the high temperature region. Due to the fact that the thermal radiation of the chip is affected by the surface layer material and the air, the temperature of the thermal image is lower than the actual temperature inside the chip. Therefore, the temperatures calculated by SATSM-I are very close to those from the thermal image. In addition, the interconnections and vias are not considered in the simplified model, which can induce a certain error in calculation. In the proposed method, it is difficult to address all the relevant effects in a single study and therefore further research is needed to strengthen the model. Nevertheless, the modeled results agree well with the measured temperature distribution of the full chip, which demonstrates that the SATSM-I proposed in this paper is effective and suitable for predicting the temperature of a large scale IC with high accuracy and high efficiency.

4. Conclusions

In summary, an efficient thermal analysis method SATSM-I has been presented for large scale compound semiconductor ICs based on HBT. Considering the temperature dependence of thermal conductivity on the thermal coupling effect and self-heat effect, the accuracy of the calculated result from the SATSM-I is significantly improved compared with the SATSM dealing with a fixed thermal conductivity, especially for the higher temperature region. However, the SATSM is also a good choice if power dissipation is lower because of its high efficiency and simplicity of calculation. Moreover, a relative error of the highest temperature from SATSM-I is only about 2.88%, achieving high efficiency operation. It is demonstrated that the proposed SATSM-I can be used in the calculation of temperature distribution and the thermal analysis design for a large scale compound semiconductor IC. Also, this method would be easily applied to other kinds of large scale integrated circuits.

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