Performance enhancement of CMOS terahertz detector by drain current*

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In this paper, we study the effect of the drain current on terahertz detection for Si metal-oxide semiconductor field-effect transistors (MOSFETs) both theoretically and experimentally. The analytical model, which is based on the small-signal equivalent circuit of MOSFETs, predicts the significant improvement of the voltage responsivity R_v with the bias current. The experiment on antennas integrated with MOSFETs agrees with the analytical model, but the R_v improvement is accompanied first by a decrease, then an increase of the low-noise equivalent power (NEP) with the applied current. We determine the tradeoff between the low-NEP and high-R_v for the current-biased detectors. As the best-case scenario, we obtained an improvement of about six times in R_v without the cost of a higher NEP. We conclude that the current supply scheme can provide high-quality signal amplification in practical CMOS terahertz detection.

Keywords: drain current, CMOS terahertz detectors, voltage responsivity, noise equivalent power

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1. Introduction

Recently, there has been a large increase of practical interest in metal-oxide semiconductor field-effect transistor (MOSFET)-based terahertz detectors owing to their advantages, including their low cost, low power consumption, wide spectral response, and their high compatibility with CMOS logic circuits. Further, there has been a significant focus on the research and development of high-performance terahertz detectors that are fabricated by various advanced CMOS technologies. Sherry *et al.*[1] used a more advanced 65-nm silicon-on-insulator (SOI) process technology. Sengupta *et al.*[2] used the modified circuit concepts in combination with a cost-efficient 0.13-μm CMOS technology and the silicon-germanium-based BiCMOS technology. In addition, more researchers have used the thinned substrate technology.[3–5] Although these fabricated chips have a high-R_v and low-NEP compared to those obtained by standard technologies, the fabrications clearly require dedicated facilities as well as more advanced process technologies, which inevitably increase the product cost and manufacturing complexities. Instead of the advanced technologies, recent developments pertaining to CMOS terahertz detectors have demonstrated that the asymmetric FET structures have the potential to dramatically improve the detector performance. These asymmetric structures include the asymmetry when feeding the incoming radiation with a special antenna,[6] the asymmetry between the source and drain structures,[7] and the asymmetry boundary conditions that are due to a current biased to the channel of the devices.[8–12] In the latter case, the external field that induced the electron concentration and potential near the drain side change dramatically, resulting in the device being more sensitive to the external perturbations. However, it should also be noted out that the impressive improvement obtained with the applied current is accompanied by an increase of the detection noise, which limits the applicability of the current-biasing scheme to applications.

In this work, we present an analytical model for current-biased terahertz detectors based on the small-signal equivalent circuit of MOSFETs. Then, we study the R_v and NEP under the current bias condition using antenna-integrated Si MOSFET detectors. Furthermore, we designed a current–mode circuit integrated with the detectors to provide the signal amplification inside the pixel.

2. Small-signal equivalent circuit-based model

We can use sub-micro MOSFETs for terahertz detection as nonlinear properties of plasma wave excitations in FET channels enable their response at frequencies that are appreciably higher than the device cutoff frequency.[13–17] The basic mechanism and operating mode of CMOS terahertz detectors have been described in detail in many studies. When terahertz signals are coupled to the gate terminals of MOSFETs,

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the transistors under the modified gate voltage rectify the signals, generating a DC source–drain voltage, and they can be detected.

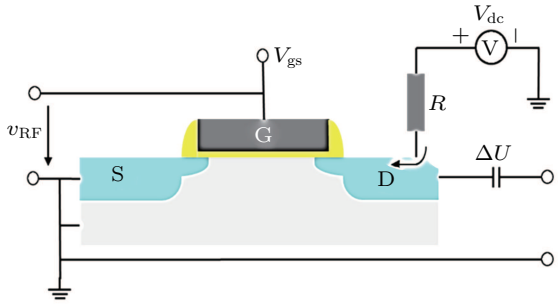


Fig. 1. (color online) Schematic diagram of MOSFETs operating in the terahertz detection mode.

To illustrate the effect of the current bias on the detector response, we first utilize an analytical model to extract R_v and NEP of the current-biased MOSFET detector based on the small-signal equivalent circuit. Figure 1 shows the schematic geometry of MOSFETs used for terahertz detection; here, the drain current I_{ds} is provided by a power supply V_{dc} connected with a resistor R. When the terahertz radiation $v_{RF} = V_{RF} \sin \omega t$ is imported from the source side of the channel, the transistors under the modified gate voltage rectify the signal and generate a dc current and voltage at the drain side as follows:

$$\Delta I = \frac{\mu_n C_{OX} W}{L} \frac{V_{RF}^2}{4}, \tag{1}$$

$$\Delta U = \frac{\Delta I}{G_{ds}}, \tag{2}$$

where G_{ds} is the channel's conductance, which can be readily adjusted by controlling the drain current in the strong inversion condition. By defining FET operation conditions by the values of V_{gs}, V_{ds}, and I_{ds}, we can then calculate G_{ds} as

$$\begin{aligned} G_{ds} &= \frac{\partial I_{ds}}{\partial V_{ds}} = \frac{\mu_n C_{OX} W}{L}((V_{gs} - V_{th}) - V_{ds}) \\ &= \frac{\mu_n C_{OX} W}{L}(V_{gs} - V_{th})\sqrt{1 - \frac{I_{ds}}{I_{ds,sat}}}, \end{aligned} \tag{3}$$

where

$$I_{ds} = \frac{\mu_n C_{OX} W}{L}((V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2), \tag{4}$$

and

$$I_{ds,sat} = \frac{\mu_n C_{OX} W}{L} \frac{(V_{gs} - V_{th})^2}{2}. \tag{5}$$

Substituting Eqs. (1) and (3) into Eq. (2), we can then describe an analytic expression for the rectified voltage ΔU, including the current bias, as

$$\Delta U = \frac{V_{RF}^2}{4(V_{gs} - V_{th})\sqrt{1 - \frac{I_{ds}}{I_{ds,sat}}}}. \tag{6}$$

The equation links the current-induced enhancement of the rectified signal with the ratio of $I_{ds}/I_{ds,sat}$, and predicts that the voltage response ΔU of the MOSFET detector sharply increases when the applied current I_{ds} approaches the saturation current $I_{ds,sat}$ for a given gate voltage. The small-signal analysis of the current-mode provides equations in a similar way to the one developed using the hydrodynamic equation described in Ref. [8]. For the zero-current situation in the strong inversion condition, equation (6) reduces to the well-known relation

$$\Delta U = \frac{V_{RF}^2}{4(V_{gs} - V_{th})^2}. \tag{7}$$

The R_v of the current-biased MOSFET detector can be calculated from Eq. (6) as

$$\begin{aligned} R_v &= \frac{\Delta U}{P_{in}} = \frac{\dfrac{V_{RF}^2}{4(V_{gs} - V_{th})\sqrt{1 - \dfrac{I_{ds}}{I_{ds,sat}}}}}{V_{RF}^2/R_{in}} \\ &= \frac{R_{in}}{4(V_{gs} - V_{th})\sqrt{1 - \dfrac{I_{ds}}{I_{ds,sat}}}}, \end{aligned} \tag{8}$$

where R_{in} is the real part of the input impedance of the detector.

When we consider only the thermal noise in the circuit, NEP of the detectors in the voltage read-out circuit can be written as follows:

$$NEP = \frac{\sqrt{S_{V,Rch} + S_{V,R}}}{R_v}, \tag{9}$$

where $S_{V,Rch}$ and $S_{V,R}$ represent the fluctuations in the thermal noise-voltage fluctuation spectral density induced by the channel resistance and the additional resistor R, respectively.

3. Experimental and results

We fabricated the MOSFET detectors studied here using 0.18-μm standard CMOS technology integrated with a 650-GHz patch antenna with an area S_{det} of 1.1×10^4 μm^2. The gate length and width of the MOSFETs are 0.18 μm and 0.5 μm, respectively, and the threshold voltage V_{th} is 0.5 V. We obtained a terahertz source with a wavelength ranging from 610–680 GHz using an Agilent E8257D signal generator and VDI AMC-T136 frequency multiplier. We measured the ΔU of the devices using the standard lock-in technique, and we measured the noise-voltage fluctuation spectral density of the detector using an Agilent 35670a signal analyzer. Additional components such as integrated amplifiers are not included in the measurement to avoid the excess noise, which makes the study of the pure MOSFET devices with regards to the NEP more difficult.

According to Eq. (8), we can calculate R_v using ΔU and the incident power P_{in} on the detector. To obtain P_{in}, we first calibrated the space distribution of the incident power density, and the radiation power received by the antenna is then calculated as:

$$P_{in} = P_d S_{det}, \tag{10}$$

where P_d is the power density on the detector position and S_{det} represents the antenna area in the detector.

Figure 2 shows the R_v of the detector with the current bias for gate voltages ranging from 0.40 V to 0.53 V. We see that R_v for a given gate voltage first increases significantly with the current, after which it saturates and reaches a maximum voltage responsivity $R_{v,max}$, which is marked by the arrow in the figure. The solid curve in Fig. 2 is related to the calculated responsivity using Eq. (6) for the gate bias $V_{gs} = 0.49$ V. The calculated curve agrees well with the experimental data in the sub-threshold and linear regions of the transistors. However, the deviation between the theoretical calculation and the measured values at the large I_{ds} is significant. There was a previous report of a similar phenomenon in InGaAs/GaAs HEMT detectors, where the deviation is considered to be due to the current saturation of the transistors.[18] To understand the reason for this, we extracted the gate-bias dependence of the saturation current from the R_v of the detector, $R_v - I_{ds}$ curves, and from the $I_{ds} - V_{ds}$ characteristics of MOSFETs. The results are shown in Fig. 3. We observe that two datasets exhibit good agreement, confirming the relationship between the responsivity saturation and the drain-current saturation. Under the condition of saturation currents, the electric field near the drain remains finite with drain currents, leading to the stable channel's conductance and the responsivity saturation.

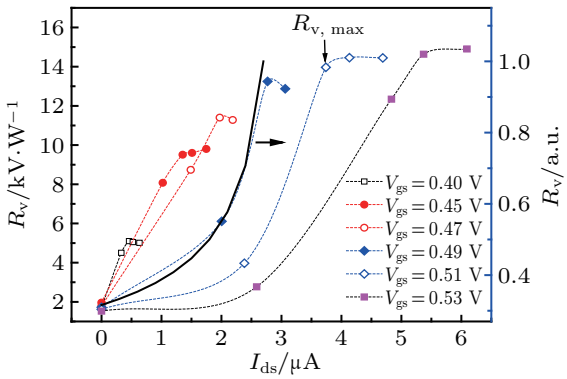


Fig. 2. (color online) Bias-current dependence of R_v for CMOS detector under 680-GHz radiation with a 1 kHz electronic chopper. The solid line represents the theoretical calculation using Eq. (6) for the gate bias $V_{gs} = 0.49$ V. The arrow in the figure shows the value of the current that corresponds to the saturated R_v.

Figure 4 shows the current bias dependence of the $R_{v,max}$ under the various gate biases. For the range of the relatively low bias current, $R_{v,max}$ follows a linear dependence with the current as follows:

$$R_{v,max} = K_1 \times I_{ds} + K_2, \tag{11}$$

where K_1 and K_2 are 4.3 kV/(W·μA) and 2.4 kV/W, respectively. Using the equation, we can predict the possible R_v enhancement of detectors for a given current.

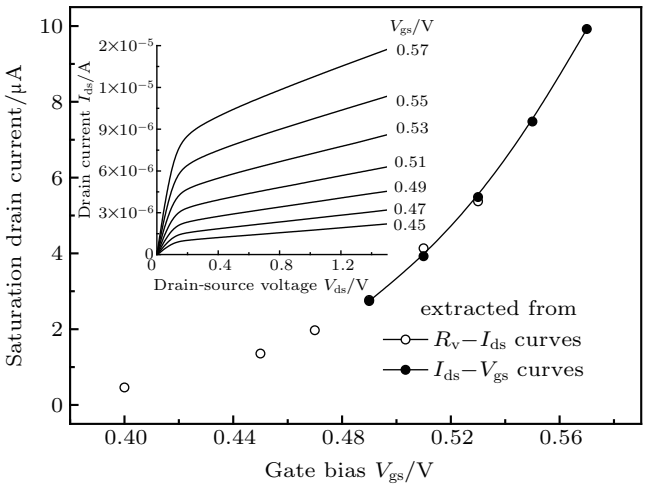


Fig. 3. Saturation drain current versus the gate bias obtained using two different methods. The hollow circle data are extracted from the R_v–I_{ds} curve in Fig. 2, while the solid circle data are extracted from I_{ds}–V_{ds} characteristics of MOSFETs, as shown in the inset of the figure.

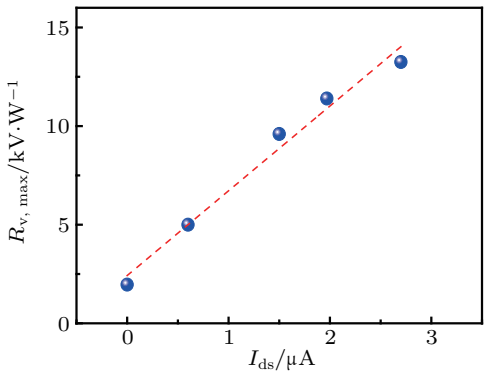


Fig. 4. (color online) Bias-current dependence of $R_{v,max}$. The dashed line is the linear fitting curve.

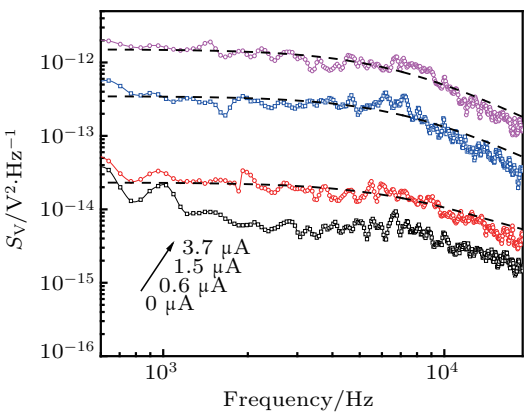


Fig. 5. (color online) Measured S_V of detectors under the condition for $R_{v,max}$. The dashed lines represent the fitting obtained using the noise model, considering the thermal noise and $G - r$ noise source.

Next, we focus on the noise characteristics of the device. Figure 5 shows the measured voltage-fluctuation spectral density S_V of detectors under the various currents. The spectra exhibit frequency dependence, and the bias current enhances the noise level of the detectors. The high-frequency roll-off behavior above 10^4 Hz, which we observed even in the zero-current bias condition, is considered from the loading of the device with an external RC circuit. On the other hand, on the low-frequency side, the noise in the MOSFETs is usually modeled by the thermal noise from the channel resistance. We evaluated the thermal noise spectral density $S_{V,T}$ for the detectors. The results are listed in Table 1, and show that the estimated values obtained from the thermal noise are much smaller than the ones observed in Fig. 5, indicating that other noise sources may be involved besides the thermal noise.

Table 1. Main parameters used in S_{V-f} fitting.

Parameter	Unit	Values		
Drain-source current, I_{ds}	μA	0.6	1.5	3.7
Time constant, τ	μs	10	21	25
Total output resistor, R_{total}	kΩ	122	135	216
Trap density, N_t	eV^{-1}	7×10^{14}	7×10^{14}	7×10^{14}
Thermal noise, $S_{V,T}$	V^2/Hz	2.0×10^{-15}	2.2×10^{-15}	3.6×10^{-15}
G–r noise, $S_{V,G-r}$	V^2/Hz	2.3×10^{-14}	3.4×10^{-13}	1.8×10^{-12}

The $G-r$ noise is one important fluctuation within the range of the low frequencies owing to trapping and de-trapping processes between the carriers and deep-level traps in the oxide layer near the Si/SiO_2 interface of MOSFETs. When we considered the $G-r$ noise mechanism, the total noise spectral density can be expressed as

$$S_V = S_{V,T} + S_{V,G-r}. \tag{12}$$

Here, $S_{V,G-r}$ is expressed as [19]

$$S_{V,G-r} = \frac{\beta}{1+(\gamma\cdot f)^2}, \tag{13}$$

with

$$\beta = \frac{N_T I_{ds}^2 \tau R_{total}^2}{N^2}, \tag{14}$$

$$\gamma = 2\pi\tau, \tag{15}$$

where N and N_T are the total number of free carriers and traps, respectively, and τ is the capture and emission time constant of the carriers.

The proposed model demonstrates a close fit to the experimental frequency characteristic of S_V, as shown in Fig. 5. The parameter values used in the fitting are listed in Table 1. Values such as the intrinsic carrier concentration and trap concentration are obtained from standard MOSFET values. Table 1 also shows the S_V constituents under three fixed current values. We observe that $S_{V,G-r}$ prevails in the measured frequency region when the current flows in the detectors. At the current of 0.6 μA, the $G-r$ noise is about one order of magnitude greater than the thermal noise. The increase in the bias current enhances the $G-r$ noise dramatically, from 2.3×10^{-14} V^2/Hz at 0.6 μA to 1.8×10^{-12} V^2/Hz at 3.7 μA, while the thermal noise component shows a relatively weak current dependence. The significant enhancement of the $G-r$ noise may be due to the larger trapping and de-trapping time constants as well as the channel resistance under the higher currents.

Figure 6 shows the bias current dependence of the NEP that was evaluated from the experimental data of $R_{v,max}$ and S_V at a frequency of 1 kHz. We observe that the magnitude of NEP first decreases and then increases with the applied current. As shown as the black dot in Fig. 6, the detector with an applied current of 2.3 μA has the same NEP value as that of the unbiased detector. We then determined the tradeoff between low-NEP and high-R_v for the current-biased detectors by comparing the data of NEP and R_v in Fig. 4. We found that the performance of CMOS terahertz detectors could be improved by introducing small drain currents below 2.3 μA. In the best-case scenario, we can obtain an improvement by a factor of six in R_v without the need for a more costly NEP. The results reveal that even though there is a relative increase in the voltage noise with the current bias, we may register an unambiguous current-bias condition to provide a high-quality signal amplification for CMOS terahertz detectors.

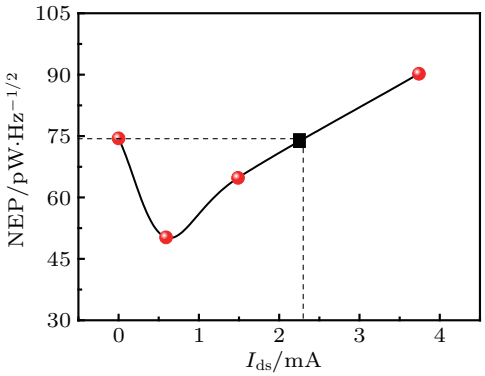


Fig. 6. (color online) Bias-current dependence of NEP evaluated from the experimental data of $R_{v,max}$ and S_V for a modulation frequency of 1 kHz. The black dot shows that the detector with the applied current of 2.3 μA has the same NEP value as that of the unbiased detector.

For MOSFETs, terahertz detection can be self-amplified using the drain current. However, the present current supply scheme using a dc power source with a resistor is not a suitable solution for large-array integrated circuits (ICs). For an increased integration and sensitivity of the CMOS detectors, we then propose an on-chip circuit with the current mirror structure for current-biased CMOS terahertz detectors.

Figure 7 shows the current supplying circuit, which consists of a sub-circuit with a current source (M1–M4) and antenna-coupled FET pairs (M5, M6) in differential operation. In the current-source circuit, the cascode current mirror is the core structure, and can increase the output resistance of a current source and suppress the effect of channel-length modulation on the accuracy of the applied current I_{ds}. The cascode structure can shield the transistor M3 from the variations that are due to the detection circuits, and the voltage bias V_{ds3} is equal to V_{ds1} with high accuracy.[20] By designing suitable-sized MOSFETs, the relationship between I_{ds} and the reference I_{REF}, as shown in Fig. 7, can then be written as

$$I_{ds} = \frac{(W/L)_3}{(W/L)_1} I_{REF}. \tag{16}$$

The equation indicates that a reference current I_{REF} can provide multiple detectors with stable current I_{ds} for array detectors. A CMOS terahertz detector that is integrated with such a current-supply circuit is more conductive to those applications.

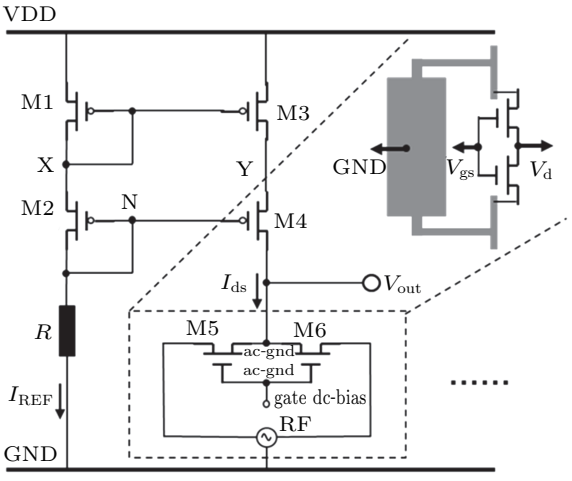


Fig. 7. Schematic diagram applied for CMOS terahertz detectors operating in the current mode. The dashed square indicates the low-frequency equivalent circuit of an antenna-coupled CMOS detector with its high-frequency one presented in the zoomed-up area.

4. Conclusions

We studied the influence of the drain-to-source current on the performance of CMOS terahertz detectors. The analytical model based on the small-signal equivalent circuit of MOSFETs predicts the improvement in the R_v of MOSFET detectors with the bias current. We performed an experiment using antennas integrated with MOSFETs, and the results agree with the analytical model, but the improvement in the R_v that is obtained using the applied current is accompanied first by a decrease, then an increase in NEP. We find that there is a marked improvement beyond the R_v and NEP values of the unbiased device. Further, we designed the current-supply circuit integrated with the detector for practical devices.

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